

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

HFD630A / HFU630A 200V N-Channel MOSFET

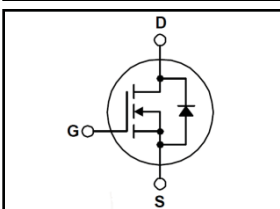
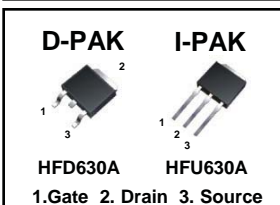
FEATURES

- ❑ Originative New Design
- ❑ Superior Avalanche Rugged Technology
- ❑ Robust Gate Oxide Technology
- ❑ Very Low Intrinsic Capacitances
- ❑ Excellent Switching Characteristics
- ❑ Unrivalled Gate Charge : 12 nC (Typ.)
- ❑ Extended Safe Operating Area
- ❑ Lower $R_{DS(ON)}$: 0.34 Ω (Typ.) @ $V_{GS}=10V$
- ❑ 100% Avalanche Tested

$$BV_{DSS} = 200 \text{ V}$$

$$R_{DS(on) \text{ typ}} = 0.34 \ \Omega$$

$$I_D = 9.0 \text{ A}$$



Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	200	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$)	9.0 *	A
	Drain Current – Continuous ($T_C = 100^\circ\text{C}$)	5.7 *	A
I_{DM}	Drain Current – Pulsed (Note 1)	36 *	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	232	mJ
I_{AR}	Avalanche Current (Note 1)	9.0	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	9.5	mJ
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$)	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	45	W
	- Derate above 25°C	0.36	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

* Drain current limited by maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	2.77	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient*	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 4.5 \text{ A}$	--	0.34	0.4	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 4.5 \text{ A}$	--	5.5	--	S

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	200	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}$	--	--	1	μA
		$V_{DS} = 160 \text{ V}, T_J = 125^\circ\text{C}$	--	--	10	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	± 100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$	--	420	525	pF
C_{oss}	Output Capacitance		--	99	128	pF
C_{rss}	Reverse Transfer Capacitance		--	24	28	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 100 \text{ V}, I_D = 9 \text{ A},$ $R_G = 25 \Omega$	--	11	--	ns
t_r	Turn-On Rise Time		--	91	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	70	--	ns
t_f	Turn-Off Fall Time		--	72	--	ns
Q_g	Total Gate Charge	$V_{DS} = 160 \text{ V}, I_D = 9 \text{ A}$ $V_{GS} = 10 \text{ V}$	--	12	17	nC
Q_{gs}	Gate-Source Charge		--	2.4	--	nC
Q_{gd}	Gate-Drain Charge		--	3.5	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I_S	Continuous Source-Drain Diode Forward Current	--	--	9	A	
I_{SM}	Pulsed Source-Drain Diode Forward Current	--	--	36		
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 9 \text{ A}, V_{GS} = 0 \text{ V}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$I_S = 9 \text{ A}, V_{GS} = 0 \text{ V}$ $di_F/dt = 100 \text{ A}/\mu\text{s}$	--	158	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.97	--	μC

Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L=4.3\text{mH}, I_{AS}=9\text{A}, V_{DD}=50\text{V}, R_G=25\Omega,$ Starting $T_J=25^\circ\text{C}$
3. Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
4. Essentially Independent of Operating Temperature

Typical Characteristics

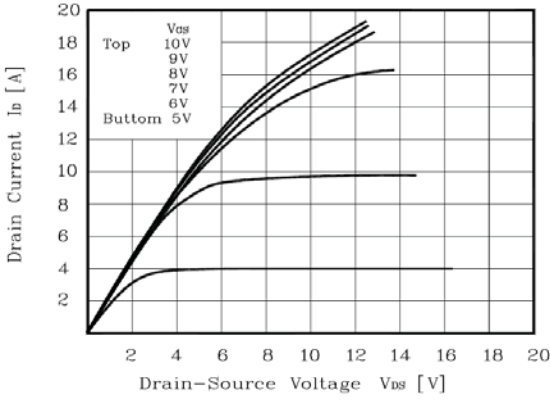


Figure 1. On Region Characteristics

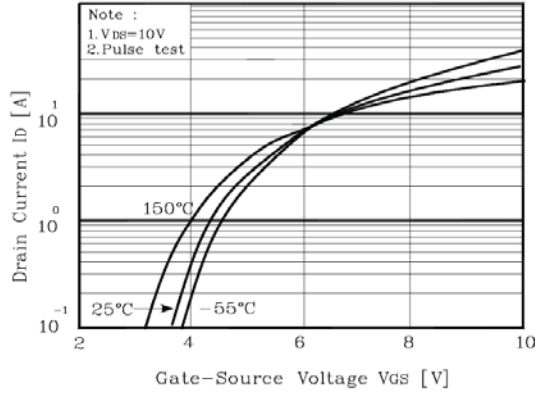


Figure 2. Transfer Characteristics

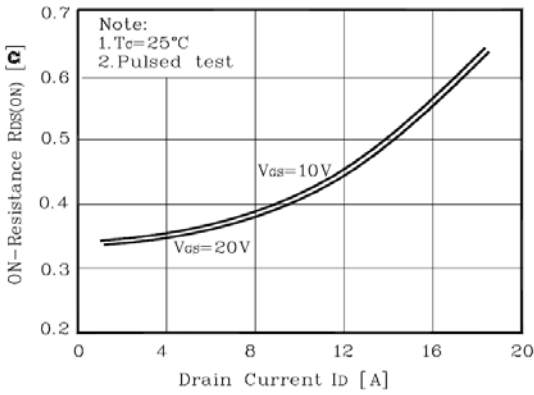


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

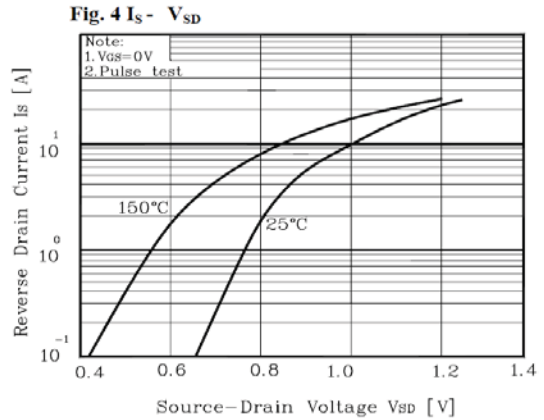


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

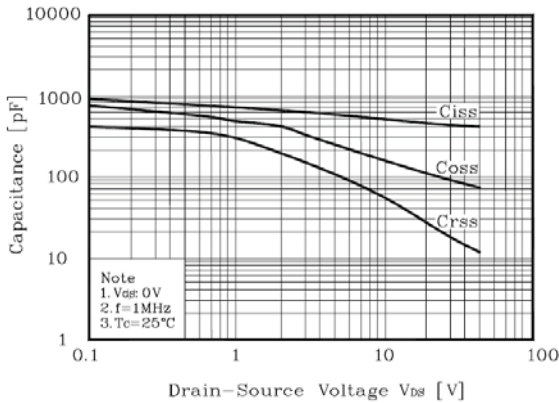


Figure 5. Capacitance Characteristics

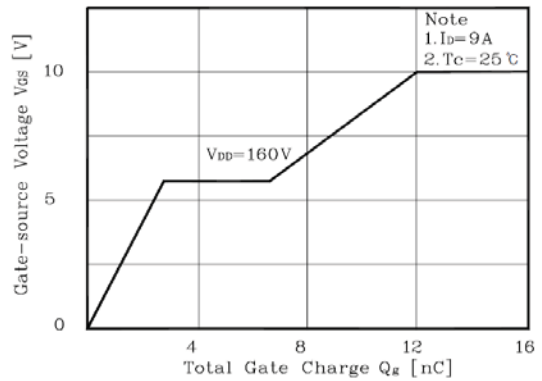


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

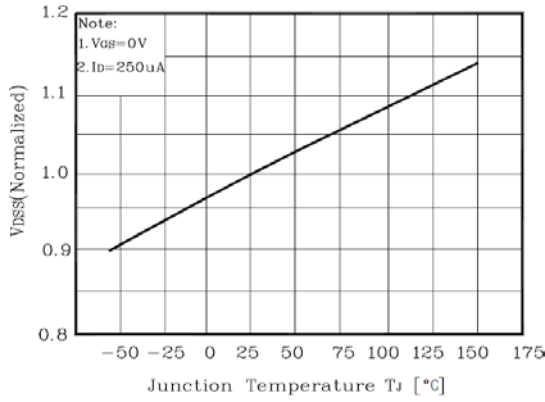


Figure 7. Breakdown Voltage Variation vs Temperature

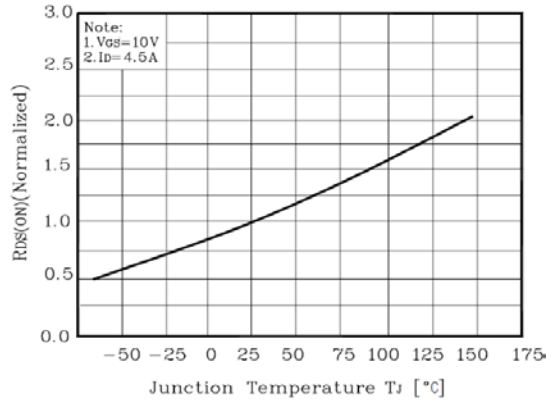


Figure 8. On-Resistance Variation vs Temperature

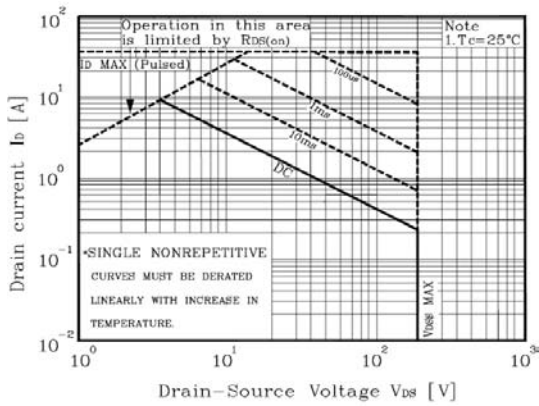


Figure 9. Maximum Safe Operating Area

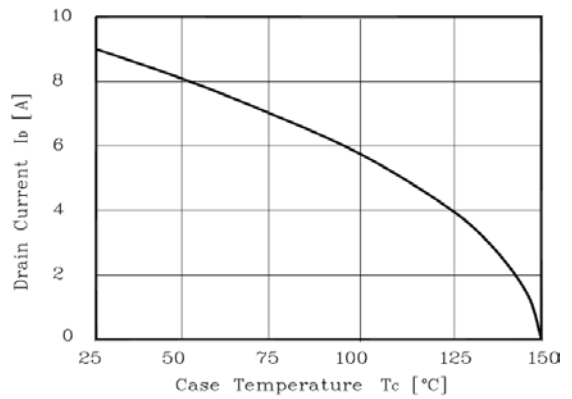


Figure 10. Maximum Drain Current vs Case Temperature

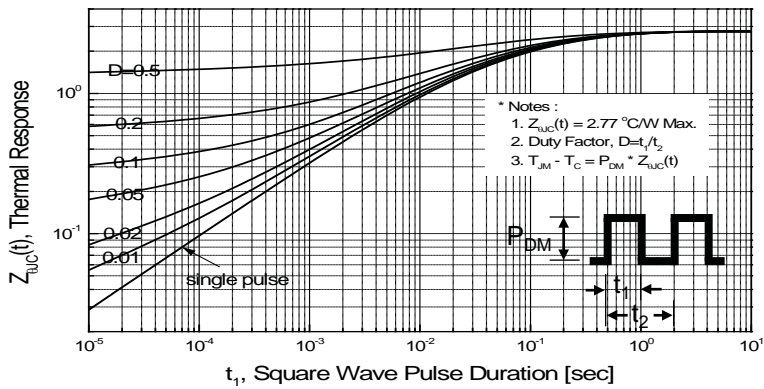


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

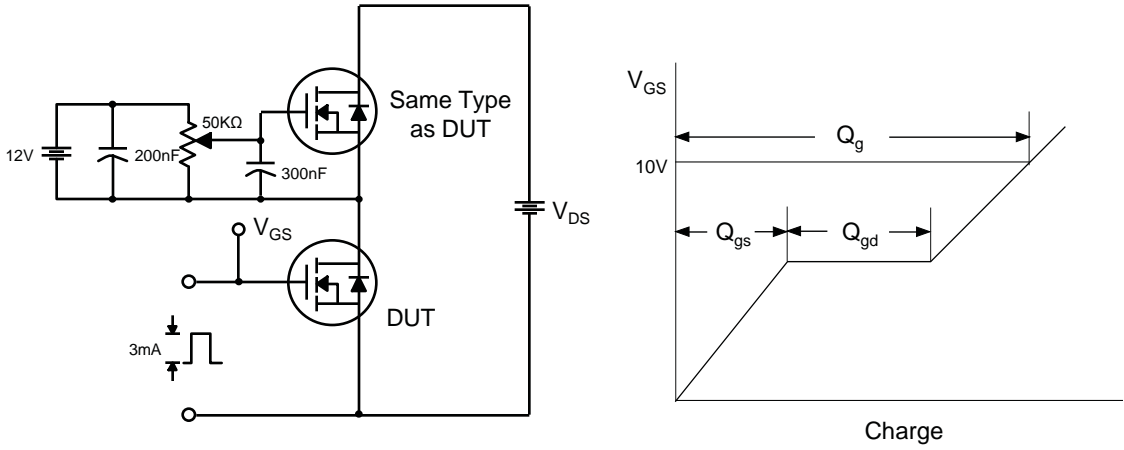


Fig 13. Resistive Switching Test Circuit & Waveforms

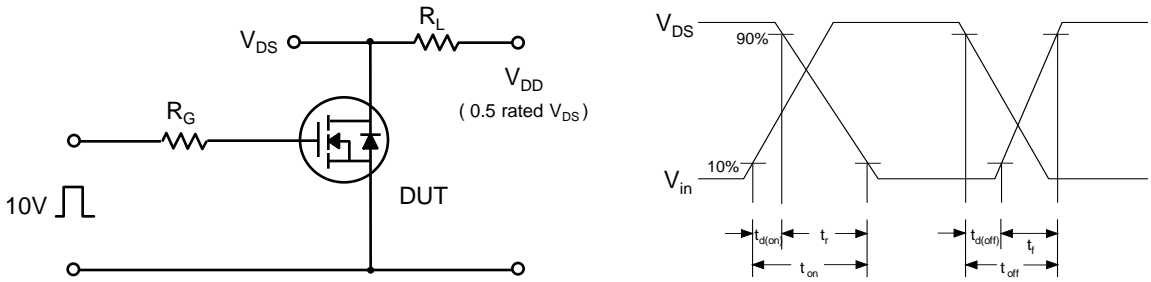


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

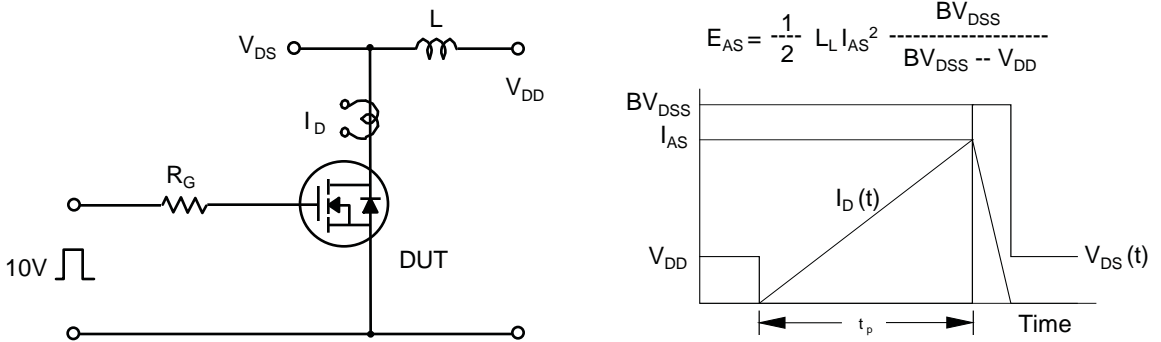
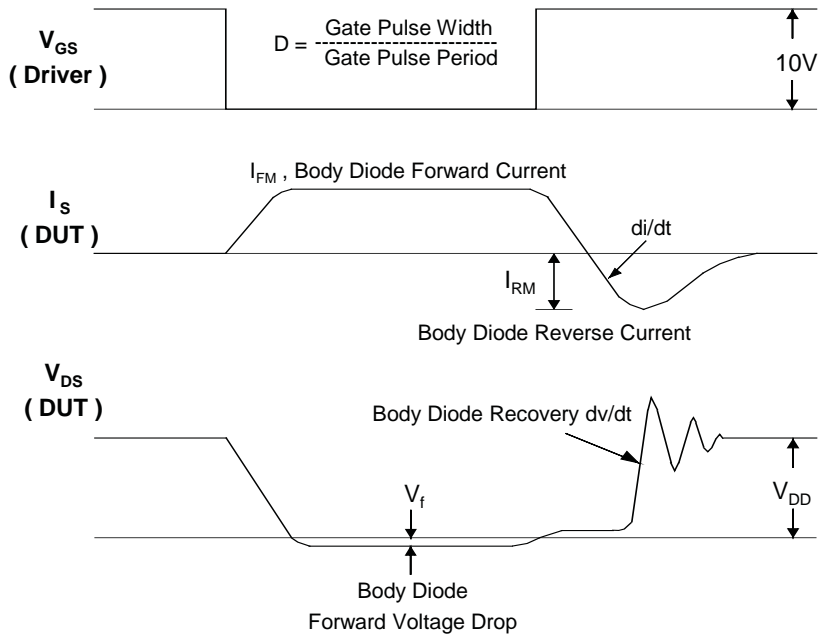
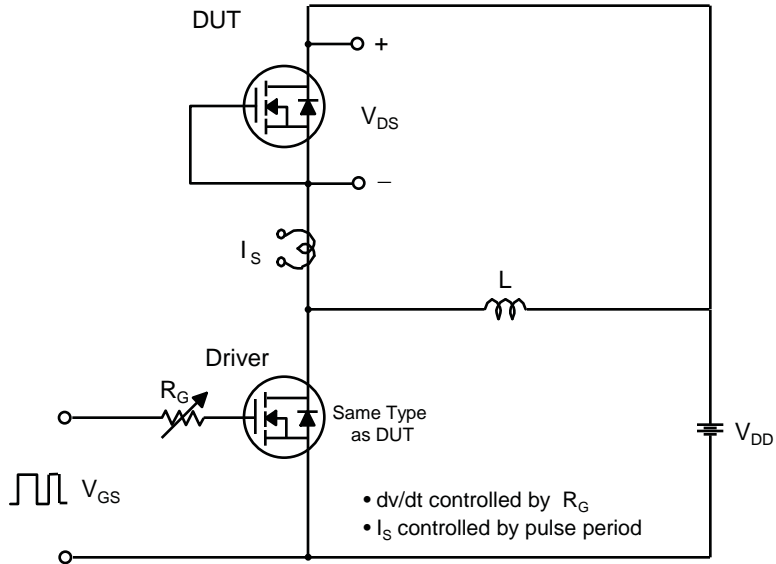
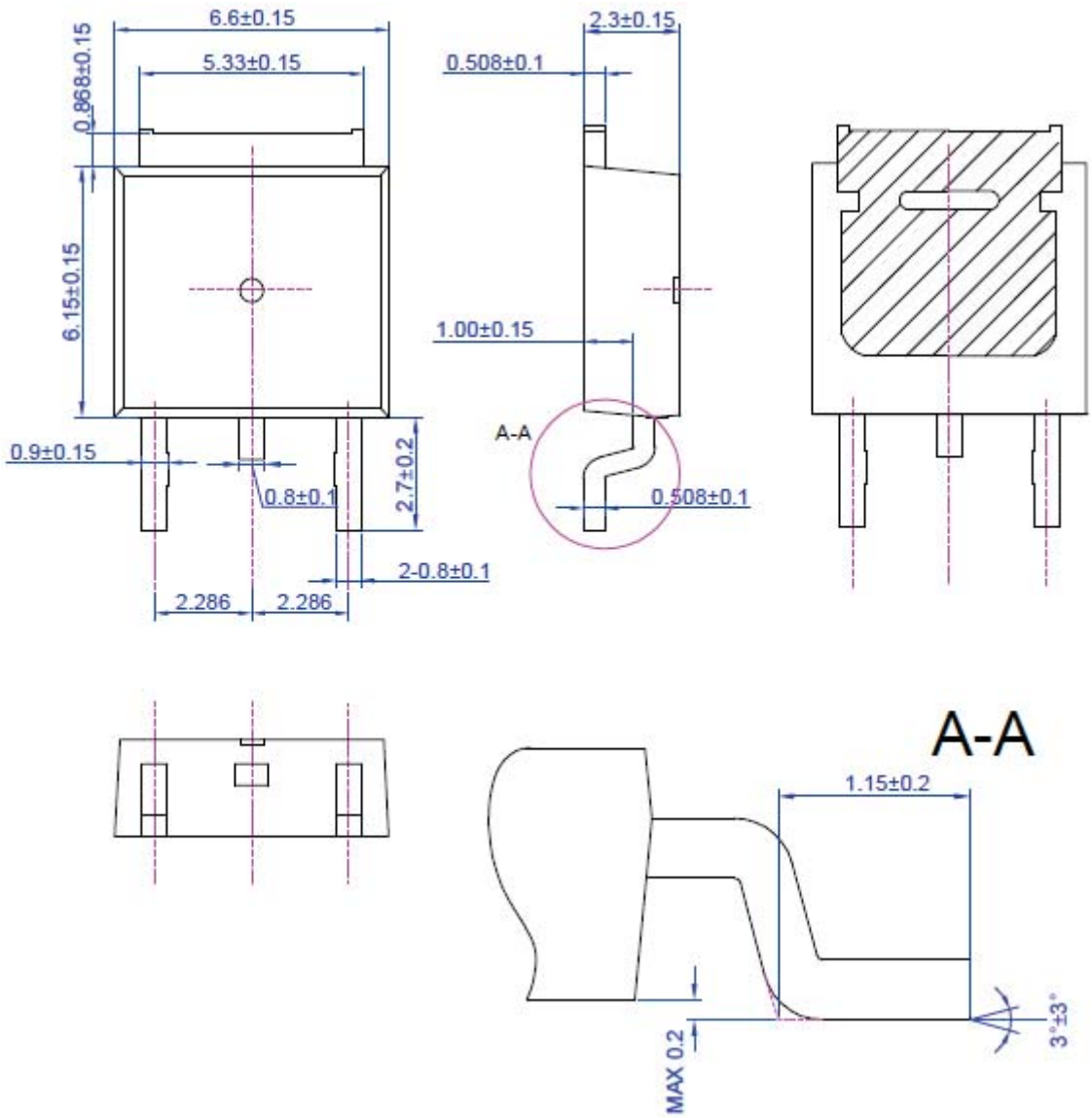


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

D-PAK
(TO-252A)



Package Dimension

I-PAK
(TO-251A)

