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# SGM800

## Low-Power, SOT $\mu$ P Reset Circuit with Capacitor-Adjustable Reset Timeout Delay

### GENERAL DESCRIPTION

The SGM800 low-power micro-processor supervisor circuit monitors system voltages from 1.6V to 5V. This device performs a single function: it asserts a reset signal whenever the  $V_{CC}$  supply voltage falls below its reset threshold. The reset output remains asserted for the reset timeout period after  $V_{CC}$  rises above the reset threshold. The reset timeout is externally set by a capacitor to provide more flexibility.

The SGM800 has an active-low, open-drain reset output. It is available in Green SOT-23-5 package and is specified over an ambient temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

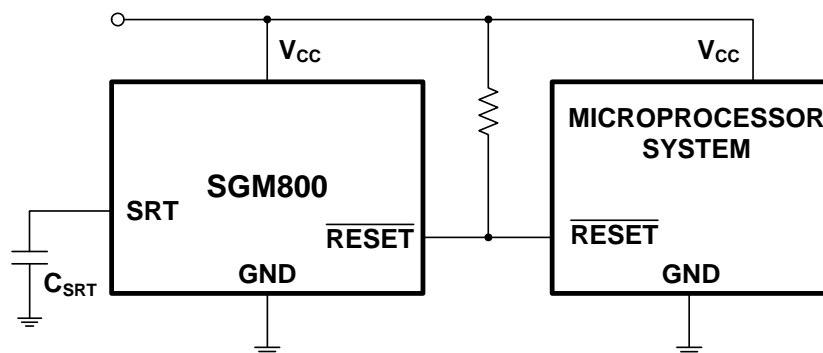
### FEATURES

- Monitor System Voltages from 1.6V to 5V
- Capacitor-Adjustable Reset Timeout Period
- Low Quiescent Current ( $3\mu\text{A}$  TYP)
- Open-Drain  $\overline{\text{RESET}}$  Output Option
- Guaranteed  $\overline{\text{RESET}}$  Valid to  $V_{CC} = 1\text{V}$
- Immune to Short  $V_{CC}$  Transients
- Available in Green SOT-23-5 Package

### APPLICATIONS

Portable Equipment  
Battery-Powered Computers/Controllers  
Automotive  
Medical Equipment  
Intelligent Instruments  
Embedded Controllers  
Critical  $\mu\text{P}$  Monitoring  
Set-Top Boxes  
Computers

### TYPICAL APPLICATION



# SGM800

# Low-Power, SOT $\mu$ P Reset Circuit with Capacitor-Adjustable Reset Timeout Delay

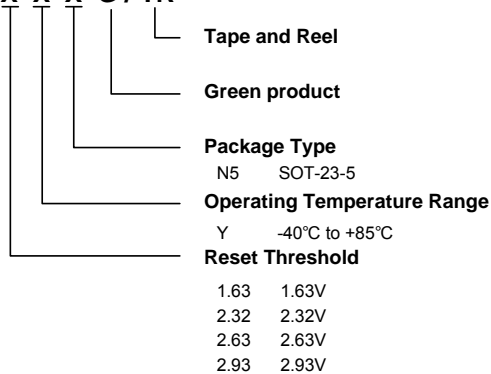
## PACKAGE/ORDERING INFORMATION

MODEL	PIN-PACKAGE	RESET THRESHOLD (TYP)	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM800	SOT-23-5	1.63V	SGM800-1.63YN5G/TR	S69XX	Tape and Reel, 3000
		2.32V	SGM800-2.32YN5G/TR	S6AXX	Tape and Reel, 3000
		2.63V	SGM800-2.63YN5G/TR	S6BXX	Tape and Reel, 3000
		2.93V	SGM800-2.93YN5G/TR	S6CXX	Tape and Reel, 3000

NOTE: Order number and package marking are defined as the follow:

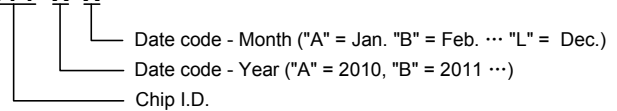
### ORDER NUMBER

SGM800 - X X X G / TR



### MARKING INFORMATION

SYX X X



For example: S69BA (2011, January)

## ABSOLUTE MAXIMUM RATINGS

All Voltages Referenced to GND

$V_{CC}$ .....	-0.3V to 6V
RESET (open-drain).....	-0.3V to 6V
Input Current (all pins).....	20mA
Output Current (RESET) .....	20mA
Operating Temperature Range .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature.....	150°C
Lead Temperature (Soldering, 10s) .....	260°C
ESD Susceptibility	
HBM.....	3000V
MM.....	300V

NOTE:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

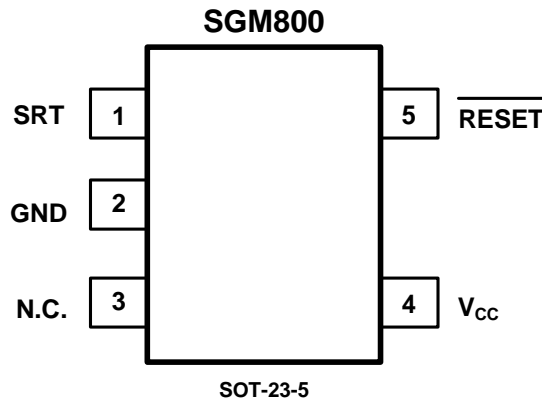
## CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the latest datasheet.



**PIN CONFIGURATION (TOP VIEW)**



**PIN DESCRIPTION**

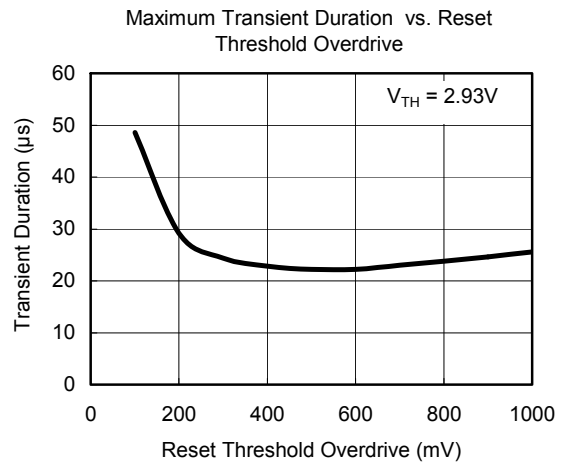
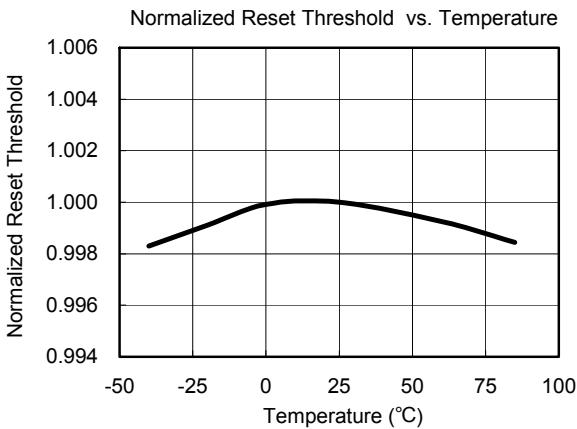
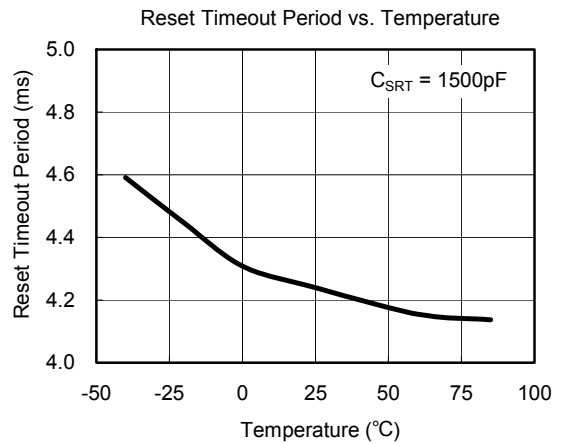
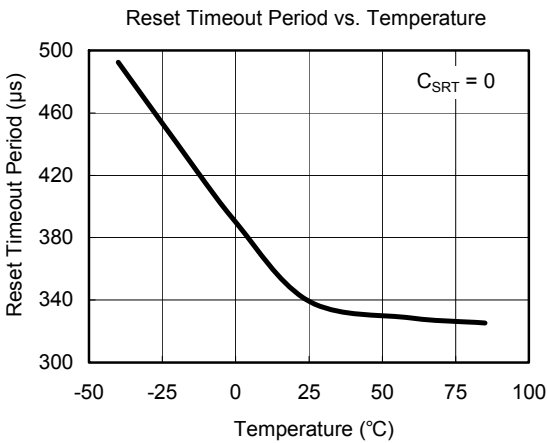
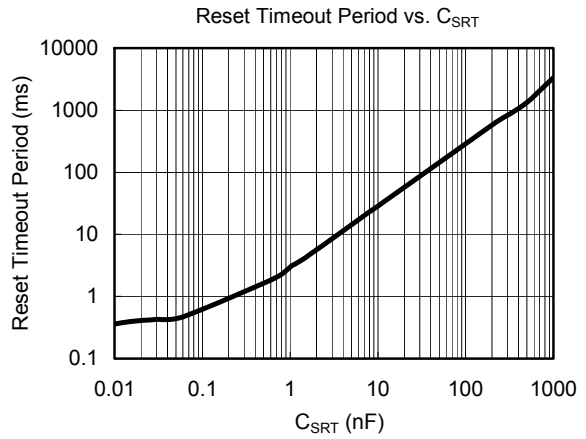
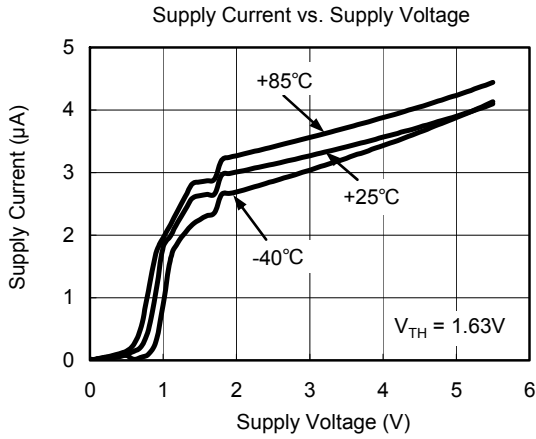
PIN	NAME	FUNCTION
1	SRT	Set Reset Timeout Input. Connect a capacitor between SRT and ground to set the timeout period. Determine the period as follows: $t_{RP} = 2.6 \times 10^6 \times C_{SRT} + 340 \times 10^{-6}$ with $t_{RP}$ in seconds and $C_{SRT}$ in farads.
2	GND	Ground.
3	N.C.	Not Internally Connected. Can be connected to GND.
4	$V_{CC}$	Supply Voltage and Reset Threshold Monitor Input.
5	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ changes from high to low whenever $V_{CC}$ drops below the selected reset threshold voltage. $\overline{\text{RESET}}$ remains low for the reset timeout period after $V_{CC}$ exceeds the reset threshold.

**ELECTRICAL CHARACTERISTICS**(V<sub>CC</sub> = 1V to 5.5V, T<sub>A</sub> = -40°C to +85°C, typical values are at V<sub>CC</sub> = 5V and T<sub>A</sub> = +25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V <sub>CC</sub>		1.0		5.5	V
Supply Current	I <sub>CC</sub>	V <sub>CC</sub> ≤ 5.0V		3.9	7.0	μA
		V <sub>CC</sub> ≤ 3.3V		3.4	5.5	
		V <sub>CC</sub> ≤ 2.0V		3.0	4.8	
V <sub>CC</sub> Reset Threshold Accuracy	V <sub>TH</sub>	T <sub>A</sub> = +25°C	V <sub>TH</sub> - 2.5%		V <sub>TH</sub> + 2.5%	V
		T <sub>A</sub> = -40°C to +85°C	V <sub>TH</sub> - 3.5%		V <sub>TH</sub> + 3.5%	
Hysteresis	V <sub>HYST</sub>			4 × V <sub>TH</sub>		mV
V <sub>CC</sub> to Reset Delay	t <sub>RD</sub>	V <sub>CC</sub> falling at 1mV/μs		80		μs
Reset Timeout Period	t <sub>RP</sub>	C <sub>SRT</sub> = 1500pF	3.00	4.25	5.75	ms
		C <sub>SRT</sub> = 0		0.34		
V <sub>SRT</sub> Ramp Current	I <sub>RAMP</sub>	V <sub>SRT</sub> = 0 to 0.65V, V <sub>CC</sub> = 1.6V to 5V		210		nA
V <sub>SRT</sub> Ramp Threshold	V <sub>TH-RAMP</sub>	V <sub>CC</sub> = 1.6V to 5V (V <sub>RAMP</sub> rising)		0.6		V
RESET Output Voltage Low	V <sub>OL</sub>	V <sub>CC</sub> ≥ 1.0V, I <sub>SINK</sub> = 50μA			0.3	V
		V <sub>CC</sub> ≥ 2.7V, I <sub>SINK</sub> = 1.2mA			0.3	
		V <sub>CC</sub> ≥ 4.5V, I <sub>SINK</sub> = 3.2mA			0.4	
RESET Output Leakage Current, Open-Drain	I <sub>LKG</sub>	V <sub>CC</sub> > V <sub>TH</sub> , reset not asserted			1	μA

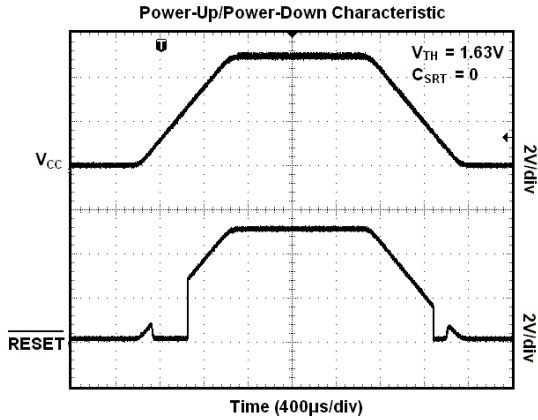
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 5V$ ,  $C_{SRT} = 1500pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 5V$ ,  $C_{SRT} = 1500pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



## DETAILED DESCRIPTION

### Reset Output

The reset output is typically connected to the reset input of a  $\mu$ P. A  $\mu$ P's reset input starts or restarts the  $\mu$ P in a known state. The SGM800  $\mu$ P supervisory circuit provides the reset logic to prevent code-execution errors during power-up, power-down, and brownout conditions.

$\overline{\text{RESET}}$  changes from high to low whenever  $V_{\text{CC}}$  drops below the threshold voltage. Once  $V_{\text{CC}}$  exceeds the threshold voltage,  $\overline{\text{RESET}}$  remains low for the capacitor-adjustable reset timeout period.

This device output is guaranteed valid for  $V_{\text{CC}} > 1\text{V}$ .

The SGM800 is open-drain  $\overline{\text{RESET}}$  output. Connect an external pull up resistor to any supply from 0 to 5.5V. Select a resistor value large enough to register a logic low when  $\overline{\text{RESET}}$  is asserted and small enough to register a logic high while supplying all input current and leakage paths connected to the  $\overline{\text{RESET}}$  line. A 10k $\Omega$  to 100k $\Omega$  pull up is sufficient in most applications.

### Selecting a Reset Capacitor

The reset timeout period is adjustable to accommodate a variety of  $\mu$ P applications. Adjust the reset timeout period ( $t_{\text{RP}}$ ) by connecting a capacitor ( $C_{\text{SRT}}$ ) between SRT and ground. Calculate the reset timeout capacitor as follows:

$$C_{\text{SRT}} = (t_{\text{RP}} - 340 \times 10^{-6}) / (2.6 \times 10^6)$$

where  $t_{\text{RP}}$  is in seconds and  $C_{\text{SRT}}$  is in farads.

The reset delay time is set by a current/capacitor-controlled ramp compared to an internal 0.6V reference. An internal 210nA ramp current source charges the external capacitor. The charge to the capacitor is cleared when a reset condition is detected. Once the reset condition is removed, the voltage on the capacitor ramps according to the formula:  $dV/dt = I/C$ . The  $C_{\text{SRT}}$  capacitor must ramp to 0.6V to deassert the reset.  $C_{\text{SRT}}$  must be a low-leakage (<10nA) type capacitor; ceramic is recommended.

### Operating as a Voltage Detector

The SGM800 can be operated in a voltage detector mode by floating the SRT pin. The reset delay times for  $V_{\text{CC}}$  rising above or falling below the threshold are not significantly different. The reset output is deasserted smoothly without false pulses.



APPLICATION INFORMATION

Interfacing to Other Voltages for Logic Compatibility

The open-drain output of the SGM800 can be used to interface to  $\mu$ Ps with other logic levels. As shown in Figure 1, the open-drain output can be connected to voltages from 0 to 5.5V. This allows for easy logic compatibility to various  $\mu$ Ps.

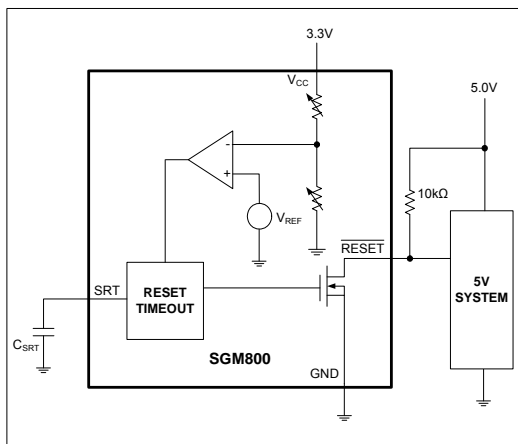


Figure 1. Open-Drain  $\overline{\text{RESET}}$  Output Allows Use with Multiple Supplies

Negative-Going  $V_{CC}$  Transients

In addition to issuing a reset to the  $\mu$ P during power-up, power-down, and brownout conditions, this supervisor is relatively immune to short-duration negative-going transients (glitches). The graph Maximum Transient Duration vs. Reset Threshold Overdrive in the Typical Performance Characteristics shows this relationship.

The area below the curve of the graph is the region in which these devices typically do not generate a reset pulse. This graph was generated using a negative-going pulse applied to  $V_{CC}$ , starting above the actual reset threshold ( $V_{TH}$ ) and ending below it by the magnitude indicated (reset-threshold overdrive). As the magnitude of the transient decreases (further below the reset threshold), the maximum allowable pulse width-decreases. Typically, a  $V_{CC}$  transient that goes 100mV below the reset threshold and lasts 50 $\mu$ s or less does not cause a reset pulse to be issued.

Wired-OR Reset

To allow auxiliary circuitry to hold the system in reset, an external open-drain logic signal can be connected to the open-drain  $\overline{\text{RESET}}$  of the SGM800, as shown in Figure 2. This configuration can reset the  $\mu$ P, but does not provide the reset timeout when the external logic signal is released.

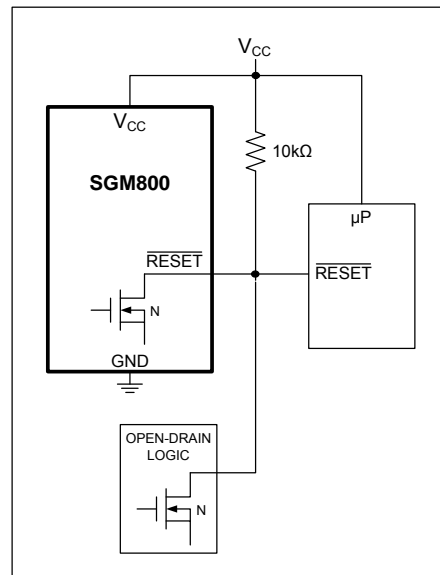


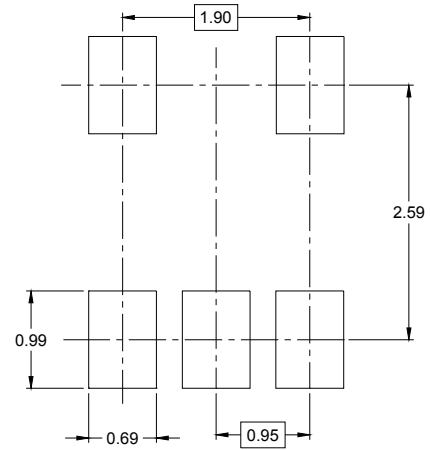
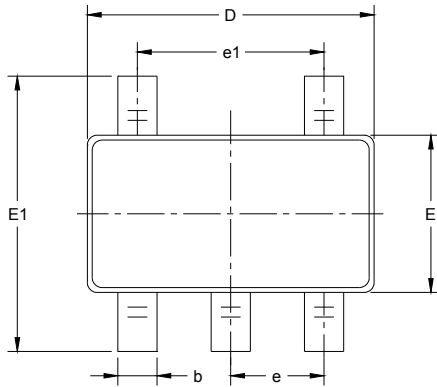
Figure 2. Wired-OR Reset Circuit

Layout Consideration

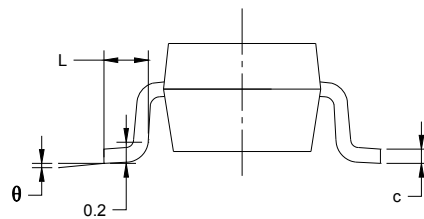
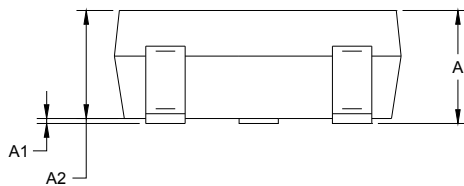
SRT is a precise current source. When developing the layout for the application, be careful to minimize board capacitance and leakage currents around this pin. Traces connected to SRT should be kept as short as possible. Traces carrying high-speed digital signals and traces with large voltage potentials should be routed as far from SRT as possible. Leakage current and stray capacitance (e.g., a scope probe) at this pin could cause errors in the reset timeout period. When evaluating these parts, use clean prototype boards to ensure accurate reset periods.

PACKAGE OUTLINE DIMENSIONS

SOT-23-5



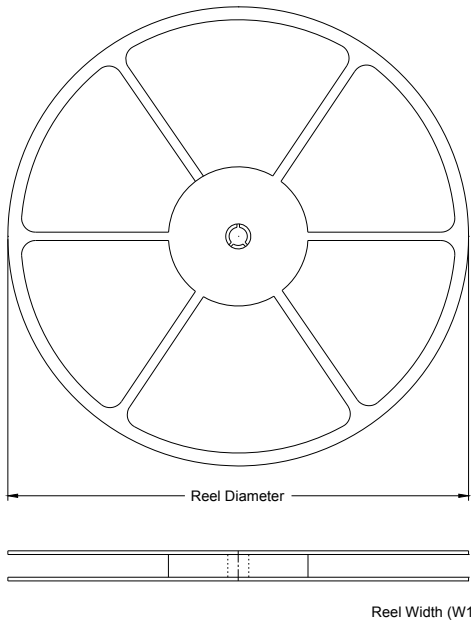
RECOMMENDED LAND PATTERN (Unit: mm)



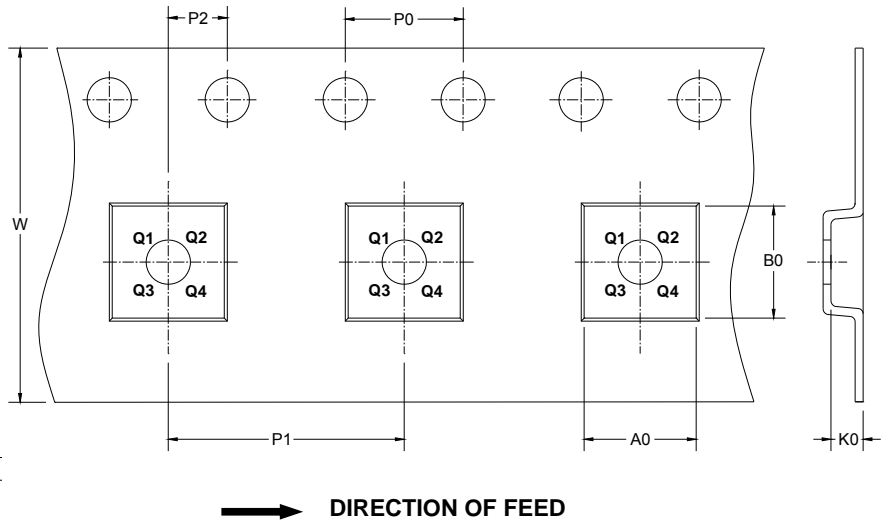
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
$\theta$	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



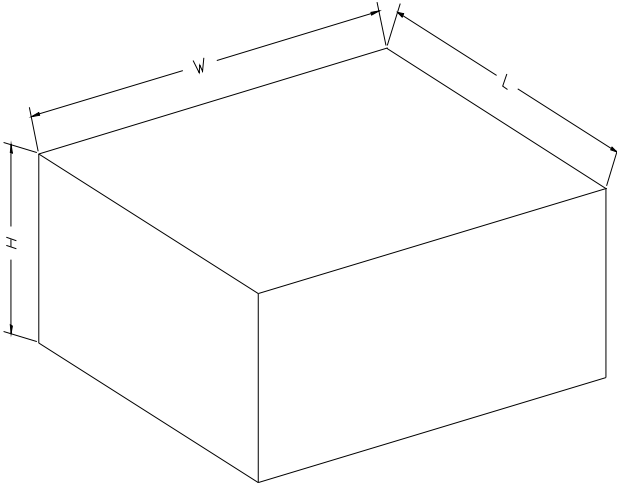
TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7"	9.5	3.2	3.2	1.4	4.0	4.0	2.0	8.0	Q3

**CARTON BOX DIMENSIONS**

NOTE: The picture is only for reference. Please make the object as the standard.

**KEY PARAMETER LIST OF CARTON BOX**

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18