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### Features

- **LOW OFFSET VOLTAGE:** 10 µV (Max)
- **ZERO DRIFT:** 0.008 µV/°C
- **0.1Hz to 10Hz Noise:** 1.1 µV<sub>PP</sub>
- **Low Supply Current:** 34 µA per Amplifier
- **Bandwidth:** 350 kHz
- **Slew Rate:** 0.16 V/µs
- **High Gain, 130 dB High CMRR and PSRR**
- **Rail-to-rail Input and Output Swing**
- **-40°C to 125°C Operation Range**
- **Small Packages:** SC70 and SOT23 (TP5531)

### Applications

- Transducer Amplifier
- Bidirectional Current Sense
- DC Offset Correction
- Temperature Measurement
- Remote Located Sensors
- Battery-Powered Instruments
- Electronic Weigh Scales

### Description

The 3PEAK TP5531/2/4 low-power chopper stabilized operational amplifiers provide input offset voltage correction for very low offset and offset drift over time and temperature. The devices operate with a single supply voltage as low as 1.8V, while drawing 34µA per amplifier of quiescent current with a gain bandwidth product of 350kHz. They are unity gain stable, have no 1/f noise, have good Power Supply Rejection Ratio (PSRR) and Common Mode Rejection Ratio (CMRR), and feature rail-to-rail input and output swing.

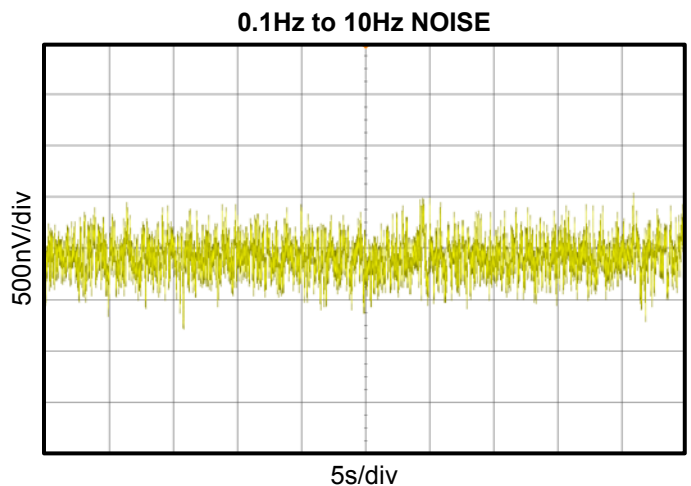
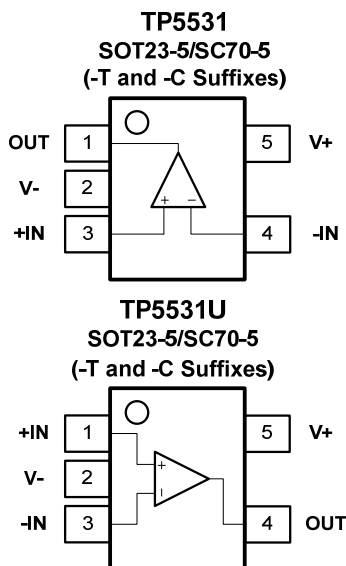
The devices were designed using an advanced CMOS process. The TP5531 (single version) is available in SC70-5, SOT23-5 and SO-8 packages. The TP5532 (dual version) is offered in MSOP-8 and SO-8 package. The TP5534 (quad version) is available in TSSOP-14 and SOIC-14 package. All versions are specified for operation from -40°C to 125°C.

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### Related Zero-Drift Op-amps

V <sub>os</sub> (Max.)	10 µV	5 µV	5 µV
<b>GBWP</b>	350 kHz	1.5 MHz	3.5 MHz
<b>Supply Current</b>	34 µA	220 µA	500 µA
<b>e<sub>n</sub> at 1 kHz</b>	55 nV/√Hz	25 nV/√Hz	15 nV/√Hz
<b>Single</b>	TP5531	TP5541	TP5551
<b>Dual</b>	TP5532	TP5542	TP5552
<b>Quad</b>	TP5534	TP5544	TP5554

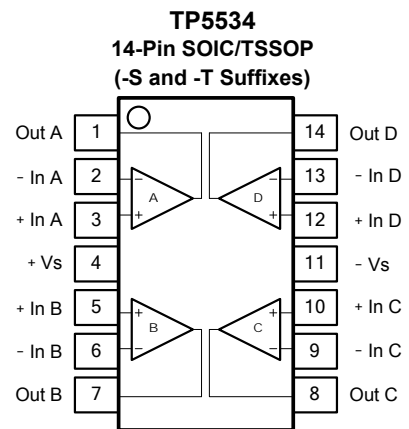
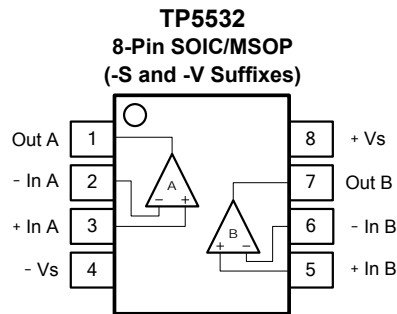
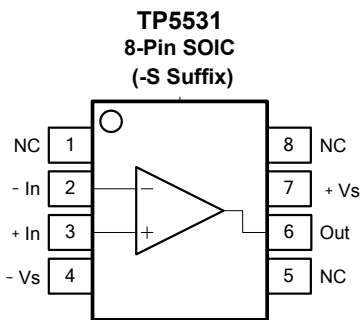
### Pin Configuration (Top View)



# TP5531 / TP5532 / TP5534

1.8V, 34µA, RRIO, Zero Drift Op-amps

## Pin Configuration (Top View, continued)



## Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP5531	TP5531-TR	SOT23-5	Tape and Reel, 3,000	E31T
	TP5531-CR	SC70-5 (SOT353)	Tape and Reel, 3,000	E31C
	TP5531-SR	SOIC-8	Tape and Reel, 4,000	E31S
TP5531U	TP5531U-TR	SOT23-5	Tape and Reel, 3,000	E31U
	TP5531U-CR	SC70-5	Tape and Reel, 3,000	E31V
TP5532	TP5532-SR	SOIC-8	Tape and Reel, 4,000	E32S
	TP5532-VR	MSOP-8	Tape and Reel, 3,000	E32V
TP5534	TP5534-SR	SOIC-14	Tape and Reel, 2,500	E34S
	TP5534-TR	TSSOP-14	Tape and Reel, 3,000	E34T

## Absolute Maximum Ratings Note 1

Supply Voltage: .....6V  
 Input Voltage: .....  $V^- - 0.2$  to  $V^+ + 0.2$   
 Input Current: +IN, -IN Note 2 .....  $\pm 20$ mA  
 Output Current: OUT .....  $\pm 60$ mA  
 Output Short-Circuit Duration Note 3 ..... Indefinite

Current at Supply Pins .....  $\pm 50$ mA  
 Operating Temperature Range .....  $-40^\circ\text{C}$  to  $125^\circ\text{C}$   
 Maximum Junction Temperature .....  $150^\circ\text{C}$   
 Storage Temperature Range .....  $-65^\circ\text{C}$  to  $150^\circ\text{C}$   
 Lead Temperature (Soldering, 10 sec) .....  $260^\circ\text{C}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

**Note 3:** A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

**ESD, Electrostatic Discharge Protection**

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	7	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

**Electrical Characteristics**

The boldface denotes the specifications which apply over the full operating temperature range, T<sub>A</sub> = -40°C to +125°C.

At T<sub>A</sub> = 27°C, V<sub>DD</sub> = 5V, R<sub>L</sub> = 10kΩ, V<sub>CM</sub> = V<sub>DD</sub>/2, unless otherwise noted.

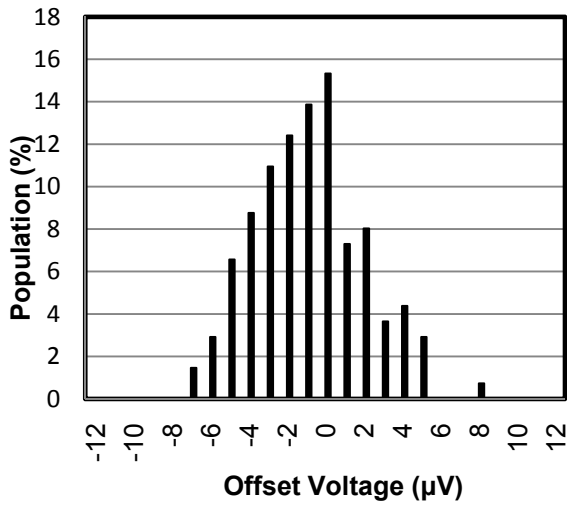
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V <sub>DD</sub>	Supply Voltage Range		1.8		5.5	V
I <sub>Q</sub>	Quiescent current per amplifier	I <sub>O</sub> = 0		34	40	µA
	<b>Over temperature</b>				<b>55</b>	<b>µA</b>
V <sub>OS</sub>	Input Offset Voltage	Input grounded, unity gain.		2	10	µV
dV <sub>OS</sub> /dT	vs temperature			<b>0.008</b>	<b>0.05</b>	<b>µV/°C</b>
PSRR	vs power supply	V <sub>S</sub> = +1.8V to +5.5V		<b>0.5</b>		<b>µV/V</b>
V <sub>n</sub>	input voltage noise, f=0.01Hz to 1Hz			0.4		µV <sub>pp</sub>
	input voltage noise, f=0.1Hz to 10Hz			1.1		µV <sub>pp</sub>
e <sub>n</sub>	Input voltage noise density, f=1kHz			55		nV/√Hz
C <sub>IN</sub>	Input capacitor, Differential			3		pF
	Input capacitor, Common-Mode			2		pF
I <sub>B</sub>	Input Bias Current			±50	±200	pA
	<b>Over temperature</b>				<b>800</b>	<b>pA</b>
I <sub>OS</sub>	Input offset current			±100	±400	pA
V <sub>CM</sub>	Common-mode voltage range		(V-) - 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio		<b>110</b>	<b>130</b>		<b>dB</b>
V <sub>O</sub>	Output Voltage Swing from rail	R <sub>L</sub> = 10kΩ		5	10	mV
	<b>Over temperature</b>	R <sub>L</sub> = 10kΩ			<b>10</b>	<b>mV</b>
I <sub>SC</sub>	Short-circuit current				±60	mA
C <sub>L</sub>	Maximum Capacitive Load			1,000		pF
GBWP	Unity Gain Bandwidth	C <sub>L</sub> = 100pF		350		kHz
SR	Slew rate	G = +1, C <sub>L</sub> = 100pF		0.16		V/µs
t <sub>OR</sub>	Overload recovery time	G = -10		60		µs
t <sub>S</sub>	Settling time to 0.01%	C <sub>L</sub> = 100pF		40		µs
A <sub>VOL</sub>	Open-Loop Voltage Gain	(V-) + 100mV < V <sub>O</sub> < (V+) - 100mV, R <sub>L</sub> = 100kΩ	<b>100</b>	<b>120</b>		<b>dB</b>
θ <sub>JA</sub>	Thermal Resistance Junction to Ambient	SC70-5 (SOT353)		250		°C/W
		SOT23-5		200		
		MSOP-8		210		
		SOIC-8		158		
		SOIC-14		83		
		TSSOP-14		100		

# TP5531 / TP5532 / TP5534

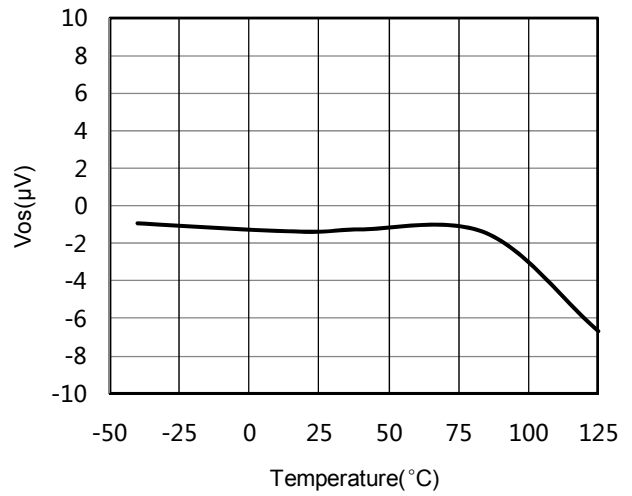
1.8V, 34 $\mu$ A, RRIO, Zero Drift Op-amps

## Typical Performance Characteristics

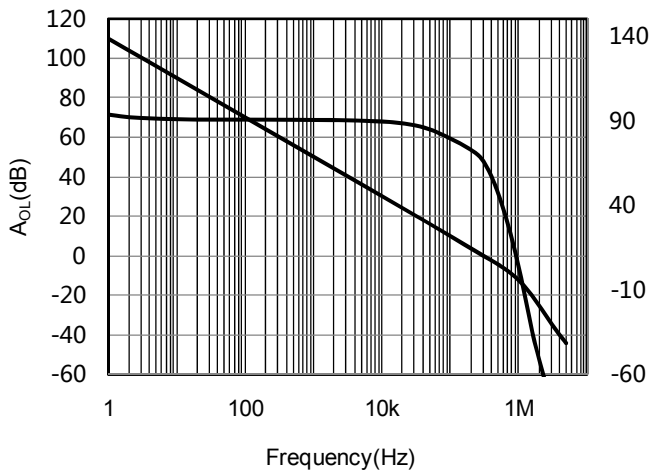
**Offset Voltage Distribution**



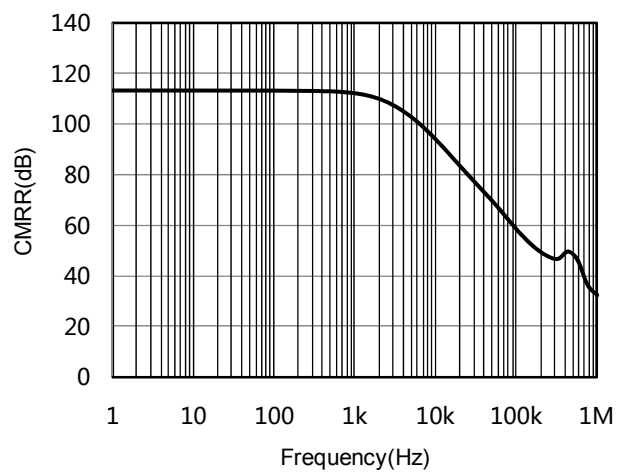
**Offset Voltage vs TEMPERATURE**



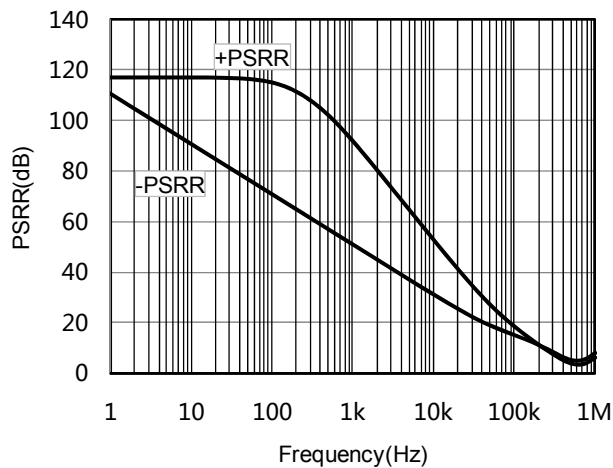
**OPEN-LOOP GAIN vs FREQUENCY**



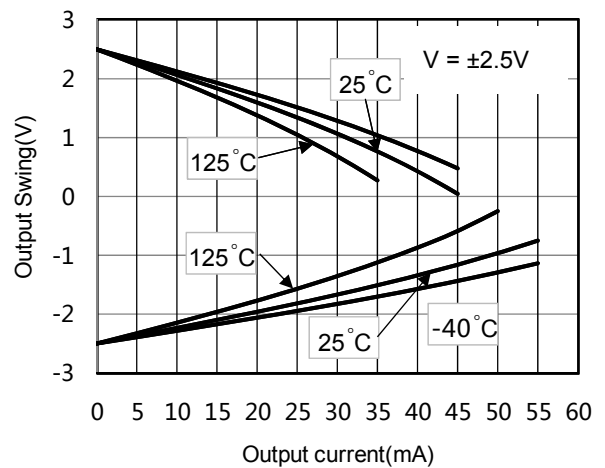
**CMRR vs FREQUENCY**



**PSRR vs FREQUENCY**

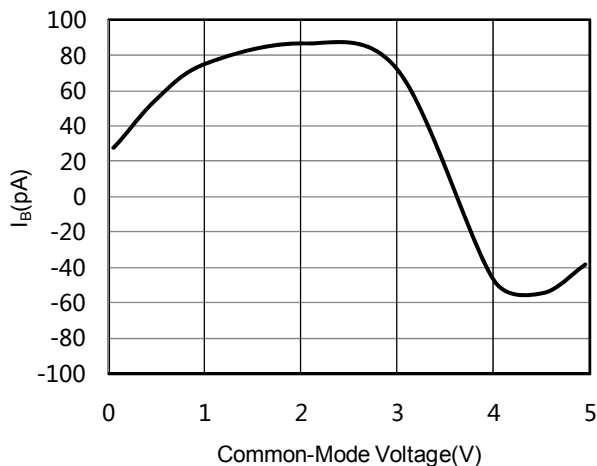


**OUTPUT SWING vs LOAD CURRENT**

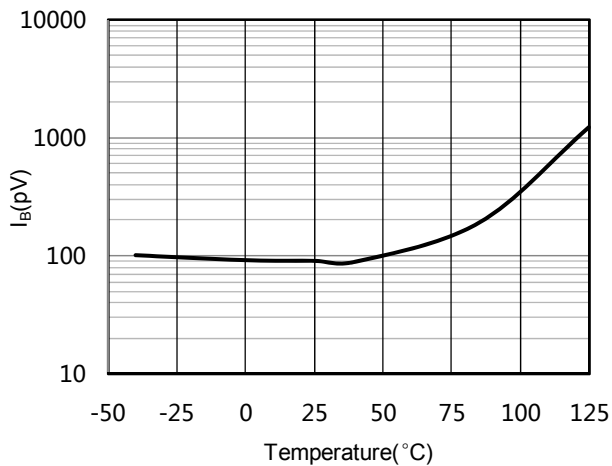


Typical Performance Characteristics(continue)

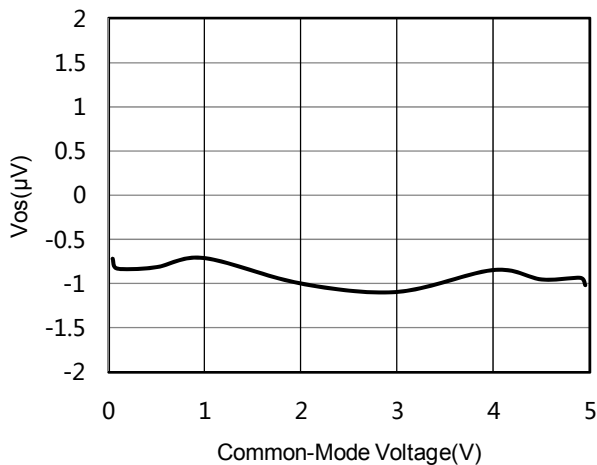
IB vs COMMON-MODE VOLTAGE



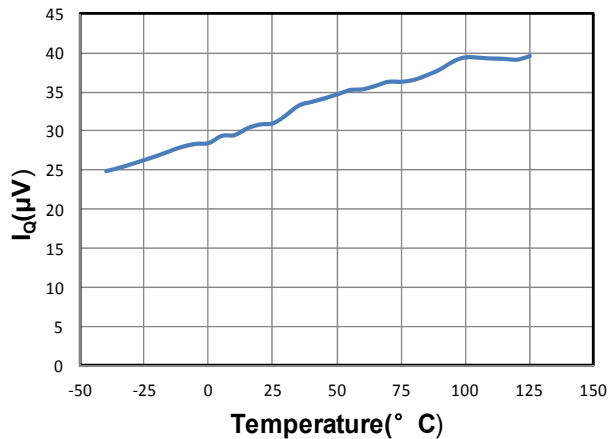
INPUT BIAS vs TEMPERATURE



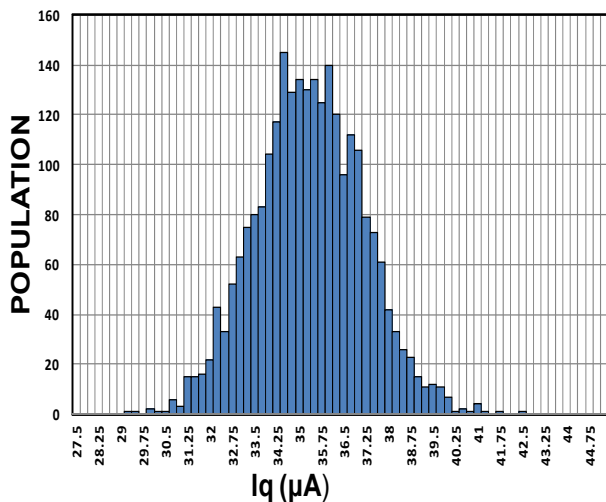
Vos vs COMMON-MODE VOLTAGE



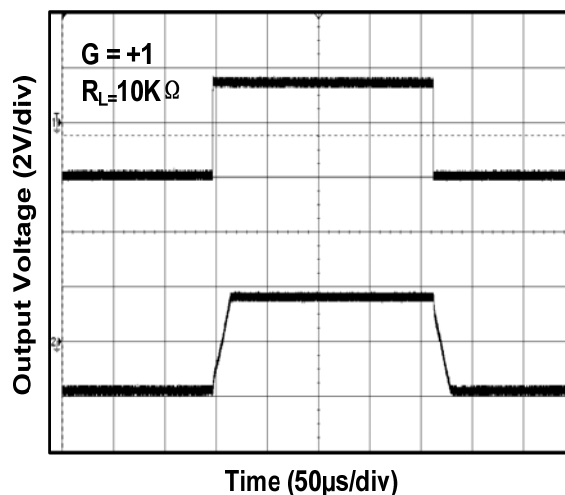
QUIESCENT CURRENT vs TEMPERATURE



Quiescent Current Distribution



Large-Scale Step Response

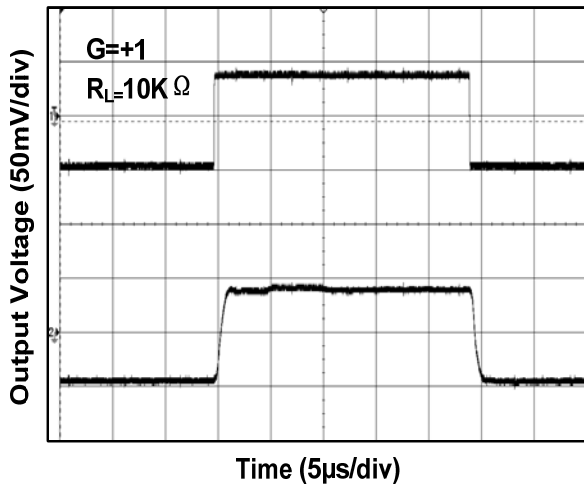


Typical Performance Characteristics(continue)

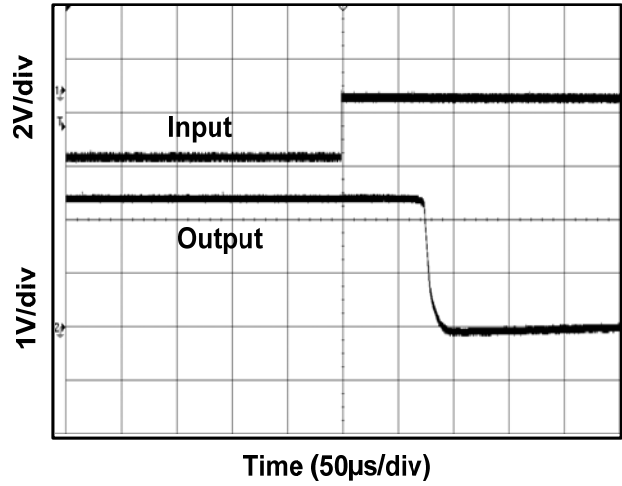
# TP5531 / TP5532 / TP5534

1.8V, 34 $\mu$ A, RRIO, Zero Drift Op-amps

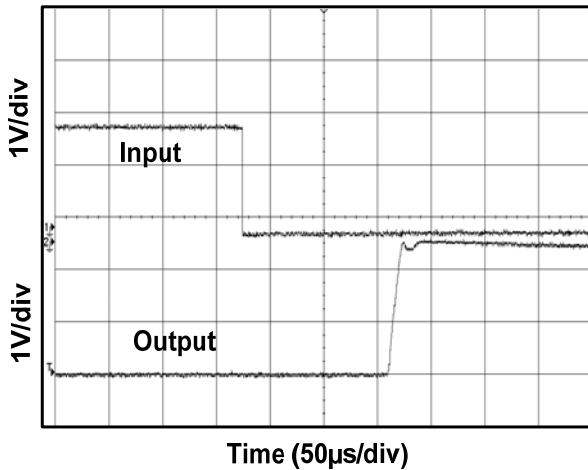
### Small-Scale Step Response



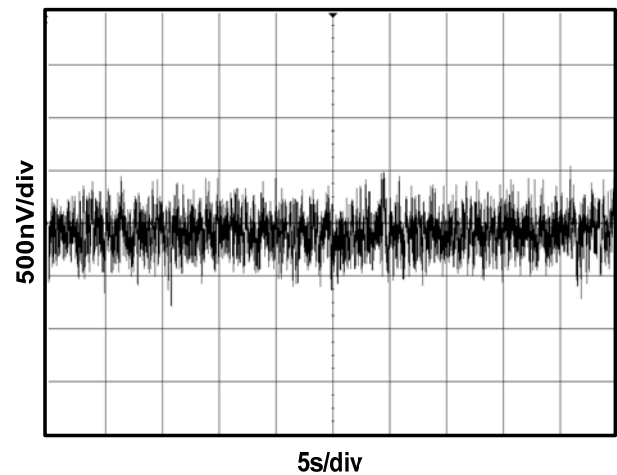
### Positive Over-Voltage Recovery



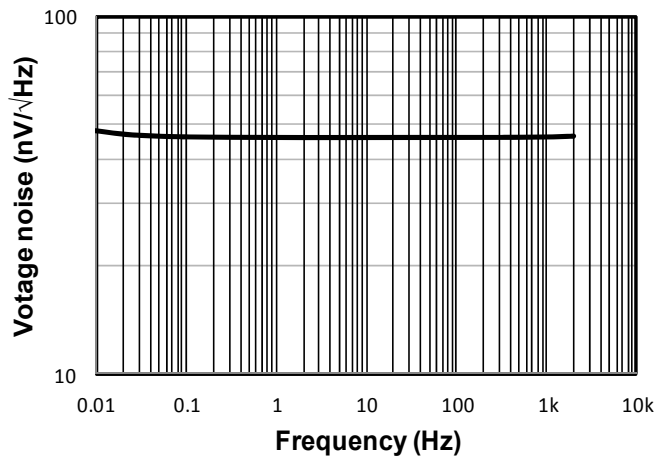
### Negative Over-Voltage Recovery



### 0.1Hz TO 10Hz NOISE

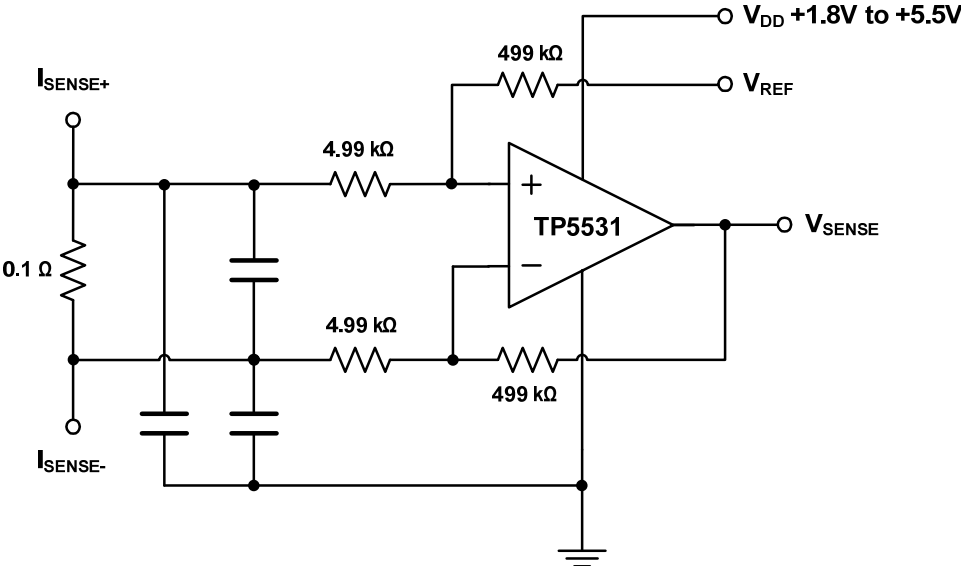


### VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

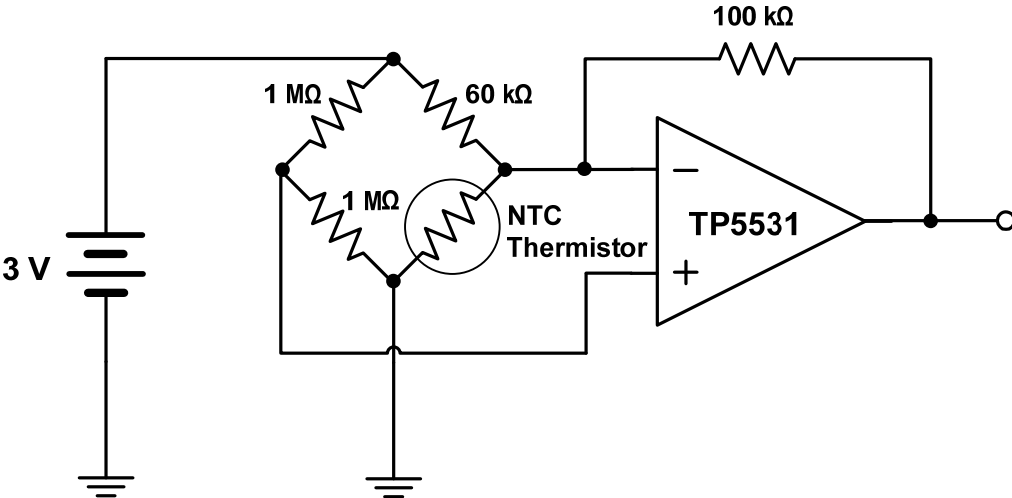


## Typical Applications

Bi-Directional Current Sense Amplifier



Thermistor Measurement





# TP5531 / TP5532 / TP5534

## 1.8V, 34 $\mu$ A, RRIO, Zero Drift Op-amps

### Pin Functions

**-IN:** Inverting Input of the Amplifier.

**+IN:** Non-Inverting Input of Amplifier.

**OUT:** Amplifier Output. The voltage range extends to within mV of each supply rail.

**V+ or +V<sub>s</sub>:** Positive Power Supply. Typically the voltage is from 1.8V to 5.5V. Split supplies are possible as long as the voltage between V+ and V- is between 1.8V and 5.5V. A bypass capacitor of 0.1 $\mu$ F as close to the part as

possible should be used between power supply pins or between supply pins and ground.

**V- or -V<sub>s</sub>:** Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V+ and V- is from 1.8V to 5.5V. If it is not connected to ground, bypass it with a capacitor of 0.1 $\mu$ F as close to the part as possible.

### Operation

The TP553x series op amps are zero drift, rail-to-rail operation amplifiers that can be run from a single-supply voltage. They use an auto-calibration technique with a time-continuous 350 kHz op amp in the signal path while consuming only 34  $\mu$ A of supply current per channel. This amplifier is zero-corrected with a 120 kHz clock. Upon power-up, the amplifier requires approximately 100  $\mu$ s to achieve specified V<sub>OS</sub> accuracy. This design has no aliasing or flicker noise.

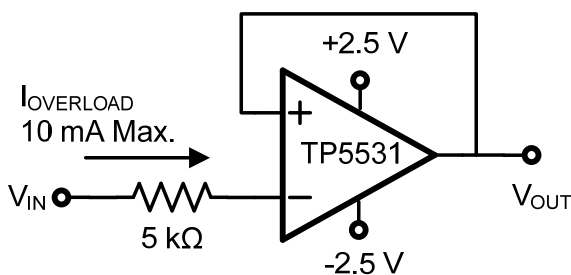
### Applications Information

#### Rail-To-Rail Input And Output

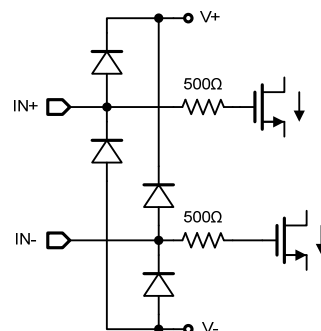
The TP553x series op amps feature rail-to-rail input and output with a supply voltage from 1.8V to 5.5 V. This allows the amplifier inputs to have a wide common mode range (50mV beyond supply rails) while maintaining high CMRR (130dB) and maximizes the signal to noise ratio of the amplifier by having the V<sub>OH</sub> and V<sub>OL</sub> levels be at the V+ and V- rails, respectively.

#### Input Protection

The TP553x series op amps have internal ESD protection diodes that are connect between the inputs and supply rail. When either input exceeds one of the supply rails by more than 300mV, the ESD diodes become forward biased and large amounts of current begin to flow through them. Without current limiting, this excessive fault current causes permanent damage to the device. Thus an external series resistor must be used to ensure the input currents never exceed 10mA.



Current-limiting resistor required if input voltage exceeds supply rails by >0.5V.



### Low Input Referred Noise

Flicker noise, as known as 1/f noise, is inherent in semiconductor devices and increases as frequency decreases. So at lower frequencies, flicker noise dominates, causing higher degrees of error for sub-Hertz frequencies or dc precision application.

The TP553x series amplifiers are chopper stabilized amplifiers, the flicker noise is reduced greatly because of this technique. This reduction in 1/f noise allows the TP553x to have much lower noise at dc and low frequency compared to standard low noise amplifier.

### Residual Voltage Ripple

The chopping technique can be used in amplifier design due to the internal notch filter. Although the chopping related voltage ripple is suppressed, higher noise spectrum exists at the chopping frequency and its harmonics due to residual ripple.

So if the frequency of input signal is nearby the chopping frequency, the signal maybe interfered by the residue ripple. To further suppress the noise at the chopping frequency, it is recommended that a post filter be placed at the output of the amplifier.

### Broad Band and External Resistor Noise Considerations

The total broadband noise output from any amplifier is primarily a function of three types of noise: input voltage noise from the amplifier, input current noise from the amplifier, and thermal (Johnson) noise from the external resistors used around the amplifier. These noise sources are not correlated with each other and their combined noise can be summed in a root sum squared manner. The full equation is given as:

$$e_n \text{ total} = [e_n^2 + 4kTR_s + (i_n \times R_s)^2]^{1/2}$$

Where:

$e_n$ = the input voltage noise density of the amplifier.

$i_n$ = the input current noise of the amplifier.

$R_s$ = source resistance connected to the noninverting terminal.

$k$ = Boltzmann’ s constant ( $1.38 \times 10^{-23}$  J/K).  $T$ = ambient temperature in Kelvin (K).

The total equivalent rms noise over a specific bandwidth is expressed as:

$$e_{n,rms} = e_n \text{ total} \times \sqrt{BW}$$

The input voltage noise density ( $e_n$ ) of the TP553x is 55 nV/√Hz, and the input current noise can be neglected. When the source resistance is 190 kΩ, the voltage noise contribution from the source resistor and the amplifier are equal. With source resistance greater than 190 kΩ, the overall noise of the system is dominated by the Johnson noise of the resistor itself.

### High Source Impedance Application

The TP553x series op amps use switches at the chopper amplifier input, the input signal is chopped at 125 kHz to reduce input offset voltage down to 10µV. The dynamic behavior of these switches induces a charge injection current to the input terminals of the amplifier. The charge injection current has a DC path to ground through the resistances seen at the input terminals of the amplifier. Higher input impedance causes an apparent shift in the input bias current of the amplifier.

Because the chopper amplifier has charge injection currents at each terminal, the input offset current will be larger than standard amplifiers. The  $I_{OS}$  of TP553x are 150pA under the typical condition. So the input impedance should be

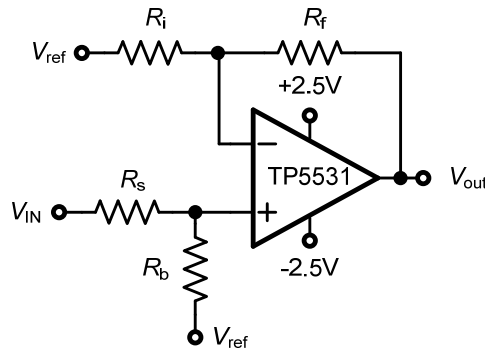
# TP5531 / TP5532/TP5534

## 1.8V, 34µA, RRIO, Zero Drift Op-amps

balanced across each input. The input impedance of the amplifier should be matched between the IN+ and IN- terminals to minimize total input offset current. Input offset currents show up as an additional output offset voltage, as shown in the following equation:

$$v_{os,total} = v_{os} - R_f \times I_{os}$$

For a gain configure using 1MΩ feedback resistor, a 150pA total input offset current will have an additional output offset voltage of 0.15mV. By keeping the input impedance low and balanced across the amplifier inputs, the input offset current effect will be suppressed efficiently.



Circuit Implication for reducing Input offset current effect

## PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

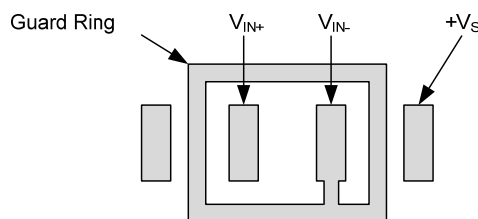
The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 2 for Inverting Gain application.

### 1. For Non-Inverting Gain and Unity-Gain Buffer:

- a) Connect the non-inverting pin ( $V_{IN+}$ ) to the input with a wire that does not touch the PCB surface.
- b) Connect the guard ring to the inverting input pin ( $V_{IN-}$ ). This biases the guard ring to the Common Mode input voltage.

### 2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

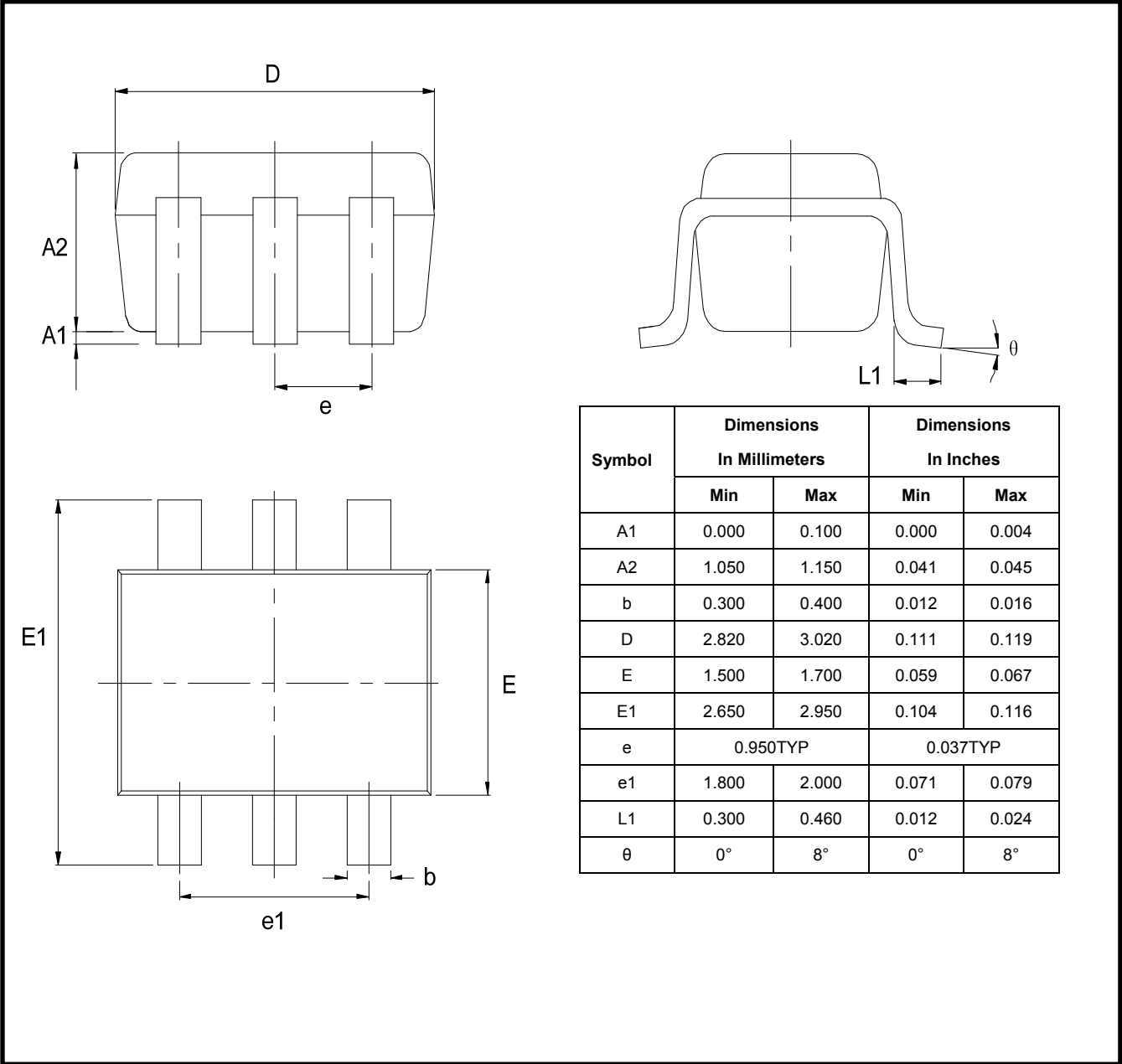
- a) Connect the guard ring to the non-inverting input pin ( $V_{IN+}$ ). This biases the guard ring to the same reference voltage as the op-amp (e.g.,  $V_{DD}/2$  or ground).
- b) Connect the inverting pin ( $V_{IN-}$ ) to the input with a wire that does not touch the PCB surface.



The Layout of Guard Ring

**Package Outline Dimensions**

SOT23-5 / SOT23-6



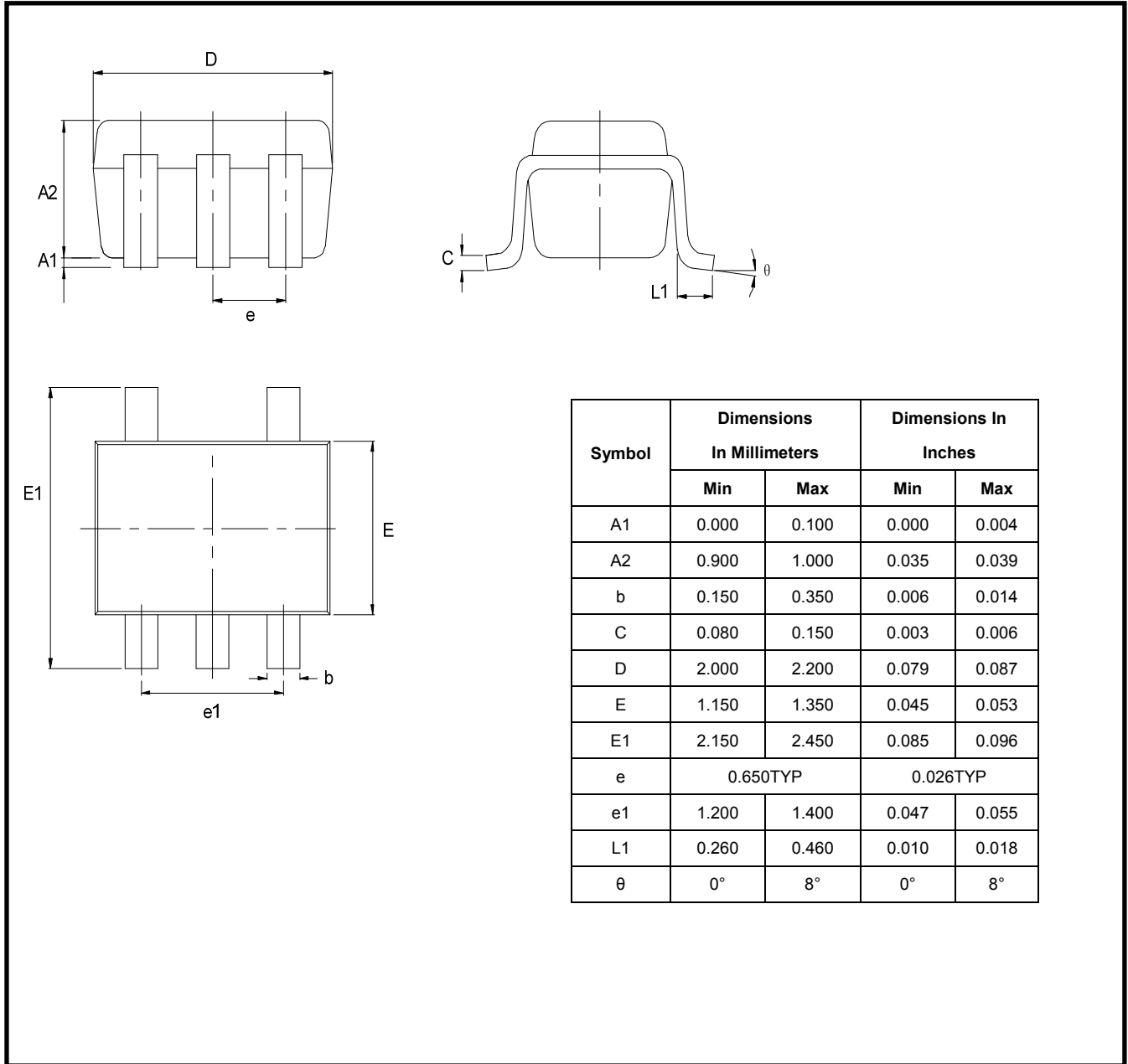
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L1	0.300	0.460	0.012	0.024
theta	0°	8°	0°	8°

# TP5531 / TP5532/TP5534

1.8V, 34 $\mu$ A, RRIO, Zero Drift Op-amps

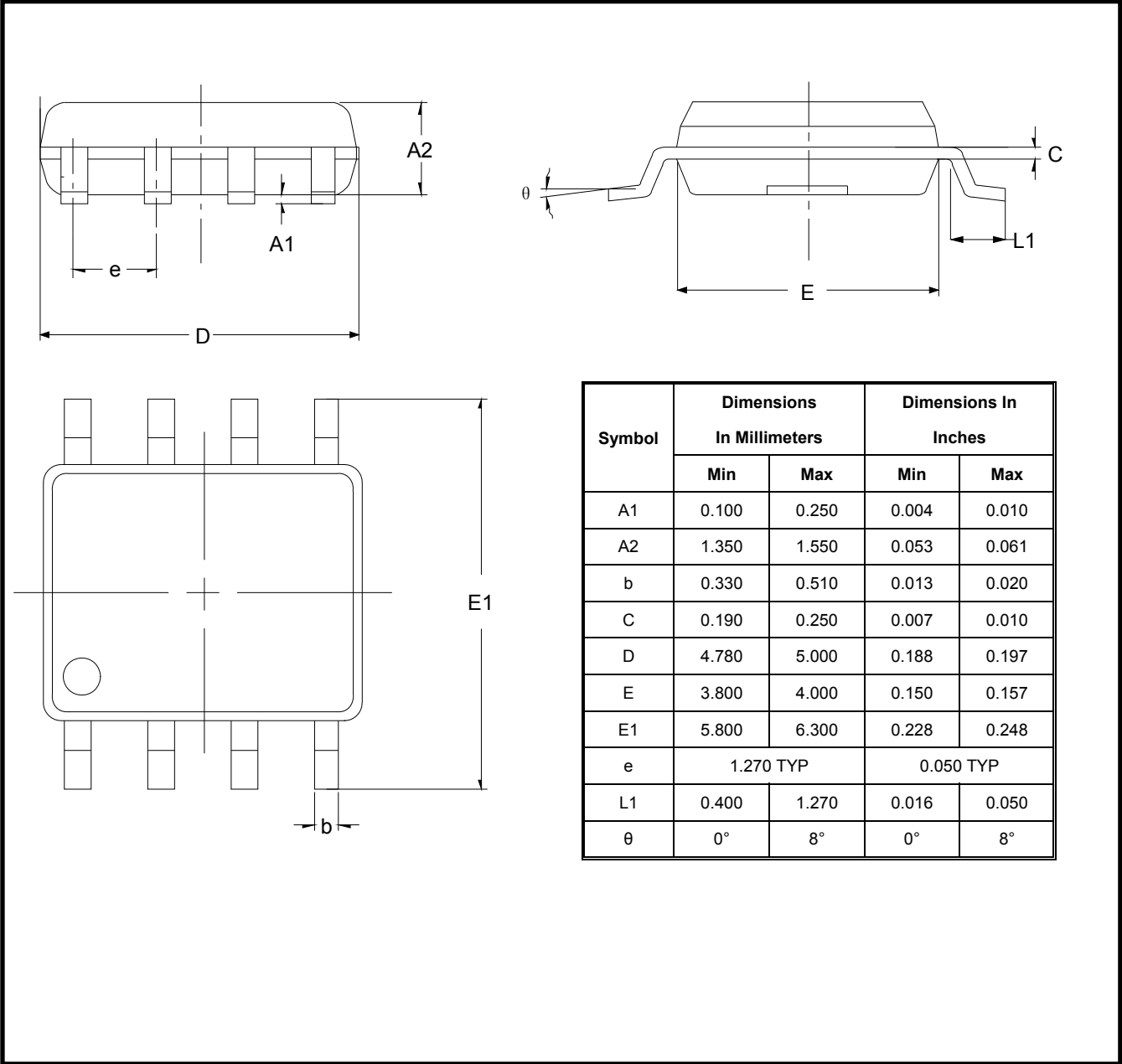
## Package Outline Dimensions

SC-70-5 (SOT353)



**Package Outline Dimensions**

SOP-8 (SOIC-8)

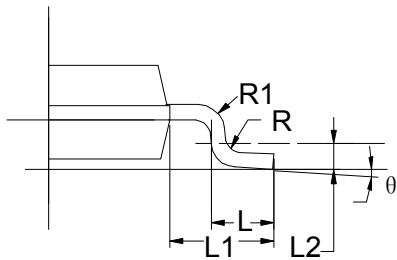
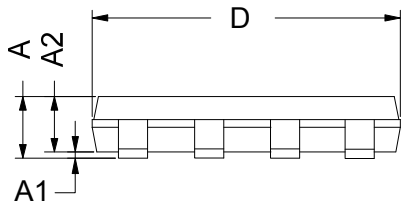
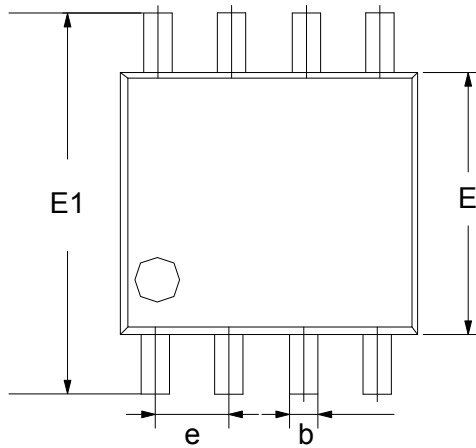


# TP5531 / TP5532 / TP5534

1.8V, 34 $\mu$ A, RRIO, Zero Drift Op-amps

## Package Outline Dimensions

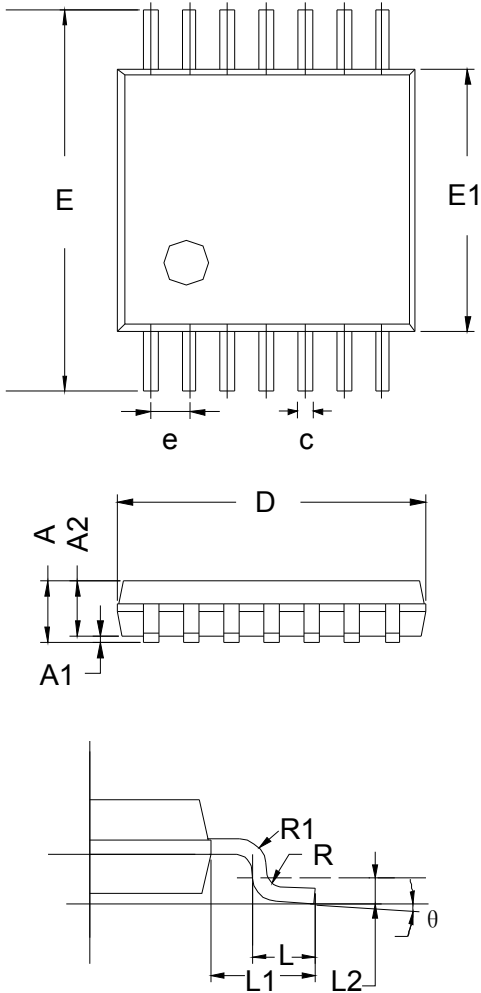
MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
$\theta$	0°	6°	0°	6°

Package Outline Dimensions

TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.20	-	0.28
c	0.10	-	0.19
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
theta	0°	-	8°

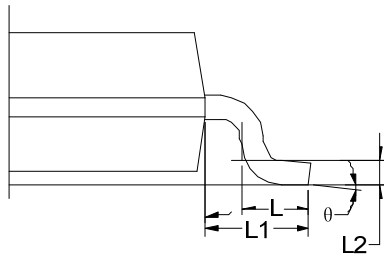
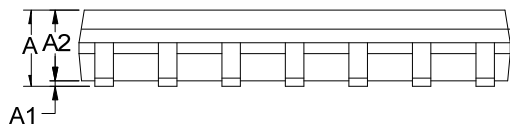
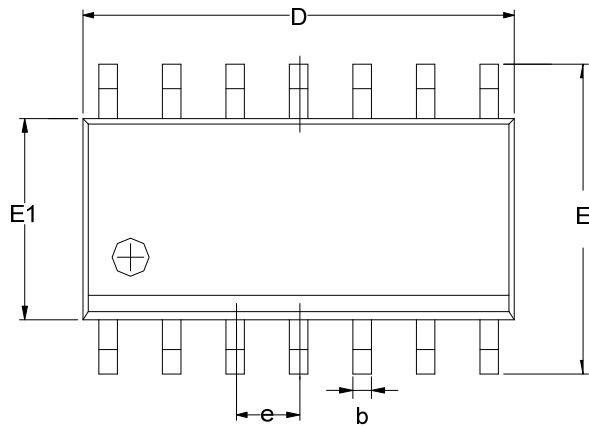


# TP5531 / TP5532 / TP5534

1.8V, 34 $\mu$ A, RRIO, Zero Drift Op-amps

## Package Outline Dimensions

SOP-14 (SOIC-14)



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.36		0.49
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
$\theta$	0°		8°