

## 阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

## Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

## Stereo 2.6W Audio Amplifier (With Gain Control)

### Features

- **Low Operating Current with 6mA**
- **Improved Depop Circuitry to Eliminate Turn-On Transients in Outputs**
- **High PSRR**
- **Internal Gain Control, Eliminate External Components**
- **2.6W per Channel Output Power into 3W Load at 5V, BTL Mode**
- **Multiple Input Modes Allowable Selected by HP/LINE Pin (APA2030)**
- **Two Output Modes Allowable with BTL and SE Modes Selected by SE/BTL Pin (for APA2030 only)**
- **Low Current Consumption in Shutdown Mode (50mA)**
- **Short Circuit Protection**
- **TSSOP-24P (APA2030) and TSSOP-20P (APA2031) with Thermal Pad Packages.**
- **Lead Free and Green Devices Available (RoHS Compliant)**

### Applications

- **Notebook PCs**
- **LCD Monitor**

### General Description

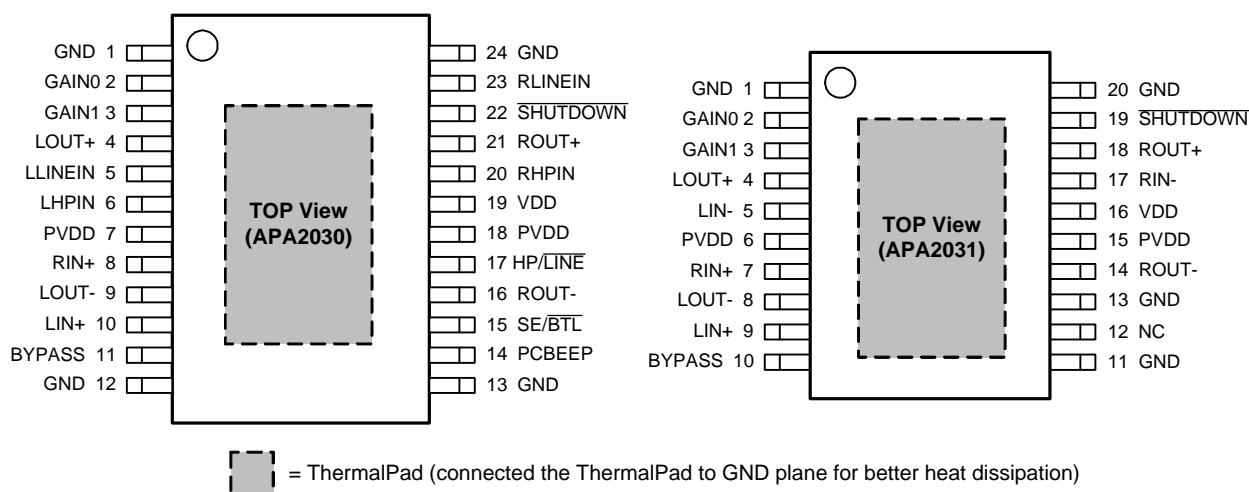
APA2030/1 is a monolithic integrated circuit, which provides internal gain control, and a stereo bridged audio power amplifiers capable of producing 2.6W (1.9W) into 3Ω with less than 10% (1.0%) THD+N. By controlling the two gain setting pins, Gain0 and Gain1, the amplifier can provide 6dB, 10dB, 15.6dB, and 21.6dB gain settings. The advantage of internal gain setting can be less components and PCB area. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in APA2030/1, that reduces pops and clicks noise during power up or shutdown mode operation. It also improves the power off pop noise and protects the chip from being destroyed by over temperature and short current failure. To simplify the audio system design, APA2030 combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/BTL input control pin signal. In addition, the multiple input selections are used for portable audio system. The APA2031 eliminates both input selection and single-end (SE) mode function to simplify the design and save the PCB space.

## Ordering and Marking Information

APA2030 APA2031	Assembly Material Handling Code Temperature Range Package Code	Package Code R : TSSOP-24P (APA2030) / TSSOP-20P (APA2031) Operating Ambient Temperature Range I : - 40 to 85 °C Handling Code TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APA2030 R :	APA2030 XXXXX	XXXXX - Date Code
APA2031 R :	APA2031 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Pin Configuration



## Absolute Maximum Ratings

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
	Supply Voltage Range, VDD, PVDD	-0.3V to 6V	V
	Input Voltage Range at SE/BTL, HP/LINE, SHUTDOWN,	-0.3V to V <sub>DD</sub>	V
T <sub>A</sub>	Operating Ambient Temperature Range	-40°C to 85°C	°C
T <sub>J</sub>	Maximum Junction Temperature	Internal Limited	
T <sub>STG</sub>	Storage Temperature Range	-65°C to 150°C	°C
T <sub>SDR</sub>	Maximum Lead Soldering Temperature, 10 Seconds	260°C	°C
P <sub>D</sub>	Power dissipation	Internal Limited	

## Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V <sub>DD</sub>	Supply Voltage	4.5V to 5.5V	V

## Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
R <sub>THJA</sub>	Thermal Resistance from Junction to Ambient in Free Air TSSOP-24P TSSOP-20P	45 48	°C/W

Note : \* 5 in<sup>2</sup> printed circuit board with 2oz trace and copper pad through 9 25mil diameter vias.

The thermal pad on the TSSOP\_P package with solder on the printed circuit board.

## Electrical Characteristics

(V<sub>DD</sub>=5V, -20°C<T<sub>A</sub><85°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	APA2030 / 2031			Unit
			Min.	Typ.	Max.	
V <sub>DD</sub>	Supply Voltage		3.3	-	5.5	V
I <sub>DD</sub>	Supply Current	SE/ $\overline{\text{BTL}}$ = 0V	-	6	12	mA
		SE/ $\overline{\text{BTL}}$ = 5V	-	4	8	mA
I <sub>SD</sub>	Supply Current in Shutdown Mode	SHUTDOWN = 0V	-	50	300	μA
V <sub>IH</sub>	High Level Threshold Voltage	SHUTDOWN, GAIN0, GAIN1	2	-	-	V
		SE/ $\overline{\text{BTL}}$ , HP/ $\overline{\text{LINE}}$	4	-	-	V
V <sub>IL</sub>	Low level Threshold Voltage	SHUTDOWN, GAIN0, GAIN1	-	-	0.8	V
		SE/ $\overline{\text{BTL}}$ , HP/ $\overline{\text{LINE}}$	-	-	3	V
I <sub>I</sub>	Input Current	SHUTDOWN, SE/ $\overline{\text{BTL}}$ , HP/ $\overline{\text{LINE}}$ , GAIN0, GAIN1	-	5	-	nA
V <sub>ICM</sub>	Common Mode Input Voltage		V <sub>DD</sub> -1.0	-	-	V
V <sub>OS</sub>	Output Differential Voltage		-	5	-	mV
	PC-BEEP Trigger Level		-	1	-	V <sub>p.p</sub>
R <sub>BYPASS</sub>	BYPASS Equivalent Resistance		-	250	-	kΩ

## Electrical Characteristics (Cont.)

### Operating Characteristics, BTL mode

$V_{DD}=5V$ ,  $T_A=25^\circ C$ ,  $R_L=4\Omega$ , Gain=6dB, (Unless otherwise noted)

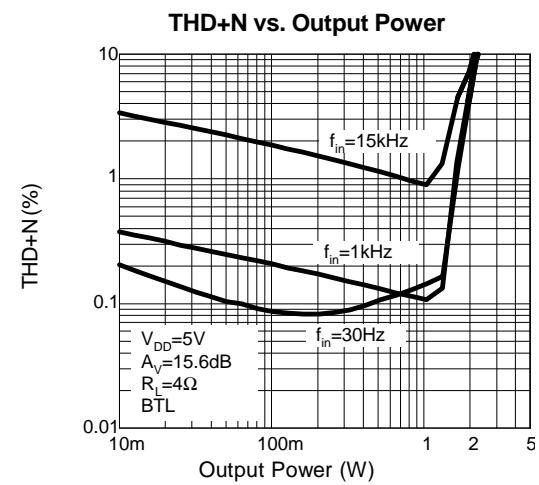
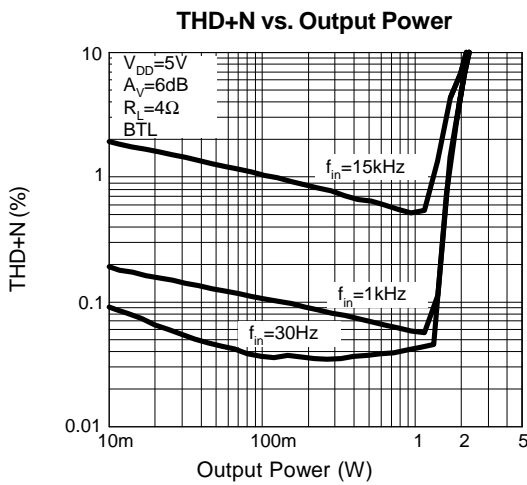
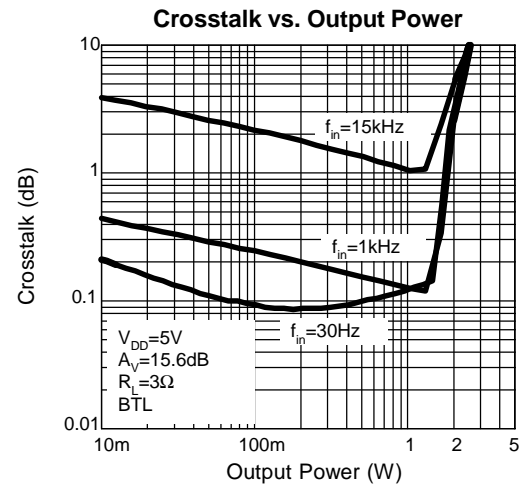
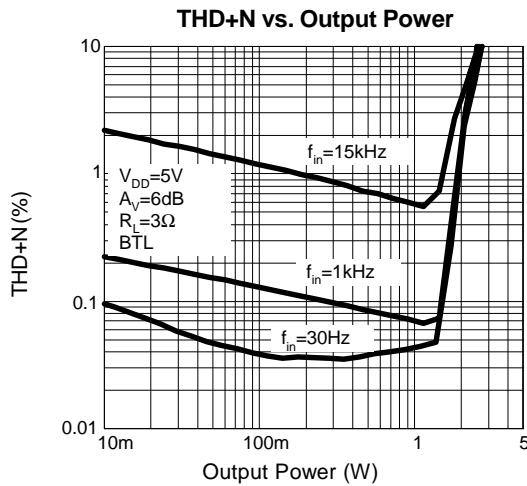
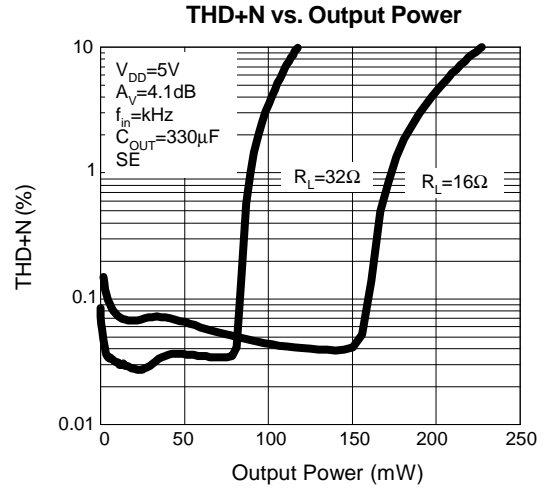
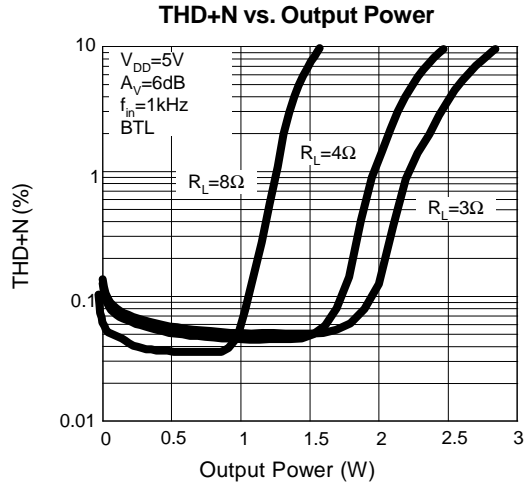
Symbol	Parameter	Test Conditions	APA2030 / 2031			Unit
			Min.	Typ.	Max.	
P <sub>O</sub>	Maximum Output Power	THD+N=10%, f <sub>in</sub> =1kHz, R <sub>L</sub> =3Ω	-	2.6	-	W
		THD+N =10%, f <sub>in</sub> =1kHz, R <sub>L</sub> =4Ω	-	2.3	-	W
		THD+N =10%, f <sub>in</sub> =1kHz, R <sub>L</sub> =8Ω	-	1.5	-	W
		THD+N =1%, f <sub>in</sub> =1kHz, R <sub>L</sub> =3Ω	-	1.9	-	W
		THD+N =1%, f <sub>in</sub> =1kHz, R <sub>L</sub> =4Ω	-	1.7	-	W
		THD+N =1%, f <sub>in</sub> =1kHz, R <sub>L</sub> =8Ω	1	1.1	-	W
THD+N	Total Harmonic Distortion Plus Noise	P <sub>O</sub> =1.1W, R <sub>L</sub> =4Ω f <sub>in</sub> =1kHz	-	0.05	-	%
		P <sub>O</sub> =0.7W, R <sub>L</sub> =8Ω, f <sub>in</sub> =1kHz	-	0.04	-	%
PSRR	Power Ripple Rejection Ratio	V <sub>IN</sub> =0.2Vrms, R <sub>I</sub> =8Ω, C <sub>B</sub> =0.47μF, f <sub>in</sub> =120Hz	-	85	-	dB
Crosstalk	Channel Separation	f <sub>in</sub> =1kHz, C <sub>B</sub> =0.47μF,	-	95	-	dB
	HP/LINE Input Separation	f <sub>in</sub> =1kHz, C <sub>B</sub> =0.47μF,	-	80	-	dB
S/N	Signal to Noise Ratio	P <sub>O</sub> =1.1W, R <sub>I</sub> =8Ω, A_weighting	-	105	-	dB

### Operating Characteristics, SE mode ( for APA2030 only)

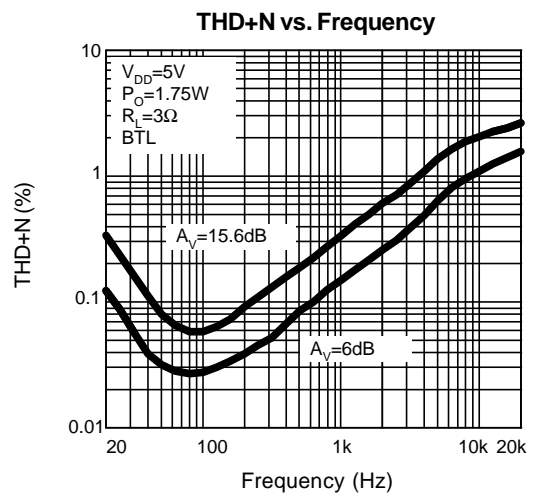
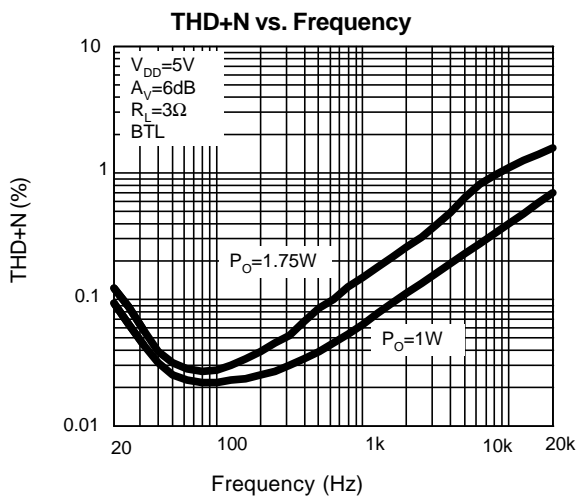
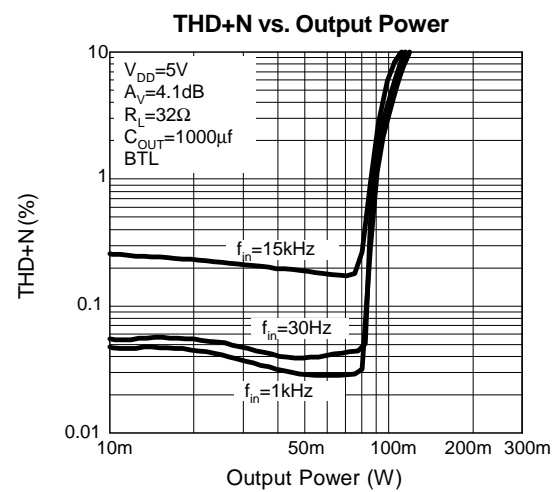
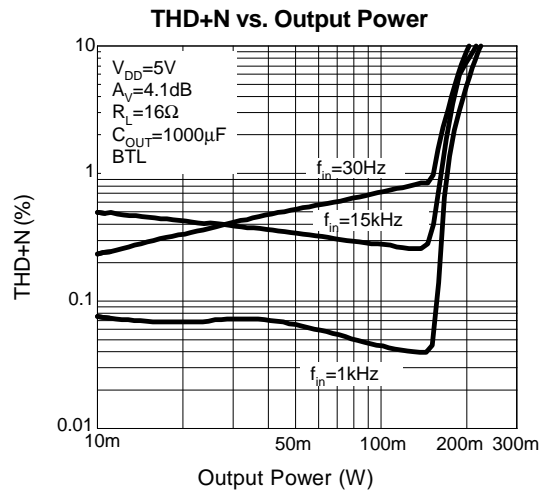
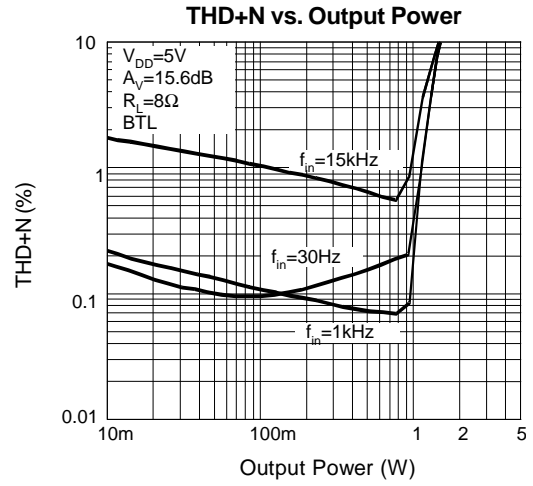
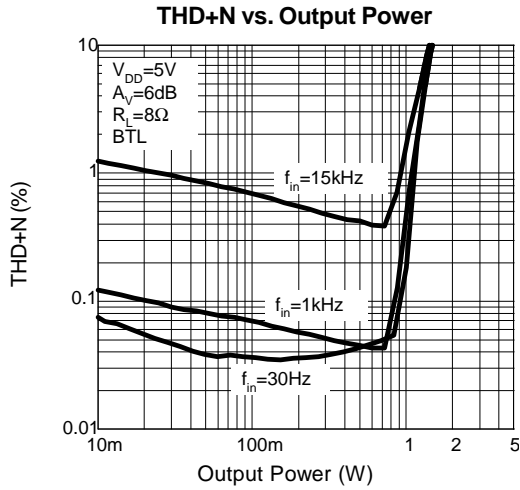
$V_{DD}=5V$ ,  $T_A=25^\circ C$ ,  $R_L=32\Omega$ , Gain=4, 1dB, (Unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2030			Unit
			Min.	Typ.	Max.	
P <sub>O</sub>	Maximum Output Power	THD+N=10%, f <sub>in</sub> =1kHz, R <sub>L</sub> =32Ω	-	110	-	mW
		THD+N =1%, f <sub>in</sub> =1kHz, R <sub>L</sub> =32Ω	-	90	-	mW
THD+N	Total Harmonic Distortion Plus Noise	P <sub>O</sub> =75mW, R <sub>L</sub> =32Ω, f <sub>in</sub> =1kHz	-	0.03	-	%
PSRR	Power Ripple Rejection Ratio	V <sub>IN</sub> =0.2Vrms, R <sub>I</sub> =32Ω, C <sub>B</sub> =0.47μF, f <sub>in</sub> =120,	-	55	-	dB
	SE/BTL Attenuation		-	80	-	dB
Crosstalk	Channel Separation	f <sub>in</sub> =1kHz, C <sub>B</sub> =0.47μF,	-	65	-	dB
	HP/LINE Input Separation	f <sub>in</sub> =1kHz, C <sub>B</sub> =0.47μF, BTL	-	80	-	dB
S/N	Signal to Noise Ratio	P <sub>O</sub> =75mW, R <sub>I</sub> =32Ω, A_weighting	-	100	-	dB

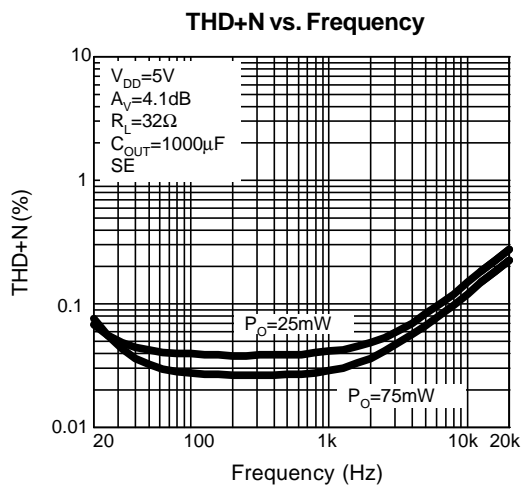
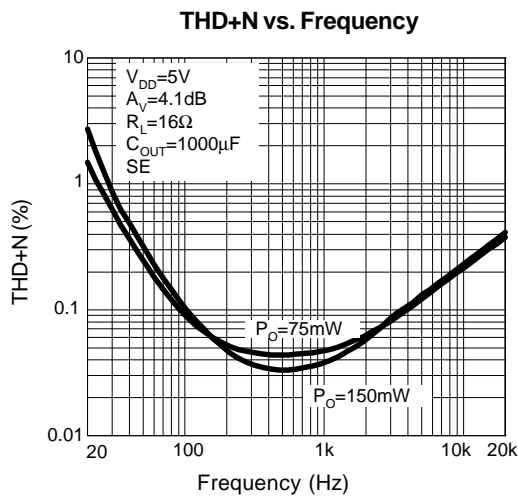
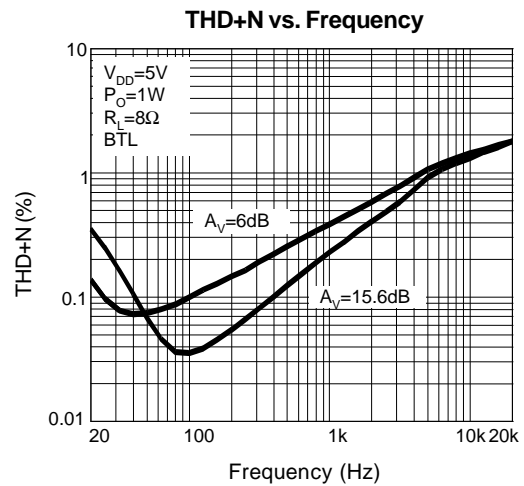
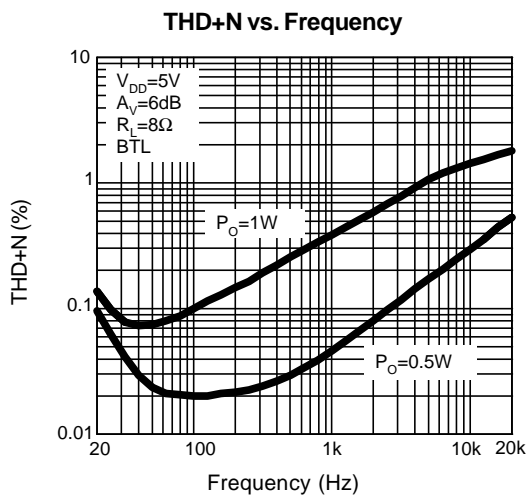
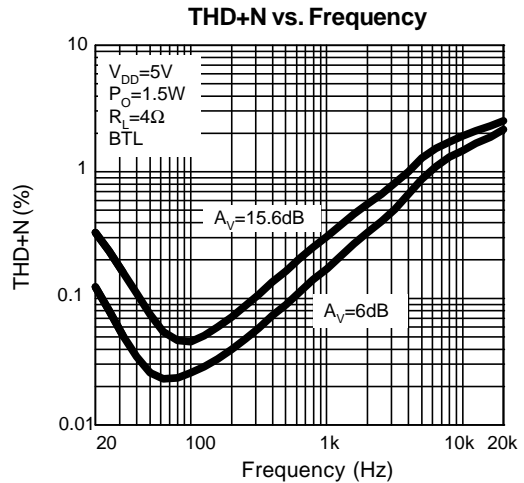
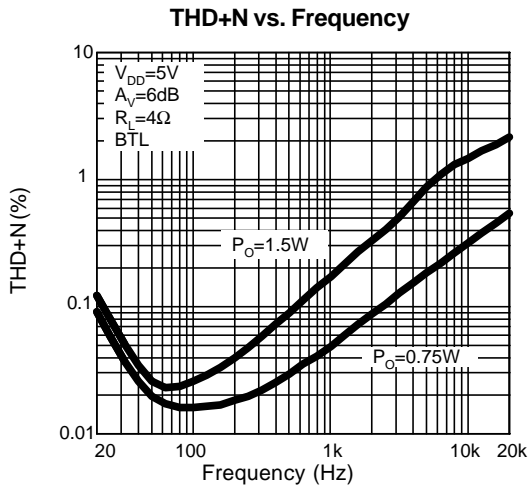
Typical Operating Characteristics



Typical Operating Characteristics (Cont.)

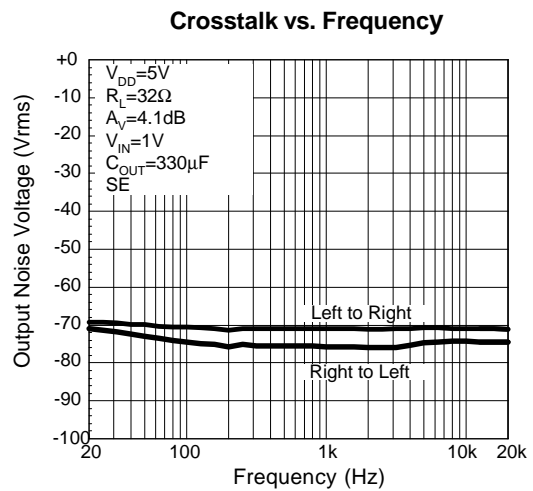
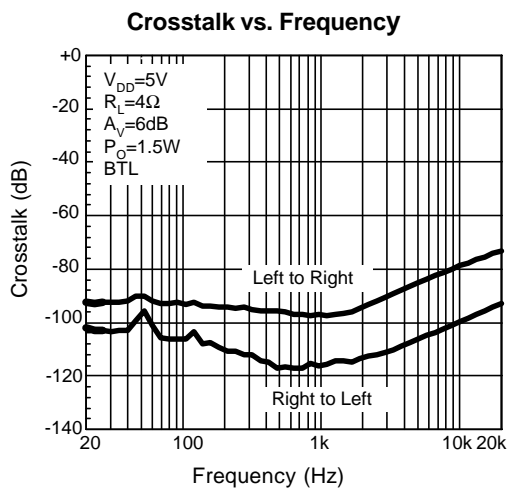
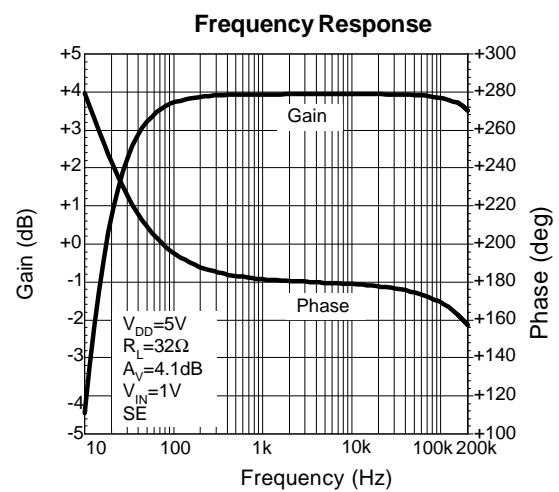
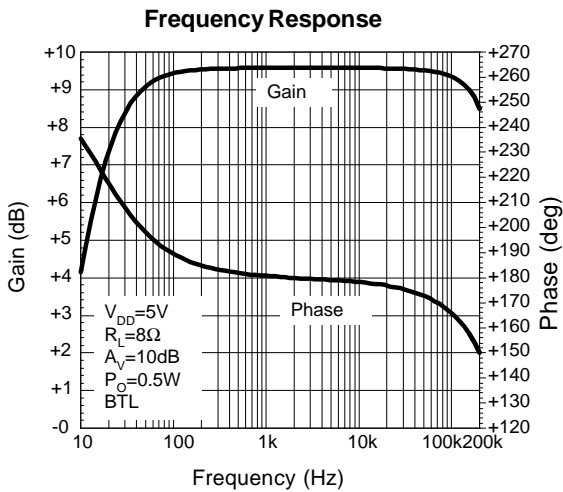
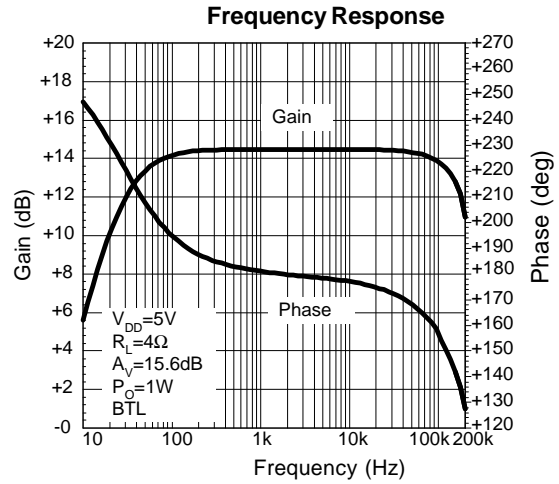
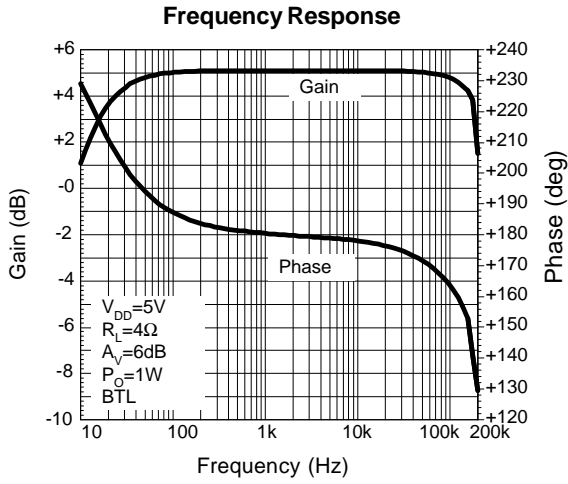


Typical Operating Characteristics (Cont.)

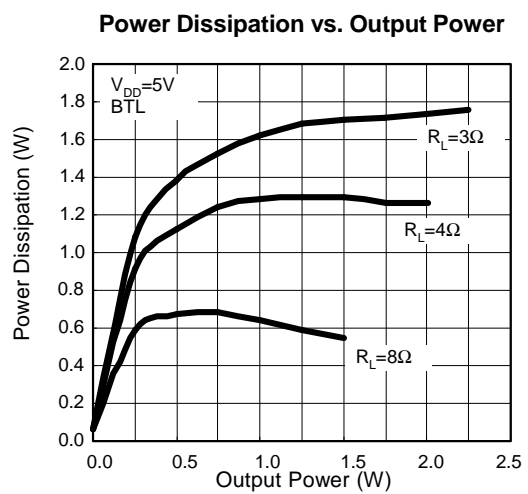
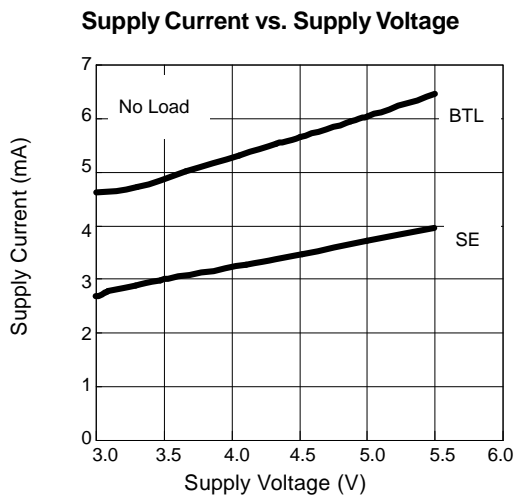
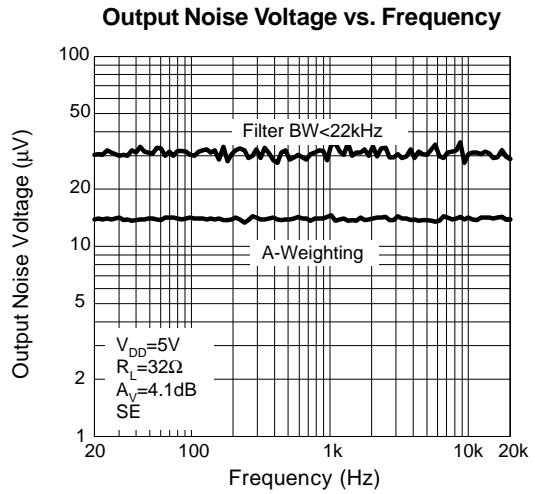
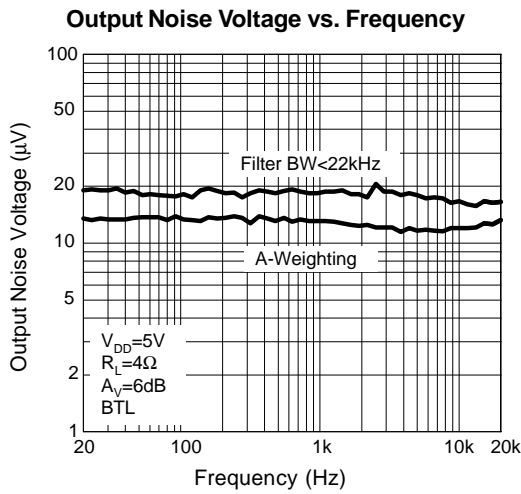
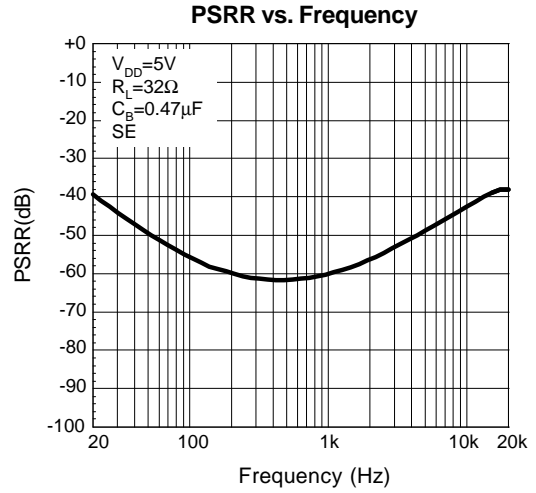
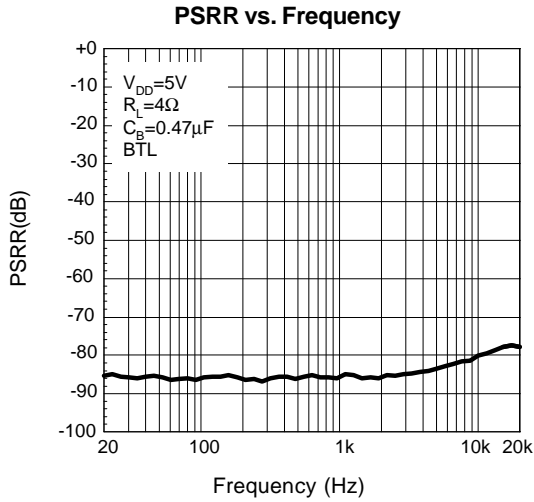




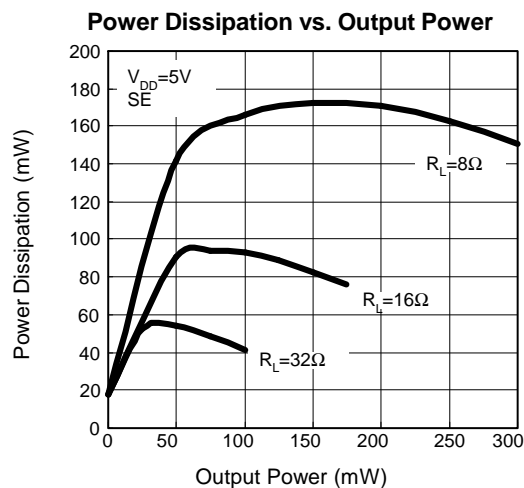
Typical Operating Characteristics (Cont.)



Typical Operating Characteristics (Cont.)



## Typical Operating Characteristics (Cont.)



## Pin Description

### APA2030

PIN NAME	PIN NO.	CONFIG.	FUNCTION
GND	1, 12, 13, 24	-	Ground connection, connected to thermal pad.
GAIN0	2	I/P	Input signal for internal gain setting.
GAIN1	3	I/P	Input signal for internal gain setting.
LOUT+	4	O/P	Left channel positive output in BTL mode and SE mode.
LLINEIN	5	I/P	Left channel line input terminal, selected when HP/LINE is held low.
RLINEIN	23	I/P	Right channel line input terminal, selected when HP/LINE is held low.
LHPIN	6	O/P	Left channel headphone input terminal, selected when HP/LINE is held high.
PVDD	7, 18	-	Supply voltage only for power amplifier.
RIN+	8	I/P	Right channel positive signal input when differential signal is accepted.
LOUT-	9	O/P	Left channel negative output in BTL mode and high impedance in SE mode.
LIN+	10	I/P	Left channel positive signal input when differential signal is accepted.
BYPASS	11	-	Bypass voltage.
PCBEEP	14	I/P	PC-beep signal input.
SE/BTL	15	I/P	Output mode control input pin, high for SE output mode and low for BTL mode.
ROUT-	16	O/P	Right channel negative output in BTL mode and high impedance in SE mode.
HP/LINE	17	I/P	Multi-input selection input, headphone mode when held high, line-in mode when held low.
VDD	19	-	Supply voltage for internal circuit excepting power amplifier.
RHPIN	20	I/P	Right channel headphone input terminal, selected when HP/LINE is held high.
ROUT+	21	O/P	Right channel positive output in BTL mode and SE mode.
SHUTDOWN	22	I/P	It will be into shutdown mode when pull low.
RLINEIN	23	I/P	Right channel line input terminal, selected when HP/LINE is held low.

## Pin Description (Cont.)

### APA2031

PIN NAME	PIN NO	CONFIG.	FUNCTION
GND	1, 11, 13, 20	-	Ground connection, connected to thermal pad.
GAIN0	2	I/P	Input signal for internal gain setting.
GAIN1	3	I/P	Input signal for internal gain setting.
LOUT+	4	O/P	Left channel positive output.
LIN-	5	I/P	Left channel negative audio signal input.
PVDD	6,15	-	Supply voltage only for power amplifier.
RIN+	7	I/P	Right channel positive audio signal input.
LOUT-	8	O/P	Left channel negative output.
LIN+	9	I/P	Left channel positive audio signal input.
BYPASS	10	-	Bypass voltage.
NC	12	-	No connection.
ROUT-	14	O/P	Right channel negative output.
VDD	16	-	Supply voltage for internal circuit excepting power amplifier.
RIN+	17	I/P	Right channel negative audio signal input.
ROUT+	18	O/P	Right channel positive output.
SHUTDOWN	19	I/P	It will be into shutdown mode when pull low.

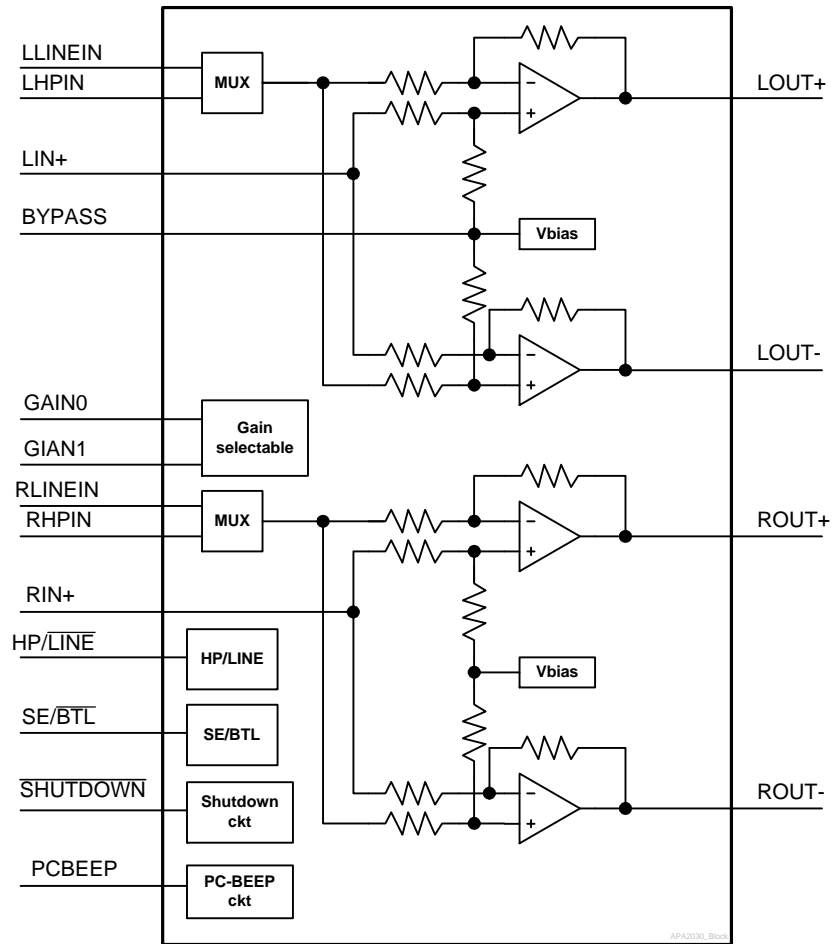
### Control Input Table ( for APA2030 only)

HP/ LINE	SE/BTL	SHUTDOWN	PCBEEP	Operating mode
X	X	L	Disable	Shutdown mode
L	L	H	Disable	Line input, BTL out
H	L	H	Disable	HP input, BTL out
L	H	H	Disable	Line input, SE out
H	H	H	Disable	HP input, SE out
X	X	X	Enable	PC-BEEP input, BTL out

### Gain Setting Table (for both APA2030 and APA2031)

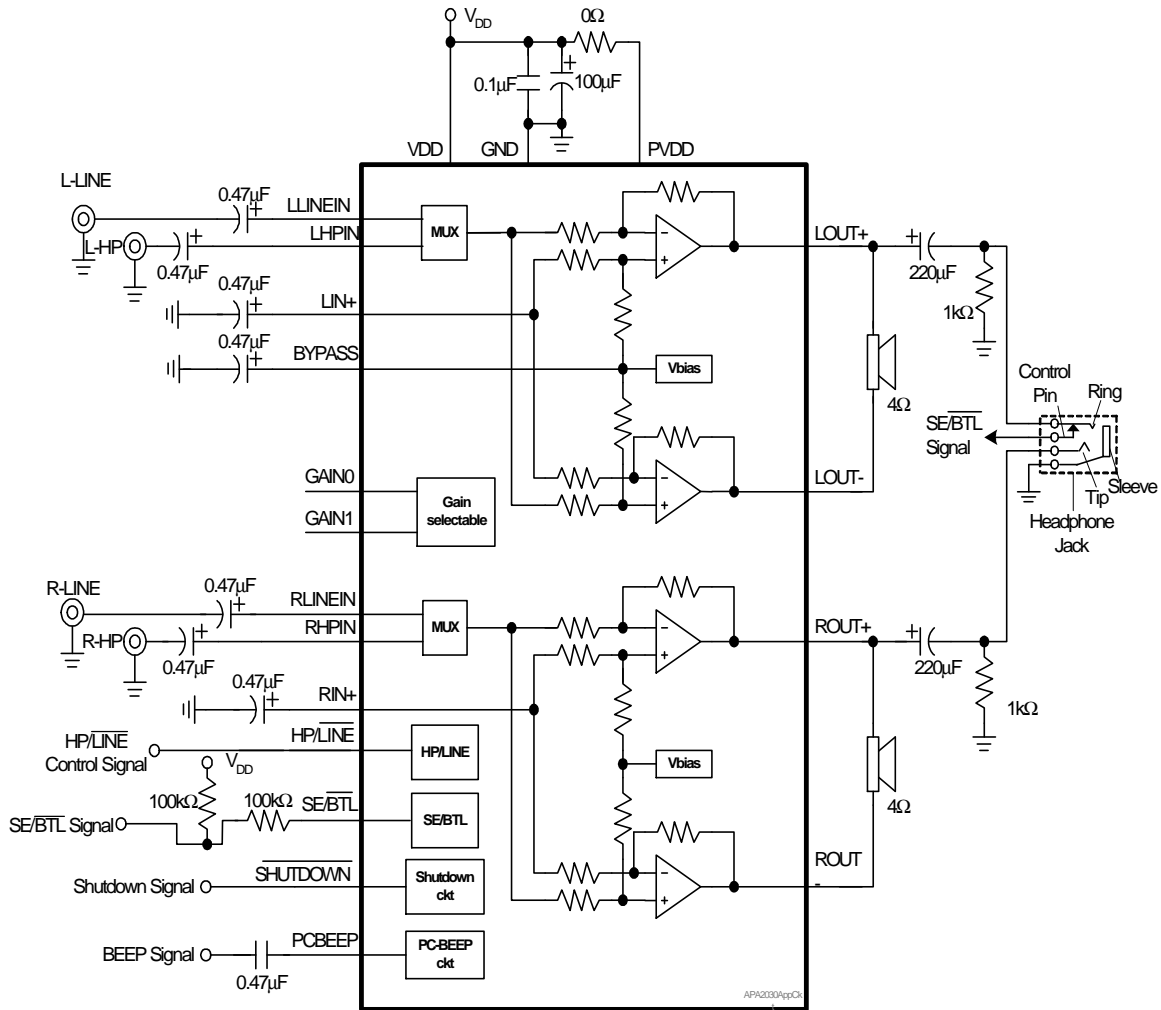
GAIN0	GAIN1	$R_i$	$R_f$	$A_v$
0	0	90k $\Omega$	90k $\Omega$	6dB
0	1	69k $\Omega$	111k $\Omega$	10dB
1	0	42k $\Omega$	138k $\Omega$	15.6dB
1	1	25.7k $\Omega$	154.3k $\Omega$	21.6dB

Block Diagram



## Typical Application Circuit

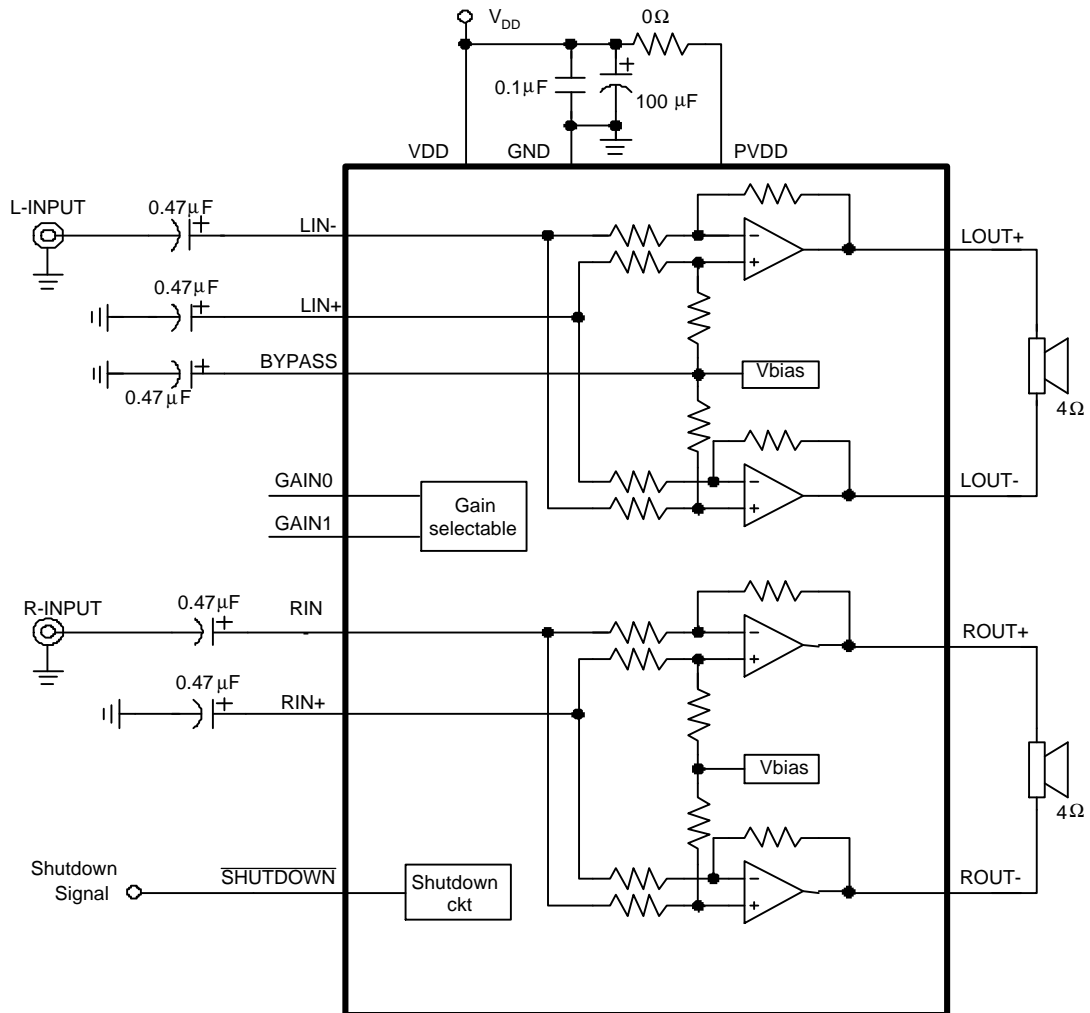
(for APA2030 using SE input signal)



APA2030

## Typical Application Circuit (Cont.)

(for APA2031 using SE input signal)



APA2031

## Application Information

### BTL Operation

The APA2030/1 has two pairs of operational amplifiers internally, which allows for different amplifier configurations.

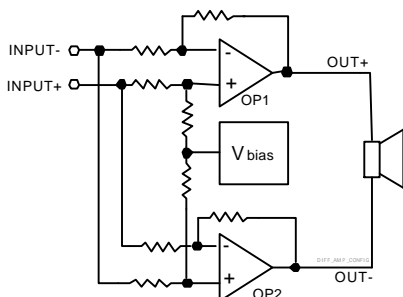


Figure 1: APA2030 Internal Configuration (each channel)

The OP1 and OP2 are all differential drive configurations. The differential driver configures doubling voltage swing on the load. Compare with the single-ended configuration, the differential gain for each channel is 2X (Gain of SE mode).

By driving the load differentially through outputs OUT+ and OUT-, an amplifier configuration which is commonly referred to as bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus doubling the output swing for a specified supply voltage. Four times the output power is possible as compared with a SE amplifier under the same conditions. A BTL configuration, such as the one used in APA2030/1, also creates a second advantage over SE amplifiers. Since the differential outputs, ROUT+, ROUT-, LOU+, and LOU-, are biased at half-supply, DC voltage doesn't exist across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

### Single-Ended Operation (for APA2030 only)

Consider the single-supply SE configuration shown Application Circuit. A coupling capacitor is required to block the DC offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF)

so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system (refer to the Output Coupling Capacitor).

The rules described should be following the relationship:

$$\frac{1}{C_{bypass} \times 250k\Omega} \leq \frac{1}{R_i C_i} \leq \frac{1}{R_L C_c} \dots \dots \dots (1)$$

### Output SE/BTL Operation (for APA2030 only)

The ability of the APA2030 is to easily switch between BTL and SE modes which is one of its most important costs saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated.

The APA2030 has two separated amplifiers drive OUT+ and OUT- (See Figure 1). The SE/BTL input controls the operation of the amplifier that drives LOU+ and LOU-.

- When SE/BTL is held low, the OP2 is activated and the APA2030 is in the BTL mode.
- When SE/BTL is held high, the OP2 is in a high output impedance state, which configures the APA2030 as SE driver from OUT+. I<sub>DD</sub> is reduced by approximately one-half in SE mode.

The SE/BTL input can be a logic-level TTL source, a resistor divider network or the stereo headphone jack with switch pin as shown in Application Circuit.

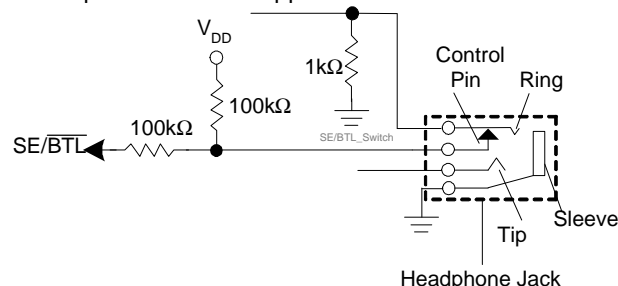


Figure 2: SE/BTL input selection by phonejack plug

In Figure 2, input SE/BTL operates as below:

When the phone jack plug is inserted, the 1kΩ resistor is disconnected and the SE/BTL input is pulled high and enables the SE mode. When the input goes high level,



## Application Information (Cont.)

### Output SE/BTL Operation (for APA2030 only) (Cont.)

the OUT- amplifier is shutdown and causes the speaker to mute. And then, the OUT+ amplifier drives through the output capacitor (CO) into the headphone jack.

When there is no headphone plugged into the system, the contact pin of the headphone jack is connected from the signal pin, the voltage divider is set up by resistors 100kΩ and 1kΩ. Resistor 1kΩ then pulls low the SE/BTL pin, enabling the BTL function.

### Input HP/LINE Operation (for APA2030 only)

APA2030 amplifier has two separated inputs for each of the left and right stereo channels. An internal multiplexer selects which input will be connected to the amplifier based on the state of the HP/LINE pin on the IC.

- To select the line inputs, set HP/LINE pin tied to low level
- To enable the headphone inputs, set HP/ LINE pin tied to high level

Refer to the application circuit, the voltage divider of 100kΩ and 1kΩ sets the voltage at the HP/LINE pin to be approximately 50mV when there are no headphones plugged into the system. This logic low voltage at the HP/LINE pin enables the APA2030 and places it LINE input mode operation.

When a set of headphones is plugged into the system, the contact pin of the headphone jack is disconnected from the signal pin, interrupting the voltage divider set up by resistors 100kΩ. Resistor 100kΩ then pulls-up the HP/LINE pin, enabling the headphone input function.

### Differential Input Operation

The APA2030/1 can accept the differential input signal and improve the CMRR (Common Mode Rejection Ratio). For example, when applying differential input signals to APA2031, connect positive input signals to the IN+ (LIN+ and RIN+) of APA2031 and negative input signals to the IN- (LIN- and RIN-) of APA2031.

When input signals are single-end, just connect IN+ (LIN+ and RIN+) to ground via a capacitor.

### Input Resistance, R<sub>i</sub>

The APA2030/1 provides four gain setting decided by GAIN0 and GAIN1 input pins in differential mode and it becomes 4.1dB fixed gain when SE mode is selected (for APA2030). In Table 1, according to BTL operation, internal resistors R<sub>i</sub> and R<sub>f</sub> set the gain for each audio input of the APA2030/1.

GAIN0	GAIN1	R <sub>i</sub>	R <sub>f</sub>	SE/BTL	A <sub>v</sub>
0	0	90kΩ	90kΩ	0	6dB
0	1	69kΩ	111kΩ	0	10dB
1	0	42kΩ	138kΩ	0	15.6dB
1	1	25.7kΩ	154.3kΩ	0	21.6dB
X	X	69kΩ	111kΩ	1	4.1dB

Table 1: The close loop gain setting resistance R<sub>f</sub>/R<sub>i</sub>

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. The input resistance has wide variation (+/-10%) caused by manufacturing.

### Input Capacitor, C<sub>i</sub>

In the typical application, an input capacitor, C<sub>i</sub>, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C<sub>i</sub> and the minimum input impedance R<sub>i</sub> form a high-pass filter with the corner frequency determined in the following equation:

$$f_{c(\text{highpass})} = \frac{1}{2\pi R_{i(\text{min})} \times C_i} \dots\dots\dots(2)$$

The value of C<sub>i</sub> must be considered carefully because it directly affects the low frequency performance of the circuit. Consider the example where R<sub>i</sub> is 90kΩ when 6dB gain is set and the specification calls for a flat bass response down to 40Hz. The equation is reconfigured below:

$$C_i = \frac{1}{2\pi R_i f_c} \dots\dots\dots(3)$$

Consider the variation of input resistance (R<sub>i</sub>), the value of C<sub>i</sub> should be 0.04μF. Therefore, it's better to choose a value in the range from 0.1μF to 1.0μF.

**Application Information (Cont.)**

**Input Capacitor, C<sub>i</sub> (Cont.)**

A further consideration for this capacitor is the leakage path from the input source through the input network (R<sub>i</sub>+R<sub>p</sub>, C<sub>i</sub>) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level there is held at V<sub>DD</sub>/2. Please note that it is important to confirm the capacitor polarity in the application.

**Effective Bypass Capacitor, C<sub>bypass</sub>**

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitor located on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger half supply bypass capacitor improves PSRR due to increased half-supply stability. Typical applications employ a 5V regulator with 1.0μF and a 0.1μF bypass capacitors which aid in supply filtering. This does not eliminate the need for bypassing the supply nodes of the APA2030/1. The selection of bypass capacitors, especially C<sub>B</sub>, is thus dependent upon desired PSRR requirements, click and pop performance. To avoid start-up pop noise occurred, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation should be maintained.

$$\frac{1}{C_{bypass} \times 250k\Omega} \ll \frac{1}{C_i \times 180k\Omega} \dots\dots\dots(4)$$

The capacitor is fed from a 250kΩ source inside the amplifier. Bypass capacitor, C<sub>B</sub>, values of 3.3μF to 10μF ceramic or tantalum low-ESR capacitors are recommended for the best THD+N and noise performance.

The bypass capacitance also affects the start-up time. It is determined in the following equation:

$$T_{Startup} = 5 \times (C_{bypass} \times 250k\Omega) \dots\dots\dots(5)$$

**Output Coupling Capacitor, C<sub>c</sub> (for APA2030 only)**

In the typical single-supply SE configuration, an output coupling capacitor (C<sub>c</sub>) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation.

$$f_{c(highpass)} = \frac{1}{2\pi R_L C_c} \dots\dots\dots(6)$$

For example, a 330μF capacitor with an 8Ω speaker would attenuate low frequencies below 60.6Hz. Large values of C<sub>c</sub> are required to pass low frequencies into the load.

**Power Supply Decoupling, C<sub>s</sub>**

The APA2030/1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible.

Power supply decoupling also prevents the oscillations caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that targets on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF placed as close as possible to the device VDD lead works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

**Shutdown Function**

In order to reduce power consumption while not in use, the APA2030/1 contains a shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the SHUTDOWN pin. The trigger point between a logic high and logic low level is typically 2.0V. It is better to switch between ground and the supply V<sub>DD</sub> to provide maximum device performance.

## Application Information (Cont.)

### Shutdown Function (Cont.)

By switching the  $\overline{\text{SHUTDOWN}}$  pin to low, the amplifier enters a low-current state,  $I_{DD} < 50\text{mA}$ . The APA2030 is in shutdown mode, except PC-BEEP detect circuit. On normal operating,  $\overline{\text{SHUTDOWN}}$  pin is pulled to high level to keep the IC out of the shutdown mode. The  $\overline{\text{SHUTDOWN}}$  pin should be tied to a definite voltage to avoid unwanted state changes.

### PC-BEEP Detection ( for APA2030 only)

The APA2030 integrates a PC-BEEP detect circuit for NOTEBOOK PC using. Over 1Vpp amplitude PC-BEEP signal with the rising time/falling time under  $1\mu\text{s/V}$  should be provided to trigger the APA2030 into PC-BEEP mode. The input impedance is  $100\text{k}\Omega$  and the bias voltage on PC-BEEP input pin is 2.5V. Therefore, the voltage level of PC-BEEP signal should be higher than 3V and lower than 2V to into PCBEEP mode correctly.

When PC-BEEP signal drives to PC-BEEP input pin, the PC-BEEP mode will be active. When chip in the PC-BEEP mode, the APA2030 will be forced to be in BTL mode and the internal gain is fixed as -10dB. The PC-BEEP signal turns to be the amplifier input signal and plays on the speaker without coupling capacitor. If the amplifier is in the shutdown mode, it will be out of shutdown mode whenever PC-BEEP mode enabled. The APA2030 will return to previous setting when it is out of PC-BEEP mode.

### Optimizing Depop Circuitry

Circuitry has been included in the APA2030/1 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry. The value of  $C_i$  will also affect turn-on pops. (Refer to Effective Bypass Capacitance) The bypass voltage rise up should be slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of  $C_B$  can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of  $C_B$ , turn-on pop can be reduced. However, the tradeoff for

using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of  $C_B$  and the turn-on time.

In a SE (for APA2030) configuration, the output coupling capacitor,  $C_C$ , is of particular concern. This capacitor discharges through the internal  $10\text{k}\Omega$  resistors. Depending on the size of  $C_C$ , the time constant can be relatively large. To reduce transients in SE mode, an external  $1\text{k}\Omega$  resistor can be placed in parallel with the internal  $10\text{k}\Omega$  resistor. The tradeoff for using this resistor is an increase in quiescent current.

In the most cases, choosing a small value of  $C_i$  in the range of  $0.33\mu\text{F}$  to  $1\mu\text{F}$ ,  $C_B$  being equal to  $0.47\mu\text{F}$  and an external  $1\text{k}\Omega$  resistor should be placed in parallel with the internal  $10\text{k}\Omega$  resistor, and it should produce a virtually clickless and popless turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. Hence, it is advantageous to use low-gain configurations.

### BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_o}{P_{\text{SUP}}} \dots\dots\dots(7)$$

Where

$$P_o = \frac{V_{\text{rms}} \times V_{\text{rms}}}{R_L} = \frac{V_P \times V_P}{2R_L}$$

$$V_{\text{rms}} = \frac{V_P}{\sqrt{2}} \dots\dots\dots(8)$$

$$P_{\text{SUP}} = V_{DD} \times I_{DD(\text{AVG})} = \frac{2V_P}{\pi R_L} \dots\dots\dots(9)$$

Efficiency of a BTL configuration

$$\frac{P_o}{P_{\text{SUP}}} = \frac{\left(\frac{V_P \times V_P}{2R_L}\right)}{V_{DD} \times \pi R_L} = \frac{\pi V_P}{4V_{DD}} \dots\dots\dots(10)$$

## Application Information (Cont.)

### BTL Amplifier Efficiency (Cont.)

Table 2 calculates efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 3W.

Po (W)	Efficiency (%)	I <sub>DD</sub> (A)	V <sub>PP</sub> (V)	P <sub>D</sub> (W)
0.25	31.25	0.16	2.00	0.55
0.50	47.62	0.21	2.83	0.55
1.00	66.67	0.30	4.00	0.5
1.25	78.13	0.32	4.47	0.35

\*\*High peak voltages cause the THD+N to increase.

Table 2. Efficiency vs. Output Power in 5V/8W BTL Systems

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation, V<sub>DD</sub> is in the dominator. This indicates that as V<sub>DD</sub> goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

### Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. In equation11, it states that the maximum power dissipation point for a SE mode operates at a given supply voltage and drives a specified load.

$$SE \text{ mode : } P_{D,MAX} = \frac{V_{DD}^2}{2\pi^2 R_L} \dots\dots\dots(11)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus, the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$BLT \text{ mode : } P_{D,MAX} = \frac{4V_{DD}^2}{2\pi^2 R_L} \dots\dots\dots(12)$$

Since the APA2030/1 is a dual channel power amplifier, the maximum internal power dissipation is 2 times that both of equations depending on the mode of operation. Even with this substantial increase in power dissipation, the APA2030/1 does not require extra heatsink. The power dissipation from equation12, assuming a 5V-power supply and an 8W load, must not be greater than the power dissipation that results from the equation13:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}} \dots\dots\dots(13)$$

For TSSOP-24P (APA2030) and TSSOP-20P (APA2031) package with and without thermal pad, the thermal resistance (θ<sub>JA</sub>) is equal to 45°C/W and 48°C/W respectively.

Since the maximum junction temperature (T<sub>J,MAX</sub>) of APA2030/1 is 150°C and the ambient temperature (T<sub>A</sub>) is defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation12. Once the power dissipation is greater than the maximum limit (P<sub>D,MAX</sub>), either the supply voltage (V<sub>DD</sub>) must be decreased, the load impedance (R<sub>L</sub>) must be increased or the ambient temperature should be reduced.

### Thermal Pad Consideration

The thermal pad must be connected to ground. The package with thermal pad of the APA2030/1 requires special attention on thermal design. If the thermal design issues are not properly addressed, the APA2030/1 4Ω will go into thermal shutdown when driving a 4Ω load.

The thermal pad on the bottom of the APA2030/1 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 13 mil or smaller in diameter should be used to thermally couple

**Application Information (Cont.)**

**Thermal Pad Consideration (Cont.)**

the thermal pad to the bottom plane. For good thermal conduction, the vias must be plated through and solder filled. The copper plane is used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the APA2030/1 junction temperature below the thermal shutdown temperature (150°C).

In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

**Thermal Consideration**

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. To calculate maximum ambient temperatures, first consideration is that the numbers from the **Power Dissipation vs. Output Power** graphs (Page 9 and 10) are per channel values, so the dissipation of the IC heat needs to be doubled for two-channel operation. Given  $\theta_{JA}$ , the maximum allowable junction temperature ( $T_{J,MAX}$ ), and the total internal dissipation ( $P_D$ ), the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the APA2030/1 is 150°C. The internal dissipation figures are taken from the **Power Dissipation vs. Output Power** graphs. (Page 9 and 10)

$$T_{A,MAX} = T_{J,MAX} - \theta_{JA}P_D \dots\dots\dots(14)$$

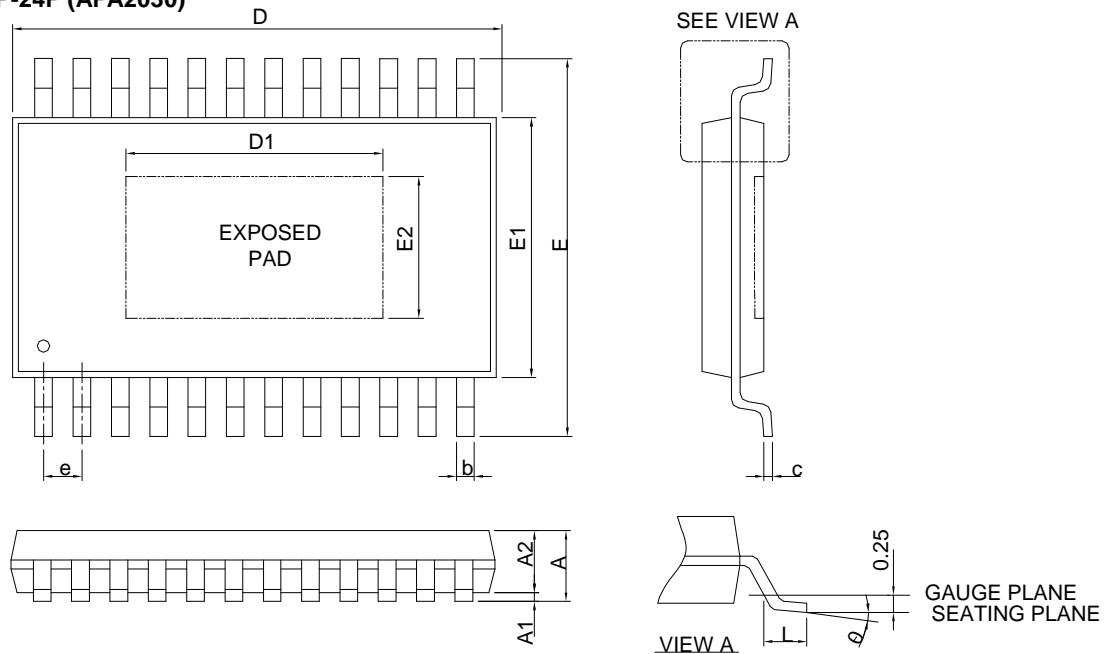
$$150 - 45(0.8*2) = 78^\circ\text{C (TSSOP-24P)}$$

$$150 - 48(0.8*2) = 73.2^\circ\text{C (TSSOP-20P)}$$

The APA2030/1 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent the IC from damages.

## Package Information

### TSSOP-24P (APA2030)



SYMBOL	TSSOP-24P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	7.70	7.9	0.303	0.311
D1	3.50	6.00	0.138	0.197
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
E2	2.50	3.50	0.098	0.138
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°

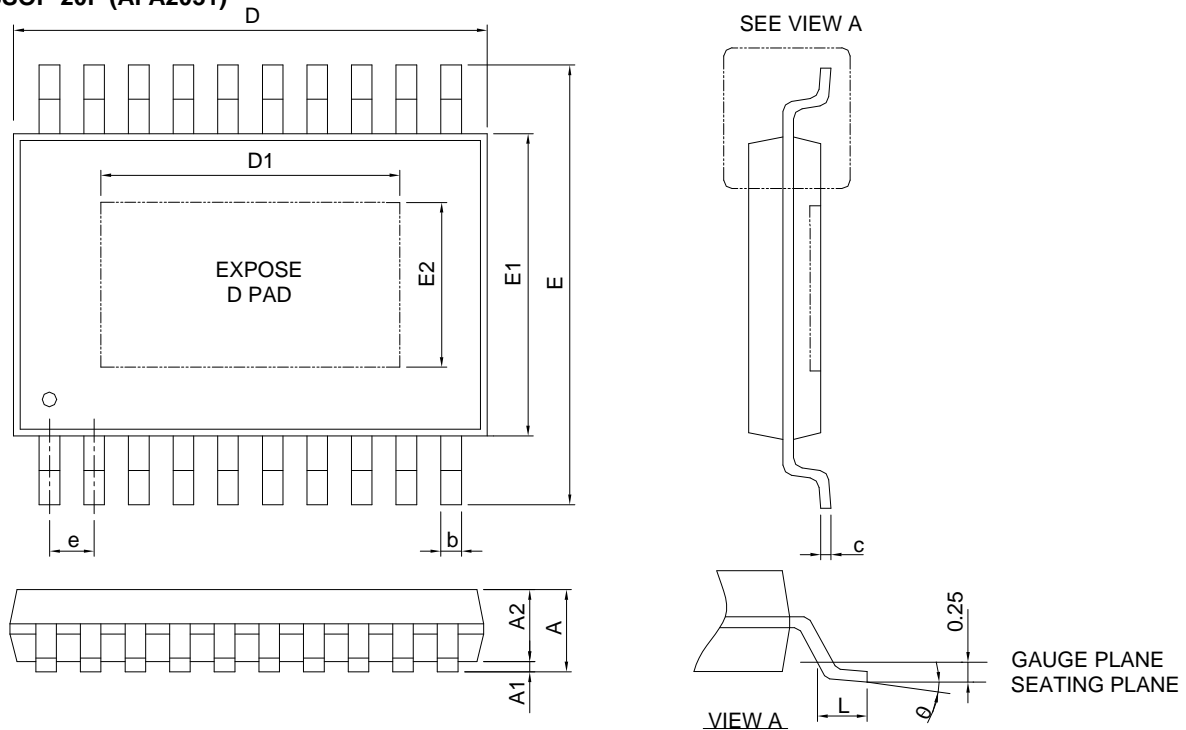
Note : 1. Followed from JEDEC MO-153 ADT.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

## Package Information

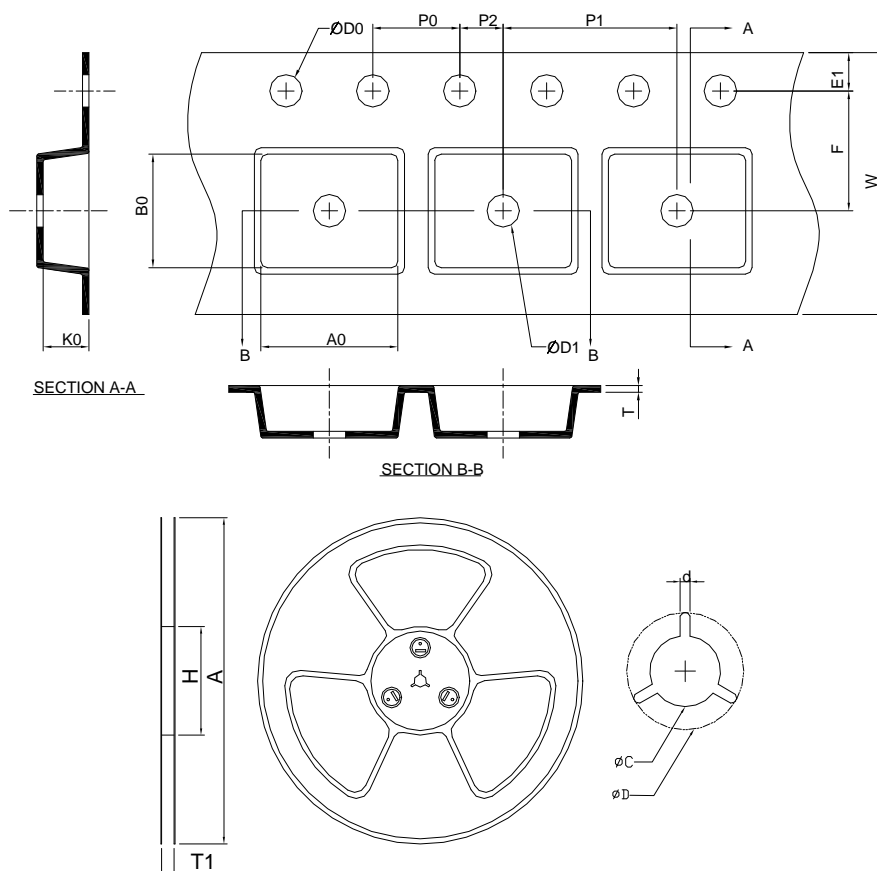
### TSSOP-20P (APA2031)



SYMBOL	TSSOP-20P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	6.40	6.60	0.252	0.260
D1	3.00	4.50	0.118	0.177
E	6.20	6.40	0.244	0.260
E1	4.30	4.50	0.169	0.177
E2	2.50	3.50	0.098	0.138
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
$\theta$	0°	8°	0°	8°

- Note : 1. Follow JEDEC MO-153 ACT.  
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.  
 3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

### Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TSSOP-24P	330.0 ±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0 ±0.30	1.75 ±0.10	7.50 ±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.00 ±0.10	8.00 ±0.10	2.00 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.3 ±0.05	6.9 ±0.20	8.30 ±0.20	1.60 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
TSSOP-20P	330.0 ±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0 ±0.30	1.75 ±0.10	7.50 ±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.00 ±0.10	8.00 ±0.10	2.00 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.30 ±0.05	6.9 ±0.20	6.90 ±0.20	1.60 ±0.20

(mm)

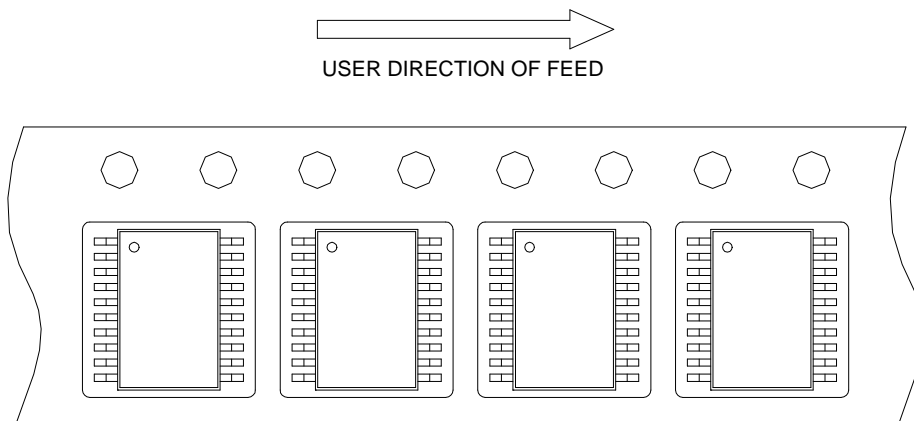
### Devices Per Unit

Package Type	Unit	Quantity
TSSOP-24P	Tape & Reel	2000
TSSOP-20P	Tape & Reel	2000

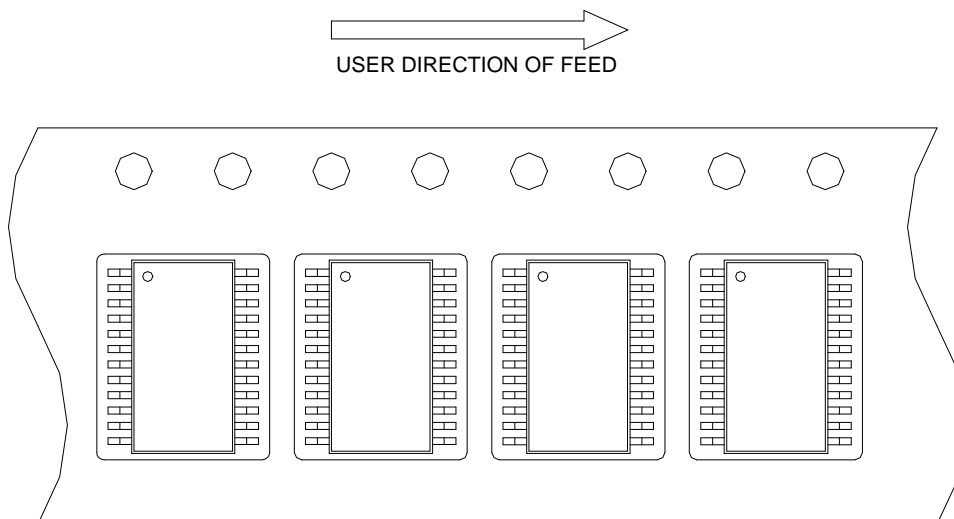


### Taping Direction Information

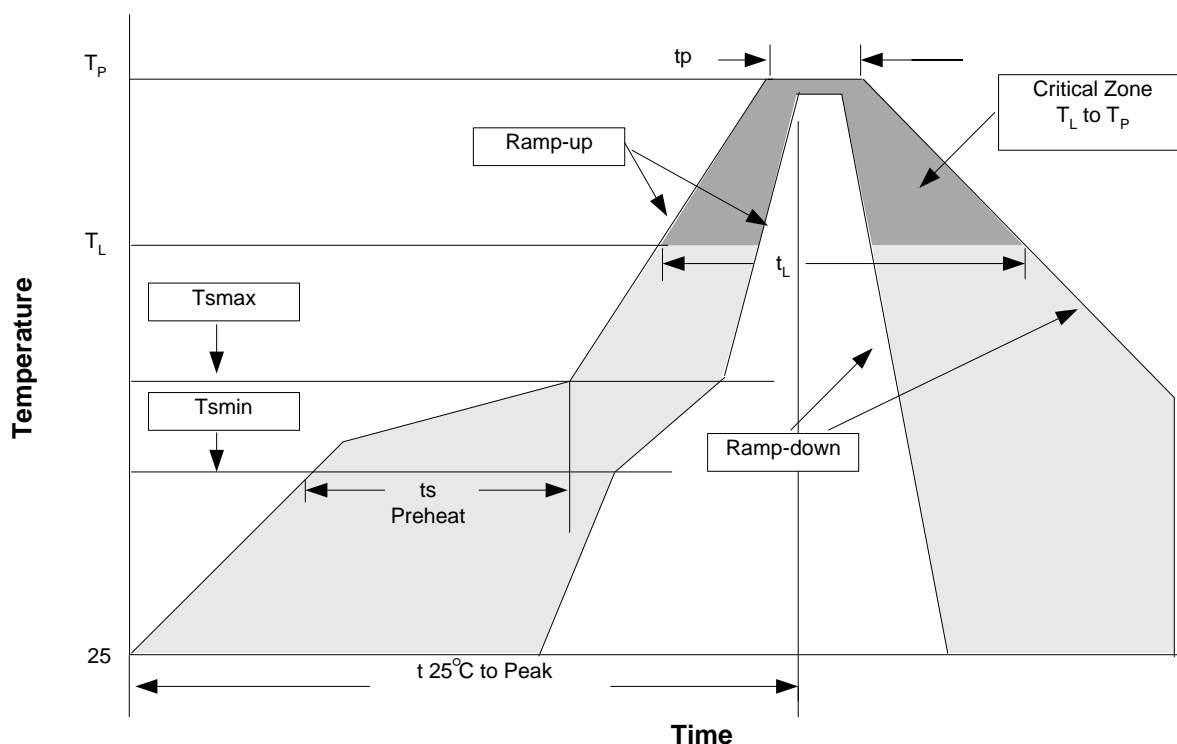
TSSOP-20(P)



TSSOP-24(P)



**Reflow Condition (IR/Convection or VPR Reflow)**



**Reliability Test Program**

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1 <sub>tr</sub> > 100mA

**Classification Reflow Profiles**

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T <sub>L</sub> to T <sub>P</sub> )	3°C/second max.	3°C/second max.
Preheat		
- Temperature Min (T <sub>min</sub> )	100°C	150°C
- Temperature Max (T <sub>max</sub> )	150°C	200°C
- Time (min to max) (t <sub>s</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
- Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak/Classification Temperature (T <sub>p</sub> )	See table 1	See table 2
Time within 5°C of actual Peak Temperature (t <sub>p</sub> )	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

## Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

\* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

## Customer Service

### Anpec Electronics Corp.

Head Office :

No.6, Dusing 1st Road, SBIP,  
Hsin-Chu, Taiwan, R.O.C.  
Tel : 886-3-5642000  
Fax : 886-3-5642050

Taipei Branch :

2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,  
Sindian City, Taipei County 23146, Taiwan  
Tel : 886-2-2910-3838  
Fax : 886-2-2917-3838