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3-Pin Microprocessor Reset Circuits

Description

The FP6809 and FP6810 are cost-effective system supervisory circuits which are designed to monitor micro-processor voltage and V_{CC} in digital systems. They provide a reset signal to the host processor when necessary.

These circuits assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold. They keep reset signal asserted for at least 140ms after V_{CC} has risen above the reset threshold.

The FP6809-N has an open-drain output stage which requires a pull-up resistor while FP6809-C and FP6810-C have push-pull outputs. The FP6809 has an active-low $\overline{\text{RESET}}$ output while the FP6810 has an active-high RESET output.

The FP6809 and FP6810 are optimized to reject fast transient glitches on the V_{CC} line. Low supply current makes these devices suitable for portable equipments.

Features

- Precision Monitoring of Power-Supply Voltage
- 140ms Guaranteed Minimum Reset Output Duration
- Low Supply Current
- V_{CC} Transient Immunity
- Small SOT-23-3 Package
- No External Components
- Guaranteed Reset Valid to V_{CC}=1V
- Available in Three Output Configurations
  - Open-Drain $\overline{\text{RESET}}$ Output (FP6809-N)
  - Push-Pull $\overline{\text{RESET}}$ Output (FP6809-C)
  - Push-Pull RESET Output (FP6810-C)
- RoHS Compliant

Applications

- Computer
- Battery Powered Equipment
- Microprocessor Power Supply Monitoring
- Embedded System
- Automotive

Pin Assignments

S3 Package (SOT-23-3)

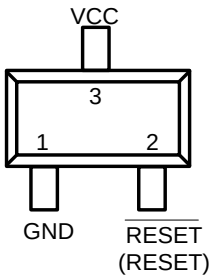


Figure 1. Pin Assignment of FP6809/FP6810

Ordering Information

FP6809/10-□□□□□

- TR: Tape/Reel
- P: Green
  G: Green
- Package Type
  S3: SOT-23-3
- N: Open-Drain (FP6809 only)
  C: Push-Pull
- Reset Voltage:
  23: 2.32V 40: 4.00V
  26: 2.63V 44: 4.38V
  29: 2.93V 46: 4.63V
  31: 3.08V
- FP6809: Active Low Reset
  FP6810: Active High Reset

Note1: Please consult Fitipower sales office or authorized distributors for availability of special reset voltages.

SOT-23-3 Marking (FP6809)

Part Number	Product Code	Part Number	Product Code
FP6809-23NS3P	**Cv**	FP6809-23CS3P	**CD**
FP6809-23NS3G	**Cv=**	FP6809-23CS3G	**CD=**
FP6809-26NS3P	**Cw**	FP6809-26CS3P	**CE**
FP6809-26NS3G	**Cw=**	FP6809-26CS3G	**CE=**
FP6809-29NS3P	**Cx**	FP6809-29CS3P	**CF**
FP6809-29NS3G	**Cx=**	FP6809-29CS3G	**CF=**
FP6809-31NS3P	**Cz**	FP6809-31CS3P	**CG**
FP6809-31NS3G	**Cz=**	FP6809-31CS3G	**CG=**
FP6809-40NS3P	**CA**	FP6809-40CS3P	**CH**
FP6809-40NS3G	**CA=**	FP6809-40CS3G	**CH=**
FP6809-44NS3P	**CB**	FP6809-44CS3P	**CJ**
FP6809-44NS3G	**CB=**	FP6809-44CS3G	**CJ=**
FP6809-46NS3P	**CC**	FP6809-46CS3P	**CK**
FP6809-46NS3G	**CC=**	FP6809-46CS3G	**CK=**

SOT-23-3 Marking (FP6810)

Part Number	Product Code	Part Number	Product Code
FP6810-23CS3P	**CL**	FP6810-31CS3G	**CP=**
FP6810-23CS3G	**CL=**	FP6810-40CS3P	**CR**
FP6810-26CS3P	**CM**	FP6810-40CS3G	**CR=**
FP6810-26CS3G	**CM=**	FP6810-44CS3P	**CS**
FP6810-29CS3P	**CN**	FP6810-44CS3G	**CS=**
FP6810-29CS3G	**CN=**	FP6810-46CS3P	**CT**
FP6810-31CS3P	**CP**	FP6810-46CS3G	**CT=**

Typical Application Circuit

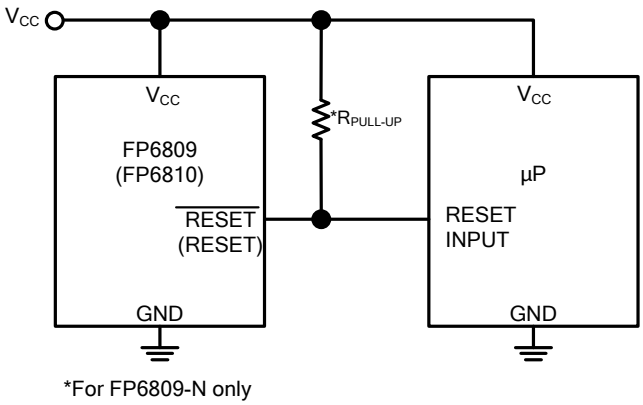


Figure 2. Typical Application Circuit of FP6809/FP6810

Functional Pin Description

Pin Name	Pin Function
GND	Ground
$\overline{\text{RESET}}$ (FP6809)	$\overline{\text{RESET}}$ Output remains low while V_{CC} is below the reset threshold, and for at least 140ms after V_{CC} rises above the reset threshold.
RESET (FP6810)	RESET Output remains high while V_{CC} is below the reset threshold, and for at least 140ms after V_{CC} rises above the reset threshold.
VCC	Supply Voltage

Block Diagram

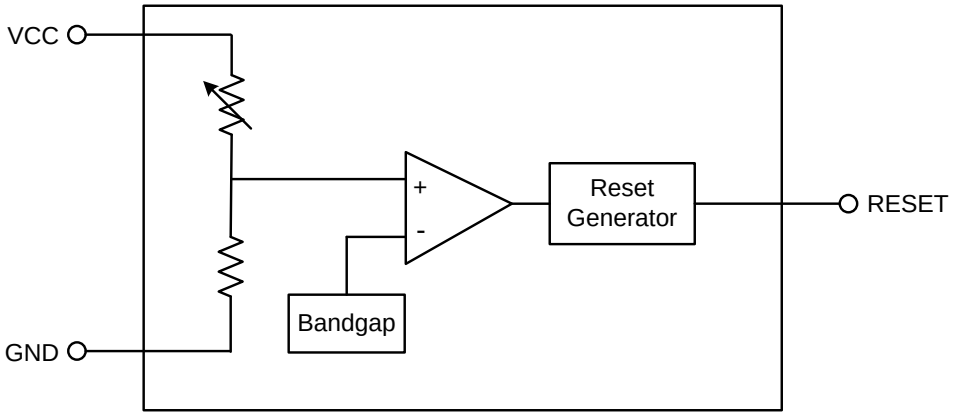


Figure 3. Block Diagram of FP6809/FP6810

Absolute Maximum Ratings

- Supply Voltage (VCC to GND) ---------- -0.3V to +6V
- RESET, $\overline{\text{RESET}}$ Voltage (Push-Pull) ---------- -0.3 to (Vcc+0.3V)
- $\overline{\text{RESET}}$ Voltage (Open Drain) ---------- -0.3V to (Vcc+0.3V)
- Input Current, VCC ---------- 20mA
- Output Current, RESET, $\overline{\text{RESET}}$ ---------- 20mA
- Rate of Rise (VCC) ---------- 100V/μs
- Power Dissipation @T_A=25°C, SOT-23-3 (P_D) ---------- +0.4W
- Package Junction-to-Case Thermal Resistance SOT-23-3 (θ_{Jc}) ---------- +150°C/W
- Package Thermal Resistance SOT-23-3 (θ_{JA}) ---------- +250°C/W
- Maximum Junction Temperature (T_J) ---------- +150°C
- Storage Temperature (T_S) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10s) (T_{LEAD}) ---------- +260°C

Note 2：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage (VCC to GND) ---------- +1.0V to +5.5V
- Operation Temperature Range ---------- -40°C to +85°C

Electrical Characteristics

(V_{CC}=full range, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
VCC Range	V_{CC}		1.0		5.5	V
Supply Current	I_{CC}	V_{CC}<5.5V, FP68__-46/44/40		3		µA
		V_{CC}<3.6V, FP68__-23/26/29/31		3		
Reset Threshold	V_{TH}	FP6809-46/ FP6810-46	4.54	4.63	4.72	V
		FP6809-44/ FP6810-44	4.29	4.38	4.47	
		FP6809-40/ FP6810-40	3.92	4.00	4.08	
		FP6809-31/ FP6810-31	3.02	3.08	3.14	
		FP6809-29/ FP6810-29	2.87	2.93	2.99	
		FP6809-26/ FP6810-26	2.58	2.63	2.68	
		FP6809-23/ FP6810-23	2.27	2.32	2.37	
Reset Threshold T.C. (Note3)				30		ppm/°C
VCC to Reset Delay (Note3)		V_{CC}=V_{TH} to (Vth-100mV)		20		µs
Reset Active Timeout Period			140	240	560	ms
$\overline{\text{RESET}}$ Output Voltage Low (Push-Pull Active Low and Open-Drain Active Low, FP6809)	V_{OL}	V_{CC}=V_{TH} min, I_{SINK}=1.2mA, FP6809-23/26/29/31			0.3	V
		V_{CC}=V_{TH} min, I_{SINK}=3.2mA, FP6809-44/46			0.4	
		V_{CC}>1.0V, I_{SINK}=50µA			0.3	
RESET Output Voltage Low (Push-Pull Active High, FP6810)	V_{OL}	V_{CC}=V_{TH} max, I_{SINK}=1.2mA, FP6809-23/26/29/31			0.3	V
		V_{CC}=V_{TH} max, I_{SINK}=3.2mA, FP6809-44/46			0.4	
$\overline{\text{RESET}}$ Output Voltage High (Push-Pull Active Low, FP6809)	V_{OH}	V_{CC}>V_{TH} max, I_{SOURCE}=500µA, FP6809-23/26/29/31	0.8Vcc			V
		V_{CC}>V_{TH} max, I_{SOURCE}=800µA, FP6809-44/46	Vcc-1.5			
RESET Output Voltage High (Push-Pull Active High, FP6810)	V_{OH}	1.8V<V_{CC}<V_{TH} Min, I_{SOURCE}=150µA	0.8Vcc			V
$\overline{\text{RESET}}$ Open-Drain Output Leakage Current (FP6809-N)		V_{CC}>V_{TH}, RESET deasserted			1	µA

Note 3：The specification is guaranteed by design, not production tested.

Typical Performance Curves

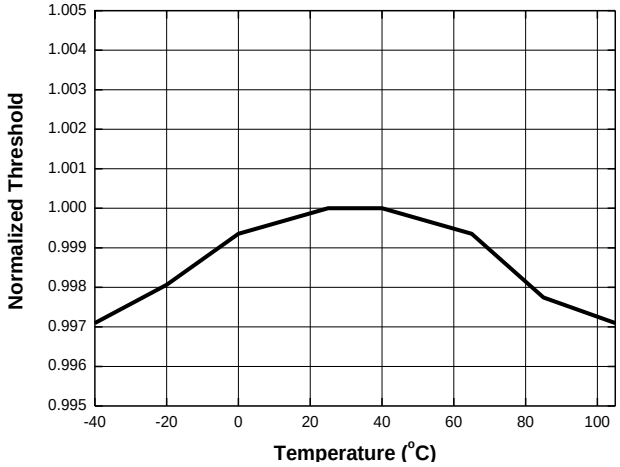


Figure 4. Normalized Reset Threshold vs. Temperature

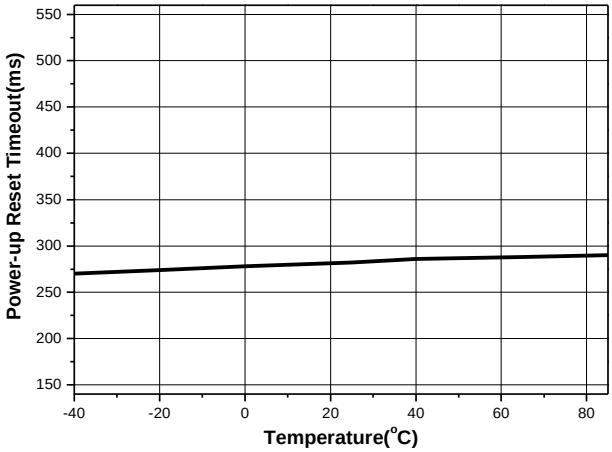


Figure 5. Power-up Timeout vs. Temperature

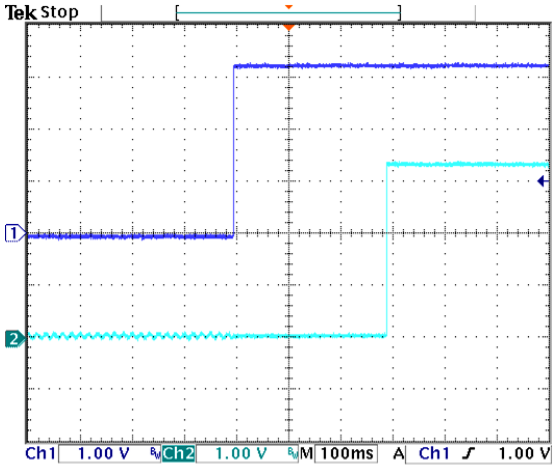


Figure 6. Power-Up $\overline{\text{RESET}}$ Timeout Waveforms;
CH1：VCC CH2：$\overline{\text{RESET}}$

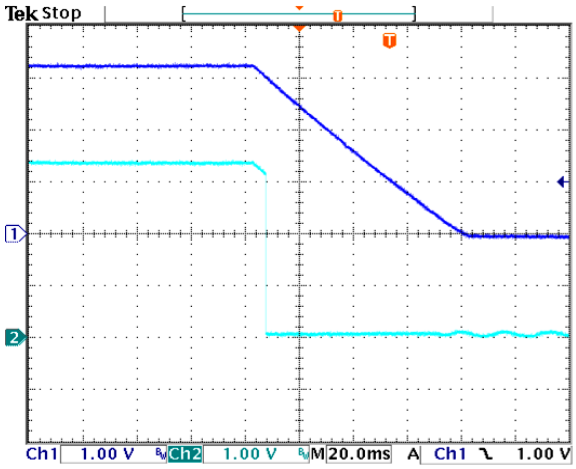


Figure 7. Power-Down $\overline{\text{RESET}}$ Delay Waveforms;
CH1：VCC CH2：$\overline{\text{RESET}}$

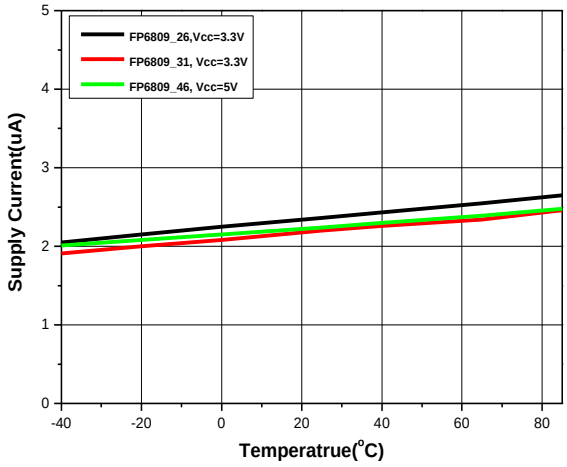


Figure 8. Supply Current vs. Temperature

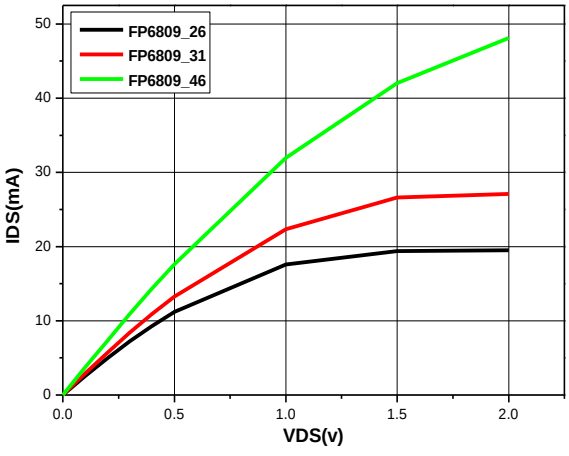


Figure 9. Output Sinking Capability

Typical Performance Curves (Continued)

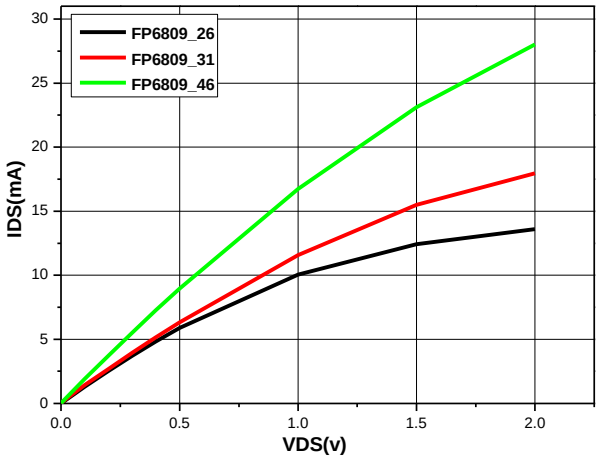


Figure 10. Output Sourcing Capability

Application Information

The FP6809/FP6810 are supervisory circuits, monitoring critical voltages and asserting reset signal to the subsequent devices. The reset signal can start the microprocessor in a known state, avoiding code- execution errors during power-up, power-down, or brownout conditions. $\overline{\text{RESET}}$(RESET) is guaranteed to be a logic low (high) for $V_{TH}>V_{CC}>0.9V$. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{\text{RESET}}$(RESET) low (high) for the reset timeout. After this period, $\overline{\text{RESET}}$(RESET) goes high (low). If V_{CC} falls below the reset threshold, $\overline{\text{RESET}}$(RESET) goes low (high) immediately.

Whenever V_{CC} drops below V_{TH}, the internal timer resets to zero and $\overline{\text{RESET}}$ (RESET) goes low (high). The internal timer keeps activated only when $V_{CC}> V_{TH}$, and $\overline{\text{RESET}}$(RESET) remains low (high) for the reset timeout interval.

Negative-Going V_{CC} Transients

In addition to issuing a reset to microprocessor during power-up, power-down, and brownout conditions, FP6809/FP6810 are relatively immune to short-duration negative-going V_{CC} transients (glitches). Figure 11 shows typical transient duration vs. reset comparator overdrive, for which the FP6809/ FP6810 do not generate a reset signal. The graph was generated using a negative-going pulse applied to V_{CC}, as shown in Figure 12, starting 0.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width a negative-going V_{CC} transient can have without causing a reset signal. As the reset comparator overdrive increases, the maximum allowable pulse width decreases. A typical 0.1µF bypass capacitor mounted as close as possible to the VCC pin provides additional transient immunity.

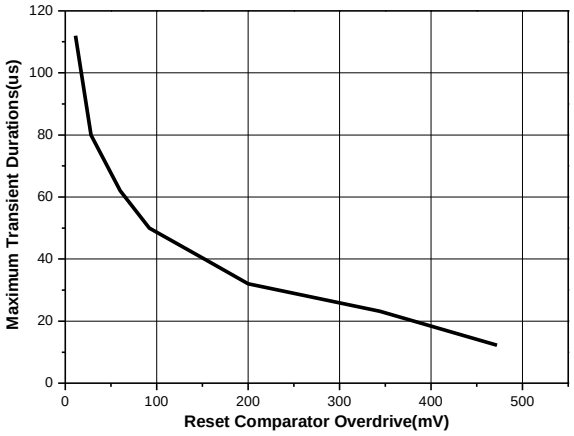


Figure 11. Maximum Transient Durations Without Causing a Reset Pulse vs. Reset Comparator Overdrive

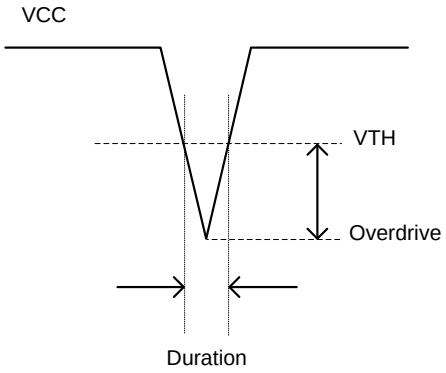


Figure 12. The VCC with Negative Going Transients

Application Information (Continued)

Benefits of Highly Accurate Reset Threshold

Most microprocessor supervisor ICs have reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when supply is 10% below nominal. In other words, the reset is guaranteed to assert after the power supply falls out of regulation, but keeps inactive even when power is at the minimum specified operating voltage of the system ICs.

Ensuring a Valid Reset Output Down to V_{CC}=0

When V_{CC} falls below 1V, the FP6809 no longer sinks current, it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to RESET can drift to undetermined voltages. This presents no problem in most applications for microprocessor's inoperative condition with V_{CC} below 1V. However, in applications where RESET must be valid down to 0V, adding a pull-down resistor to RESET causes stray leakage currents to flow to ground, providing some impedance between RESET and ground (Figure 13). R1 is recommended around 100kΩ.

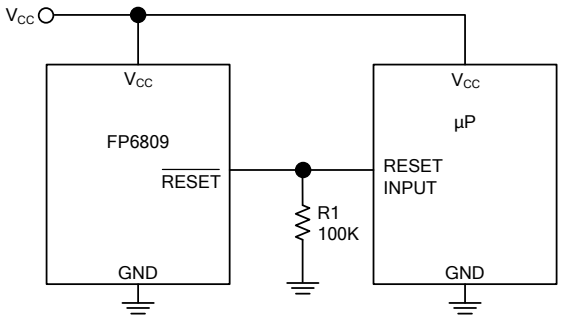


Figure 13. $\overline{\text{RESET}}$ Valid to V_{CC}=0V Circuit

A 100kΩ pull-up resistor to V_{CC} is also recommended for FP6810 if RESET is required to remain valid for V_{CC}<1V.

Interfacing to µPs with Bidirectional Reset Pins

Since the RESET output of FP6809N is open drain, this device interfaces easily with µP that has bidirectional reset pins. Connect the FP6809N's RESET output directly to the microcontroller's RESET pin with a single pull-up resistor allows either device to assert reset (Figure 14).

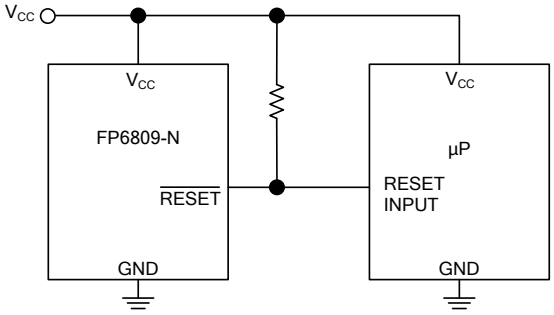
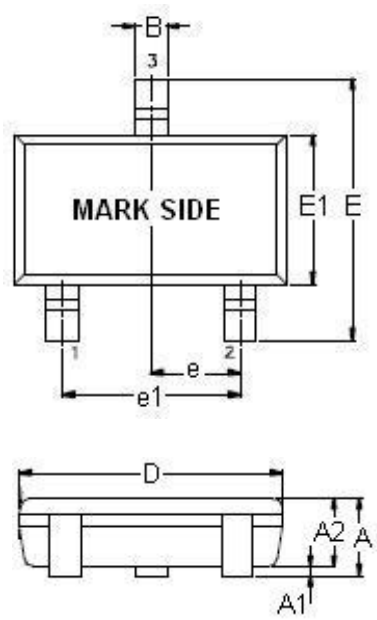
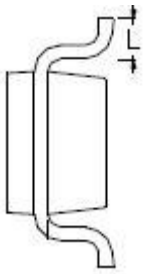


Figure14. Interfacing to µPs with Bidirectional Reset I/O

Outline Information

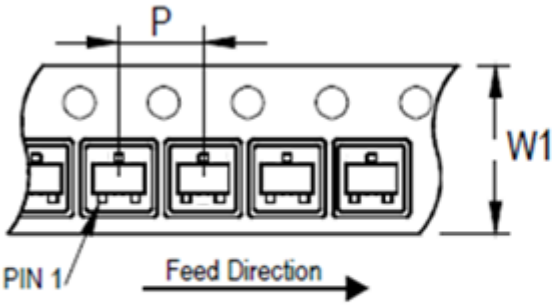
SOT-23-3 Package (Unit: mm)

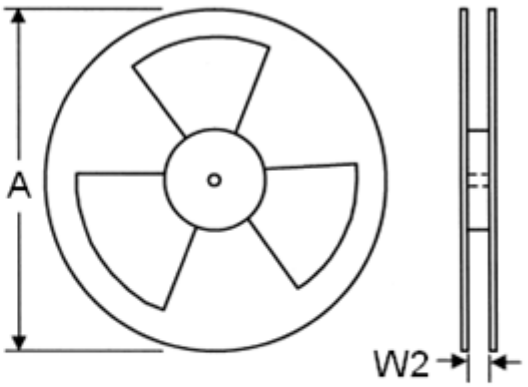




SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.30	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.30	0.60

Carrier Dimensions





Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

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