MT5931 Data Sheet

Version: 0.12
Release date: 2011-07-29

Document Revision History

Revision	Date	Author	Description
0.01	2011/03/28	SC Yin	First formal release
0.02	2011/06/29	SC Yin	For initial release
0.1	2011/07/04	SC Yin	For Preliminary release
0.11	2011/07/22	RenYu	Fix pin assignment
0.12	2011/07/29	JackyChou	Update TFBGA POD information

Table of Contents

1 System overview

1.1 General description

MT5931 is a WiFi device which includes

- 802.11 bgn
- PA
- LNA
- TRSW

MT5931 provides the best and most convenient connectivity functions. MT5931 implements advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. Enhanced overall quality for simultaneous voice, data, and audio/video transmission on mobile phone and Tablet PC can be achieved. The small size with low power consumption reduces PCB layout area. The software package enables all advanced wireless features on Android OS.

1.2 Features

- Embedded single core CPU for better system level management and offload host resource.
- Coexistence: IEEE 802.15.2 external three-wire coexistence scheme to support additional wireless technologies such as 3G, GPS and WiMAX
- Self Calibration.
- Integrated switching regulator enables direct connection to battery
- Best-in-class current consumption performance
- OS support: Android, Windows Mobile, Linux, Symbian
- Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (for example, transmit window and duration that take into account of protocol exchange sequence, frequency, etc.)
- TFBGA(5.1x5.3mm^2) and WLCSP(2.93x3.17mm^2) packages
- 2.4GHz single stream 802.11 b/g/n MAC/BB/RF
- 802.11 d/h/k compliant
- Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (Hardware)
- QoS: WFA WMM, WMM PS
- Support 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
- Support 802.11w Protected Managed Frames
- Support WiFi Direct (WFA P-2-P standard)
- Interface: SDIO 2.0 (4-bit & 1-bit), SPI , EHPI-8 / 16
- Per packet Tx power control

1.3 Applications

- Smart Phone applications
- Tablet PC applications
- Mobile Internet Device (MID) applications

- Portable Navigation Device (PND) applications
- Portable Media Player (PMP) applications
- Portable Gaming Device

1.4 Block diagram

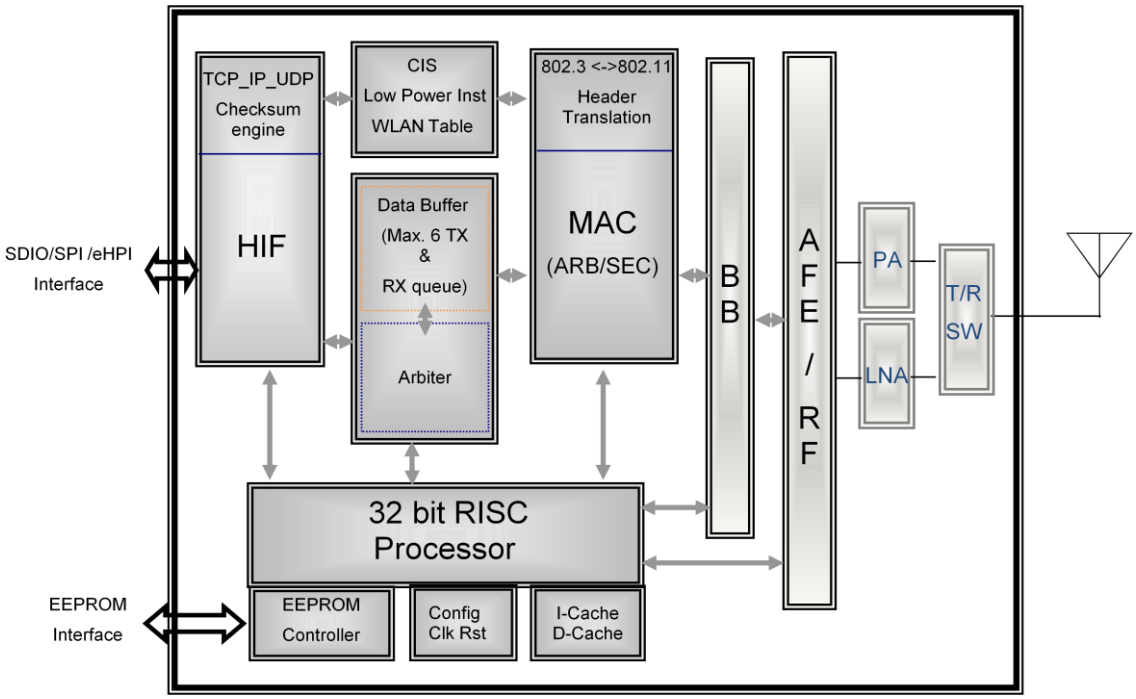


Figure 1 MT5931 block diagram

2 Product description

2.1 Pin description

Symbol	WLCSP bump	TFBGA ball	Description	PU/PD	I/O
Power Ground Pin					
CGND	F6	F4	Ground	NA	VSS
CGND	G6	F6	Ground	NA	VSS
PAD_VDDK	E5	G4	1.2V core power	NA	VDD
PAD_VDDK		G6	1.2V core power	NA	VDD
PAD_VDDK		G7	1.2V core power	NA	VDD
DVDDIO3	G1	H1	1.8/2.8V Host interface I/O power	NA	VDD
CGND		F7	Ground	NA	VSS
CGND		K1	Ground	NA	VSS
DVDDIO0	F3	K10	1.8 / 2.8V I/O power	NA	VDD
DVDDIO2		J7	1.8/2.8V Host interface or PTA I/O power	NA	VDD
DVDDIO1		K7	1.8/2.8V PTA I/O power	NA	VDD
PMU					
GND_REF	B7	B1	Ground	NA	
OUT_FB	C7	C3	Buck feedback	NA	
AVDD16_CLDO	C8	C2	CLDO feedback	NA	
CLDO	B8	C1	CLDO 1.2V output	NA	
REF	A8	A1	Bandgap reference point	NA	
AVDD43_REF	A7	A2	4.3V reference point	NA	
AGND43_SMPS	B5	B3	Ground	NA	
LXBK	A6	A3	Buck feedback	NA	
AVDD43_SMPS	B5	A4	Buck power	NA	
PALDO	A5	A5	PALDO output	NA	
GND_PALDO	C5	C5	Ground	NA	
PALDO_FB	C6	E5	PALDO remote sense feedback	NA	
PAD_EN	D7	B5	PMU enable from host	NA	I
RTC					
X32K_IN	D5	D1	RTC 32K Hz clock input	NA	I
AVDDRTC		D3	RTC Power	NA	VDD
AVSSRTC		D4	RTC ground	NA	VSS

Symbol	WLCSP bump	TFBGA ball	Description	PU/PD	I/O
X32K_OUT		D2	RTC 32K output	NA	O
RF					
AVDD33_XO	C4	A6	XO power	NA	VDD
PAD_ICAL_EXTR		F10	External ICAL input	NA	I
TRX_QN		E9	TRX Q signal	NA	I/O
TRX_QP		E8	TRX Q signal	NA	I/O
TRX_IN		E7	TRX I signal	NA	I/O
TRX_IP		E6	TRX I signal	NA	I/O
AVDD16_LF	D1	E10	LF power	NA	VDD
AVSS16_WF	C2	D6	Ground	NA	VSS
AVSS16_WF	D2	D7	Ground	NA	VSS
AVDD16_TRX	C1	D10	TRX power	NA	VDD
AVSS16_WF	B3	D9	Ground	NA	VSS
TRX_IO_N		C10	TRX IO signal	NA	I/O
AVSS33_PA	A2	A10	Ground	NA	VSS
AVSS33_PA	B2	B9	Ground	NA	VSS
TRX_IO_P		B10	TRX IO signal	NA	I/O
AVDD33_TX	A3	A9	WLAN power	NA	VDD
AVSS33_PA		C9	Ground	NA	VSS
AVSS16_VCO		B8	Ground	NA	VSS
AVDD16_SX	C3	A8	SX power	NA	VDD
AVSS16_WF		C6	Ground	NA	VSS
OSC_IN	A4	A7	XTAL / OSC input	NA	I
Digital					
FSOURCE	F7	E1	eFuse power pin.	NA	VDD
WIFI_INT_B	F5	E2	WIFI_INT_B: WIFI component interrupt output	PU	O
D15		J6	eHPI_DAT15: eHPI data bus bit 15	None/SW	I/O
			WX_REQ: WiMAX co-existence PTA interface	None/SW	I
D14		J5	eHPI_DAT14: eHPI data bus bit 14	None/SW	I/O
			WX_INFO: WiMAX co-existence PTA interface	None/SW	I
D13		K6	eHPI_DAT13: eHPI data bus bit 13	None/SW	I/O
			WX_NO_GRANT:	None/SW	O

Symbol	WLCSP bump	TFBGA ball	Description	PU/PD	I/O
			WiMAX co-existence PTA interface		
D12		H6	eHPI_DAT12: eHPI data bus bit 12	None/SW	I/O
			BT_FREQ: BT co-existence PTA interface	None/SW	I
D11		H5	eHPI_DAT11: eHPI data bus bit 11	None/SW	I/O
			BT_ACT: BT co-existence PTA interface	None/SW	I
D10		H4	eHPI_DAT10: eHPI data bus bit 10	None/SW	I/O
			WLAN_ACT: BT co-existence PTA interface	None/SW	O
D9		J4	eHPI_DAT9: eHPI data bus bit 9	None/SW	I/O
			GPIO0_16: GPIO0_16 in / out	None/SW	I/O
D8		K4	eHPI_DAT8: eHPI data bus bit 8	None/SW	I/O
			GPIO0_17: GPIO0_17 in / out	None/SW	I/O
D7		E3	eHPI_DAT7: eHPI data bus bit 7	None/SW	I/O
			EEDO: EEPROM interface	None/SW	I
			GPIO0_18: GPIO0_18 in / out	None/SW	I/O
D6		G3	eHPI_DAT6: eHPI data bus bit 6	None/SW	I/O
			EEDI: EEPROM interface	None/SW	O
			GPIO0_19: GPIO0_19 in / out	None/SW	I/O
D5		G2	eHPI_DAT5: eHPI data bus bit 5	None/SW	I/O
			EECS: EEPROM interface	None/SW	O

Symbol	WLCSP bump	TFBGA ball	Description	PU/PD	I/O
			GPIO0_20: GPIO0_20 in / out	None/SW	I/O
D4		G1	eHPI_DAT4: eHPI data bus bit 4	None/SW	I/O
			EESK: EEPROM interface	None/SW	O
			GPIO0_21: GPIO0_21 in / out	None/SW	I/O
D3	E8	K2	eHPI_DAT3: eHPI data bus bit 3	None/SW	I/O
			SDIO_DAT3: SDIO data bus bit 3	PU	I/O
			GPIO0_22: GPIO0_22 in / out	None/SW	I/O
D2	E7	H2	eHPI_DAT2: eHPI data bus bit 2	None/SW	I/O
			SDIO_DAT2: SDIO data bus bit 2	None/SW	I/O
			GPIO0_23: GPIO0_23 in / out	None/SW	I/O
D1	E6	J3	eHPI_DAT1: eHPI data bus bit 1	None/SW	I/O
			SDIO_DAT1: SDIO data bus bit 1	None/SW	I/O
			GPIO0_24: GPIO0_24 in / out	None/SW	I/O
D0	G7	H3	eHPI_DAT0: eHPI data bus bit 1	None/SW	I/O
			SDIO_DAT0: SDIO data bus bit 1	None/SW	I/O
			SPI_DIN: SPI interface DIN	None/SW	I
A0	F8	J1	eHPI_A0: eHPI interface A0	None/SW	I
			SDIO_CMD: SDIO interface CMD	None/SW	I/O
			SPI_DOUT: SPI interface DOUT	None/SW	O
CS_N		F3	eHPI_CSN: eHPI interface CS_N	None/SW	I
			GPIO0_27: GPIO0_27 in/out	None/SW	I/O

Symbol	WLCSP bump	TFBGA ball	Description	PU/PD	I/O
			SPI_CS: SPI interface CS	None/SW	I
WE_N		F2	eHPI_WEN: eHPI interface WE_N	None/SW	I
			GPIO0_28: GPIO0_28 in/out	None/SW	I/O
			SPI_MODE_SEL: SPI interface MODE_SEL	None/SW	I
OE_N	G8	J2	eHPI_OEN: eHPI interface OE_N	None/SW	I
			SDIO_CLK: SDIO interface SD_CLK	None/SW	I
			SPI_CLK: SPI interface SPI_CLK	None/SW	I
RF_I_CAL	D4		RF_I_CAL: Analog pin	NA	I
			OSC_EN: OSC enable in co-clocking platform	None/SW	O
			ICAP_TRIG_EXT: External trigger event for internal capture debugging	None/SW	I
OSC_EN		F9	OSC_EN: OSC enable in co-clocking platform	None/SW	O
			ICAP_TRIG_EXT: External trigger event for internal capture debugging	None/SW	I
GPIO_0		G10	ANTSEL_0: Antenna selection #0	PD	O
			UART_DBG_RX: UART debug RXD	None/SW	I
			GPIO0_8: GPIO0_8 in/out	None/SW	I/O
GPIO_1		H9	ANTSEL_1: Antenna selection #1	PD	O
			UART_DBG_TX: UART debug TXD	None/SW	O
			GPIO0_0: GPIO0_0	None/SW	I/O

Symbol	WLCSP bump	TFBGA ball	Description	PU/PD	I/O
			in/out		
BT_PRI	G4	H7	BT_PRI: BT co-existence PTA interface	None/SW	I/O
			GPIO0_9: GPIO0_9 in/out	None/SW	I/O
ANTSEL_0	G2	K8	ATNSEL_0: Antenna selection #0	PD	O
			MCU_DBGACKN: JTAG interface	None/SW	O
ANTSEL_1	G3	J8	ATNSEL_1: Antenna selection #1	PU	O
			MCU_JTDO: JTAG interface	None/SW	O
ANTSEL_2	E1	G9	EESK: EEPROM interface	PD	O
			WLAN_ACT: BT co-existence PTA interface	None/SW	O
			MCU_DBGIN: JTAG interface	None/SW	I
ANTSEL_3	E2	F8	EEDI: EEPROM interface	PD	O
			GPIO0_7: GPIO0_7 in/out	None/SW	I/O
			MCU_JTMS: JTAG interface	None/SW	I
UART_DBG_TX	E3	J10	EECS: EEPROM interface	None/SW	O
			UART_DBG_TX: UART debug TXD	None/SW	O
			MCU_JTRST_B: JTAG interface	None/SW	I
UART_DBG_RX	F1	H10	EEDO: EEPROM	None/SW	I

Symbol	WLCSP bump	TFBGA ball	Description	PU/PD	I/O
			interface		
			UART_DBG_RX: UART debug RXD	None/SW	I
			MCU_JTCK: JTAG interface	None/SW	I
EXT_INT_B	F2	H8	ICAP_TRIG_EXT: External trigger event for internal capture debugging	None/SW	I
			WLAN_ACT: BT co-existence PTA interface	None/SW	O
			EXT_INT_B: External interrupt input from Host	None/SW	I
			MCU_JTDI: JTAG interface	PD/SW	I
XTEST	F4	J9	Test mode enable	PD	I
SYSRST_B	E4	K9	External system reset active low	PU	I

Table 1 Pin description

2.1.1 Strapping Table

XTAL_SEL[0] 【ANTSEL_0】	XTAL_SEL[1] 【ANTSEL_1】	XTAL_SEL[2] 【GPIO_1】	Description
0	0	0	24MHz
1	0	0	19.2MHz
0	1	0	26MHz (default)
1	1	0	38.4MHz
0	0	1	Reserved
1	0	1	52MHz
0	1	1	40MHz
1	1	1	Reserved

Table 2 OSC/XTAL frequency selection

SLOW_SRC 【GPIO_0】	Note
1	Internal
0	External

Table 3 Slow Clock source selection

OSC_SRC 【WIFI_INT_B】	Note
0	OSC / Co-clocking
1	XTAL

Table 4 Clock source selection

HOST[0] 【ANTSEL_2】	HOST[1] 【ANTSEL_3】	Note
0	0	eHPI-8
1	0	eHPI-16
0	1	SPI
1	1	SDIO

Table 5 Host interface selection

2.2 Package information

2.2.1 TFBGA packaging

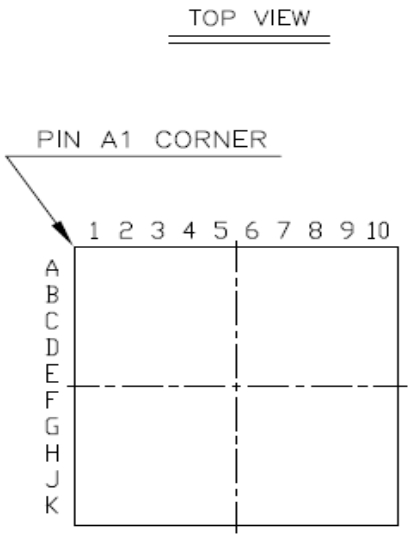


Figure 2 MT5931 TFBGA top marking

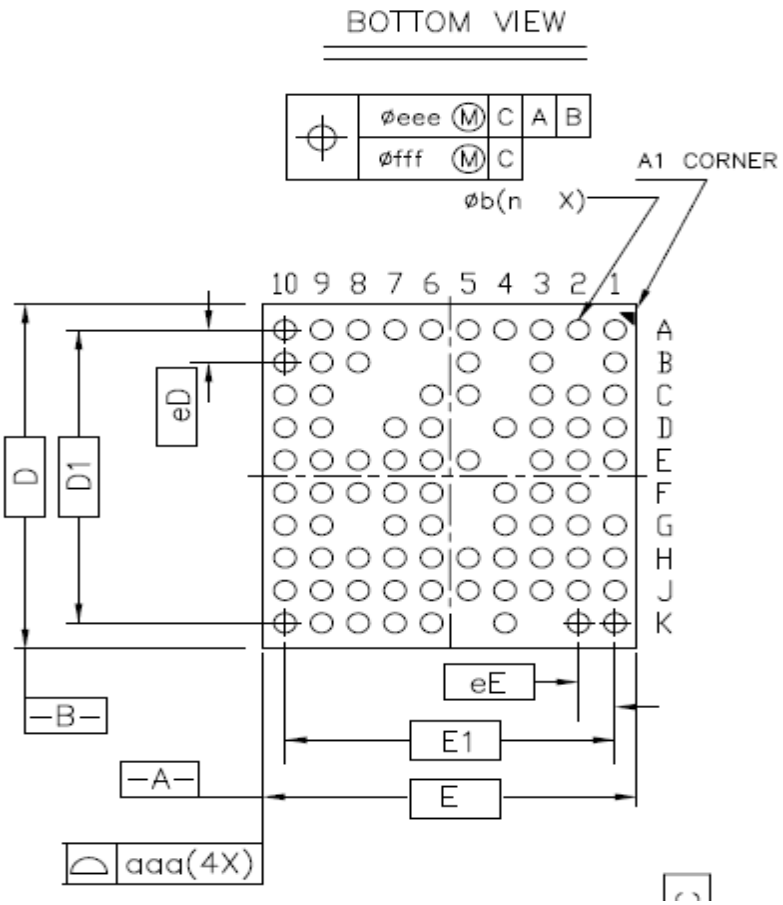
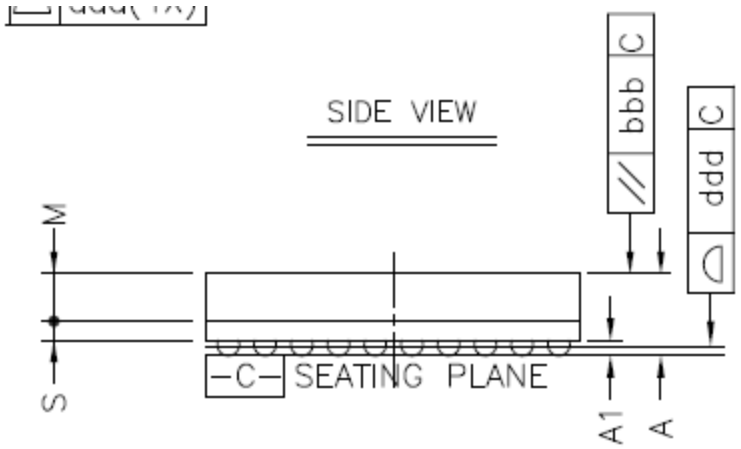


Figure 3 MT5931 TFBGA POD (a)



		Symbol	Common Dimensions
Package :			TFBGA
Body Size:	X	E	5.100
	Y	D	5.300
Ball Pitch :	X	eE	0.500
	Y	eD	0.500
Total Thickness :		A	1.200 MAX.
Ball Diameter :			0.300
Stand Off :		A1	0.160 ~ 0.260
Ball Width :		b	0.250 ~ 0.350
Package Edge Tolerance :		aaa	0.100
Mold Flatness :		bbb	0.100
Coplanarity:		ddd	0.080
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.050
Ball Count :		n	84
Edge Ball Center to Center :	X	E1	4.500
	Y	D1	4.500

Figure 4 MT5931 TFBGA POD (b)

2.2.2 WLCSP packaging

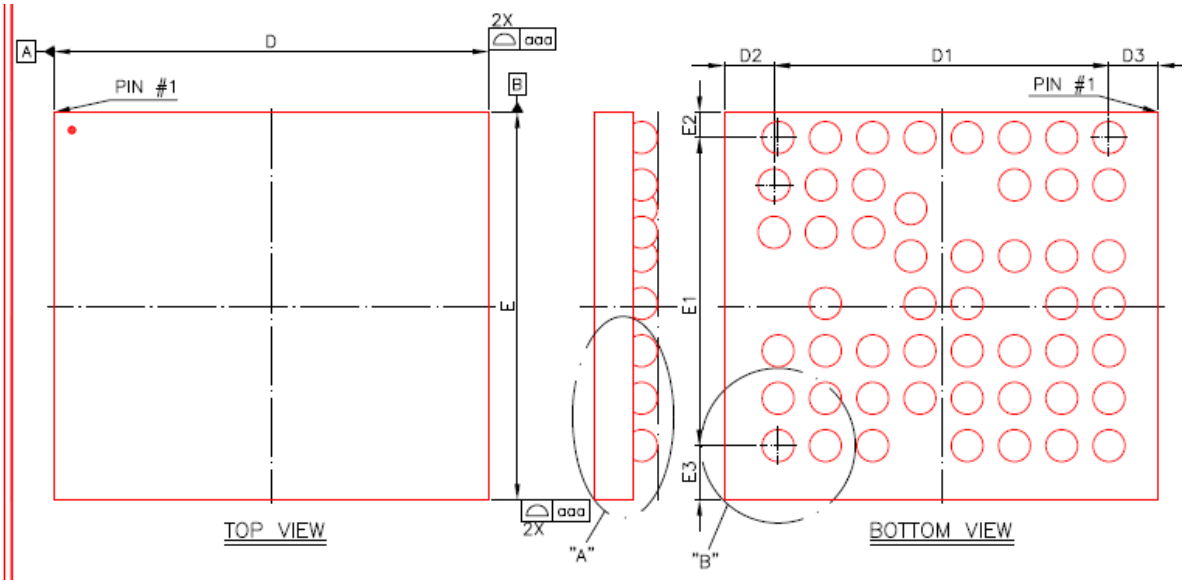


Figure 5 MT5931 WLCSP marking

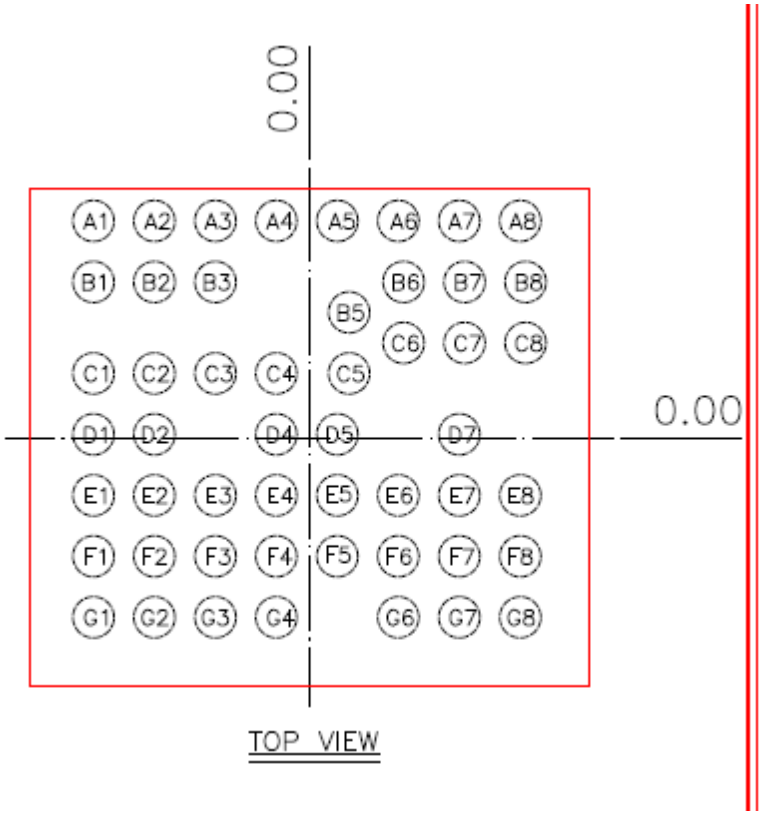


Figure 6 MT5931 WLCSP POD (a)

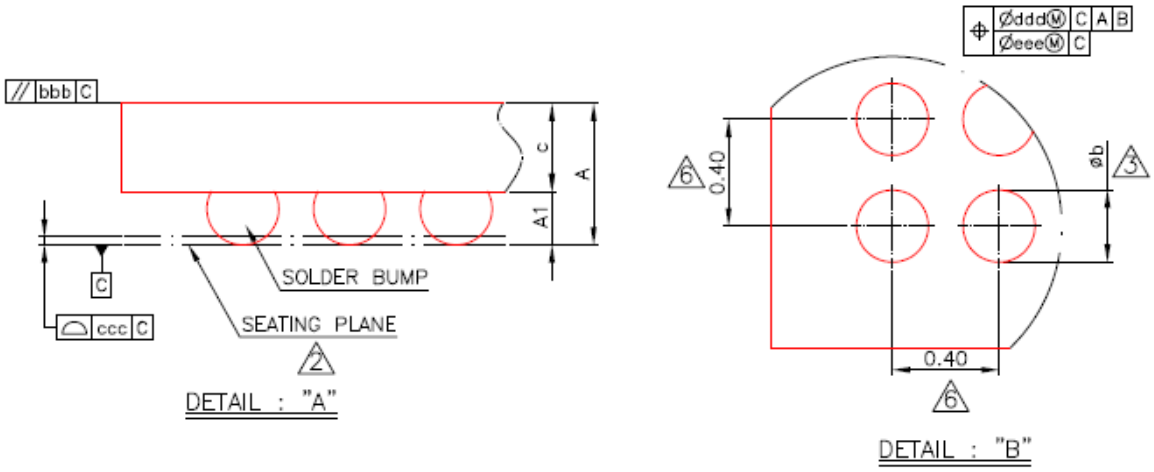


Figure 7 MT5931 WLCSP POD (b)

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.490	0.530	0.571	0.019	0.021	0.022
A1	0.185	0.200	0.215	0.007	0.008	0.008
c	0.305	0.330	0.356	0.012	0.013	0.014
D	3.620	3.675	3.700	0.143	0.145	0.146
E	3.175	3.270	3.295	0.125	0.129	0.130
D1	---	2.8348	---	---	0.1116	---
D2	---	0.4215	---	---	0.0166	---
D3	---	0.4187	---	---	0.0165	---
E1	---	2.6000	---	---	0.1024	---
E2	---	0.2130	---	---	0.0084	---
E3	---	0.4570	---	---	0.0180	---
b	0.216	0.270	0.324	0.009	0.011	0.013
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.03			0.001		
ddd	0.15			0.006		
eee	0.05			0.002		

Figure 8 MT5931 WLCSP POD (c)

3 Electrical characteristics

3.1 PMU description

The MT5931 has integrated Power Management Unit (PMU) which generates the power supplies required by the internal circuitry from the battery.

The PMU mainly contains Low Dropout Regulators (LDOs), buck converter and control circuits such as Under-Voltage Lockout (UVLO), thermal protection and power-on/off sequencer.

3.1.1 PALDO

The PALDO converts the battery input to a 3.3V supply for the use of WiFi RF PA circuits. It's optimized for the given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection, and output noise.

3.1.2 CLDO

One CLDO is integrated in PMU to supply digital core. It converts 1.8V input to 1.2V output which is suited for the digital circuits. The input is typically connected to the buck's output.

3.1.3 Buck converter

The regulator is a DC-DC step-down converter (Buck converter) which produce a programmable power supply from the battery input. Typically it supplies the power for the core LDO and the RF circuits. The buck converter is optimized for high efficiency, low EMI, and low quiescent current.

3.1.4 Power management control

The PMU host the power-on/off control of MT5931.

- Under-Voltage Lockout (UVLO)

  The UVLO state in the PMU prevents startup if the initial voltage of the main battery is below the pre-defined threshold. It ensures that MT5931 is powered-on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which can make the power-on sequence smoothly. In addition, when the battery voltage is getting lower and lower, it will enter UVLO state and the PMU will be turned-off automatically to prevent battery over-drainage.

- Thermal protection

  To prevent the abnormal behavior or chip damage due to over-temperature condition, the PMU in MT5931 senses the junction temperature (Tj) and issues the over-temperature warning when the Tj is over the pre-defined threshold. Typically all the regulators in PMU will be turned-off automatically when the over-temperature event happens.

- Power-on/off sequencer

  In normal condition without UVLO or over-temperature event, Buck converter and CLDO can be turned-on sequentially by setting EN pin to H. PMU will issue RESETB as soon as the power-on sequence is complete. After that, PALDO can be turned-on by software. Reset the EN pin will cause all regulators off.

3.1.5 PMU Power Connection

CLDO and some RF circuits are powered by the SMPS (Buck converter) output in the normal mode.

At system sleep mode, all the RF LDOs and PALDO are turned off. The voltage source of digital core LDO can be switched to VIO_HOST instead of the SMPS, which is also turned off. The power switch is integrated in the PMU.

The VIO_HOST is a power input which may be 1.8V or 2.8V from the host side. The connection structure is shown in the figure below.

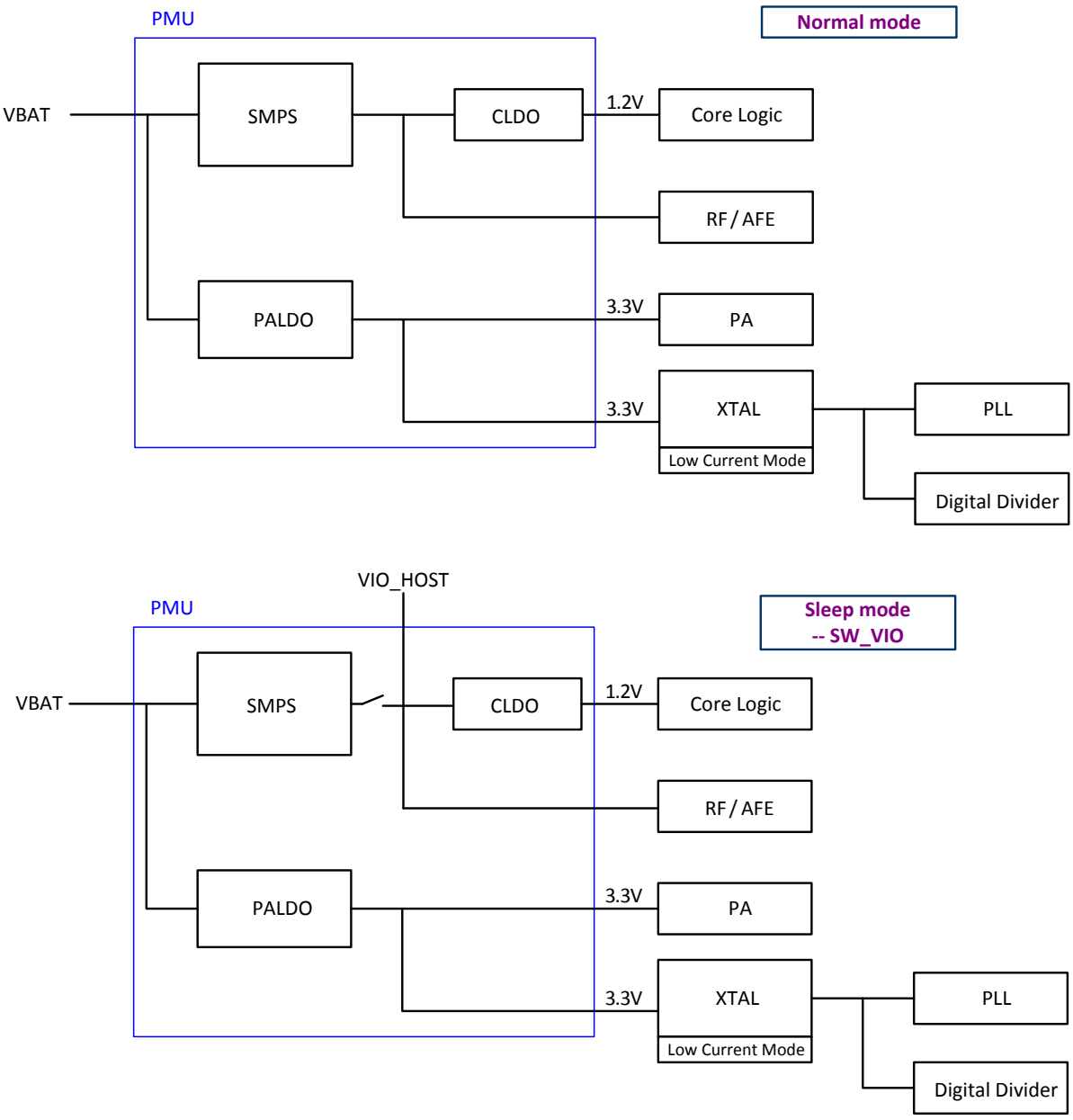


Figure 9 Normal mode and sleep mode connection

3.2 Absolute maximum ratings

SYMBOL	PARAMETER	RATING	UNIT
DVDDIO0 DVDDIO1 DVDDIO2	1.8V or 2.8 Digital Power Supply	-0.3 to 3.6	V
DVDDIO3 (VIO_HOST)	1.8V or 2.8V SDIO Digital IO Power Supply	-0.3 to 3.6	V
DVDD	Digital 1.2V Power Supply	-0.3 to 3.6	V
AVDD_CLDO	Internal CLDO Power Supply	-0.3 to 3.6	V
AVDD28_* AVDD33_*	RF power supply	-0.3 to 3.6	V
AVDD13_*	RF power supply	-0.3 to 1.8	V
AVDD_SMPS	BUCK and PALDO power supply	-0.3 to 4.7	V
AVDD_MISC	PMU power supply	-0.3 to 4.7	V
T_{STG}	Storage Temperature	-60 to +150	°C
T_A	Operating Temperature	-45 to +85	°C

Table 3 Absolute maximum ratings

3.3 Recommended operating range

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
DVDDIO0 DVDDIO1 DVDDIO2 DVDDIO3	2.8V Digital Power Supply	2.0	2.8	3.6	V
	1.8V Digital Power Supply	1.6	1.8	2.0	V
DVDD	Digital Core Power Supply	1.08	1.2	1.32	V
AVDD13_*	RF power supply	1.28	1.35	1.4	V
AVDD28_*	RF power supply	2.66	2.8	2.94	V
AVDD33_*	RF power supply	3.14	3.3	3.46	V
AVDD_SMPS	BUCK and PALDO power supply	2.9	3.8	4.3	V
AVDD_MISC	PMU power supply	2.3	3.8	4.3	V
T_j	Commercial Junction Operating Temperature	0	25	115	°C
	Industry Junction Operating Temperature	-40	25	125	°C
T_a	Operation Temperature	-40	25	85	°C
T_{stg}	Storage Temperature	-60	25	150	°C

Table 4 Recommended operating range

3.4 PMU electrical characteristics

3.4.1 PMU characteristics

Parameter	Conditions	Min.	Typical	Max.	Unit
PMU_EN = 0: shut down current					
VBAT < 2.3V	VBAT=2.3V		TBD		µA

Parameter	Conditions	Min.	Typical	Max.	Unit
2.3V < VBAT < 4.3V	VBAT=3.8V		15	20	µA
PMU_EN = 1: quiescent current					
All outputs on	VBAT=4.2V		TBD		µA
PALDO off, CORE LDO and Buck converter on	VBAT=4.2V		TBD		µA
Under Voltage Lock-Out (UVLO)					
Under voltage rising threshold			2.25		V
Under voltage falling threshold			2.15		V
PMU_EN Voltage Level					
High Voltage		1.4			V
Low Voltage				1.0	V
Thermal Shutdown					
Threshold			150		°C
Hysteresis			40		°C
LDO Enable Response Time			250		µs

Parameter	Conditions	Min.	Typical	Max.	Unit
SMPS Voltage					
Output voltage (V_BUCK)			1.65		V
Digital Core Voltage					
Output voltage (V_D)			1.2		V
WLAN PA Voltage					
Output voltage (V_PALDO)			3.3		V

Table 5 PMU characteristics

3.5 XOSC32

3.5.1 Block description

The low-power 32-KHz crystal oscillator, XOSC32, is designed to work with an external piezoelectric 32.768 kHz crystal and a load composed of two functional capacitors, as shown in the figure below.

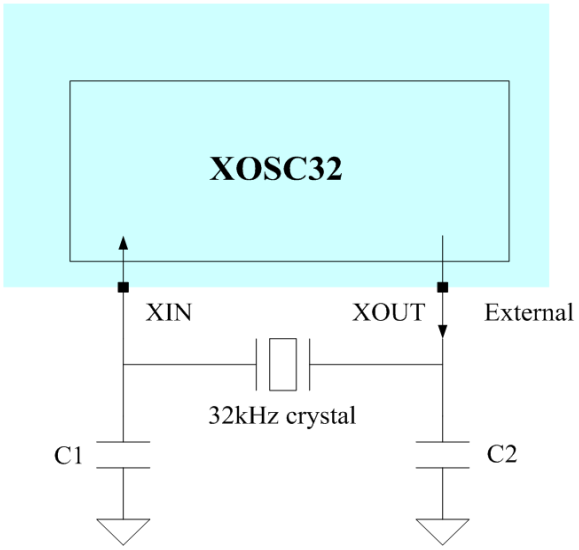


Figure 10 Block diagram of XOSC32

3.5.2 Functional specification of XOSC32

Symbol	Parameter	Min	Typical	Max.	Unit
AVDDRTC	Analog power supply	1	2.8	3	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	30	50	70	%
	Current consumption		5		μA
T	Operating temperature	-20		80	°C

Table 6 Functional specification of XOSC32

3.5.3 Recommendations for crystal parameters for XOSC32

Symbol	Parameter	Min	Typical	Max	Unit
F	Frequency range		32768		Hz
GL	Drive level			5	uW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance			50	KΩ
C0	Static capacitance			1.6	pF
CL[1]	Load capacitance	6		12.5	pF

Table 7 Recommended parameters of the 32 kHz crystal

[1] CL is the parallel combination of C1 and C2 in the block diagram.

3.6 DC electrical characteristics for 2.8 volts operation

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Low Voltage	LVTTL	-0.28	0.6	V
V_{IH}	Input High Voltage		2.0	3.08	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	LVTTL	0.68	1.36	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage		1.36	1.7	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 1.6~14 mA	-0.28	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 1.6~14 mA	2.4	VDD28 + 0.28	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

Table 8 2.8V DC description

3.7 DC electrical characteristics for 1.8 volts operation

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Lower Voltage	LVTTL	-0.18	0.4	V
V_{IH}	Input High Voltage		1.5	1.98	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	LVTTL	0.44	0.88	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage		0.88	1.1	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 1.6~14 mA	-0.18	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 1.6~14 mA	1.4	VDD18 + 0.18	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

Table 9 1.8V DC description

4 Functional description

4.1 Clock generation

There are two clock domains inside MT5931. One is the RF XTAL clock, which supports the RF and the major MODEM functions; while the other is the RTC 32.768 KHz clock, which maintains the system operation in sleep mode.

The RF XTAL is shared by all the RF and modem subsystems, and MT5931 has two options for this system clock source: One is for one-pin crystal input, and the other is for external clock source. The strap setting of WIFI_INT_B is used to select between these two alternatives. The clock source configuration is shown in the table below:

WIFI_INT_B	Description
0	External OSC (default)
1	External XTAL

Table 13 Clock source selection

MT5931 supports most widely used clock frequencies in the mobile handset, including 19.2, 24, 26, 38.4, 40 and 52MHz. The input frequencies are informed by input strapping.

The RTC clock can be an external 32.768 KHz clock from the host or it can use its own RTC XTAL/OSC. or divided from RF clock

4.2 Chip power management

4.2.1 Power saving mode

There are 3 power modes that MT5931 operates in when it is initialized: ACTIVE mode, IDLE mode, and SLEEP mode. The following are the brief introduction to each mode.

- Power off: Power supply is not enabled or PMU_EN is low.
- INIT: initial state since power on and waiting for firmware download.
- FWDL: state for firmware download
- ACTIVE: It is defined as the state that RF circuit is enabled to transmit or receive data, and the whole system is under normal operation. PLL is active and the MCU / AHB bus is alive.
- IDLE: When the firmware finishes its task and starts to wait for the next hardware trigger, it forces the hardware to enter this mode. In this mode, part of the logic circuits, like MCU, will enter low power mode. RF circuits might still be operating in idle mode.
- SLEEP: The baseband controller can determine when to enter sleep mode to turn off most circuits in MT5931. All the RF, PLL circuits are turned off. In sleep mode, the system could be awakened after the sleep time is expired or by an external wake up signal from the host controller.

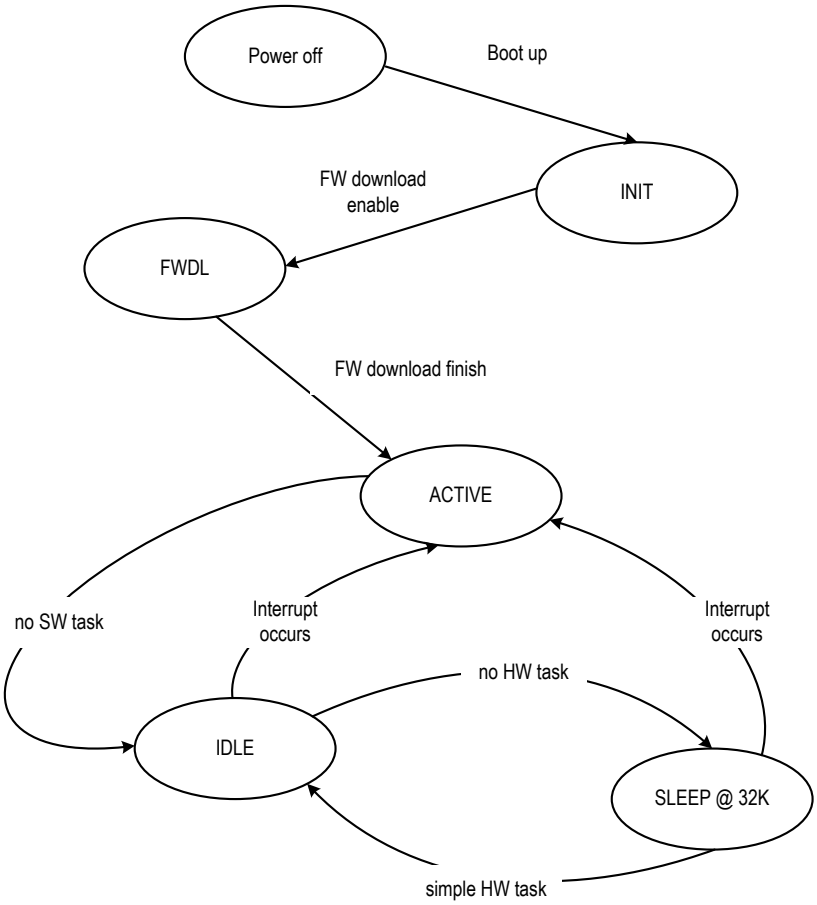


Figure 11 System power state machine

4.3 WLAN subsystem

The MT5931 WLAN is designed to support IEEE 802.11™ a/b/g/n single stream with the state-of-the-art design techniques and process technology to achieve low power consumption and high throughput performance to address the requirement of mobile devices. The MT5931 WLAN low power function uses the innovative design techniques and the optimized architecture which best utilizes the advanced process technology to reduce active and idle power, and achieve extreme low power consumption at sleep state to extend the battery life. The MT5931 WLAN TX A-MPDU function uses the state-of-the-art design technique to maximize the throughput performance while achieving the best buffer utilization at low cost. Further, the MT5931 WLAN also implements the highly sophisticated coexistence scheme to allow extremely collaborative WLAN, BT and external WiMax coexistence. As a result, the enhanced overall quality has been achieved for simultaneous voice, video, and data transmission on a mobile device.

4.3.1 MAC features

- 802.11 b/d/e/g/i/k/n/r/w
- 802.11n throughput : 35M/70Mbps for 20M/40MHz BW
- Hardware state machine controller for extreme low power consumption

- WLAN/BT/WiMAX coexistence mechanisms:
  - WLAN supports frequency domain division (FDD) mode by extensive frequency plan and interference cancellation with BT/WiMAX for optimal throughput (even in single antenna)
    - Based on the frequencies of WLAN, BT and WiMAX, WLAN adjusts its Tx power (Tx Power Control).
    - WLAN adapts its Rx path when the BT traffic is busy.
  - WLAN supports time domain division (TDD) mode by scheduling WLAN/BT/WiMAX blocks for optimal distance with acceptable throughput
    - For periodic BT or WiMAX traffic, like SCO, WLAN supports the following enhancement.
      - WLAN schedules all traffic in BT or WiMAX idle period.
      - WLAN supports channel protection to prevent rate-down when BT or WiMAX is busy.
  - WLAN supports time domain division (TDD) mode by PTA (Packet Traffic Arbiter) with BT and external device, like WiMAX.
- 802.11n optional features
  - A-MPDU TX
    - Up to 8 simultaneous links
    - Up to 16 MPDUs A-MPDU
    - TX window size up to 64 (maximum)
    - MMSS full support (0~16 us)
    - Instantly releasing the acknowledged MPDUs data buffer to achieve perfect data buffer utilization
    - Instantly aggregation for not acknowledged retry MPDUs and outstanding MPDUs within SIFS to achieve A-MPDU burst for best throughput performance
    - BAR for life time out to help RX side re-ordering buffer early releasing
  - TXOP protection and truncation
  - Reverse Direction
  - Link Adaptation (MCS Feedback)
  - PCO
  - RIFS TX/RX
  - PSMP
- AP/STA/ad-hoc mode
- Up to 20 peers for Direct Link or ad-hoc mode
- Up to 32 multicast addresses
- Rate adaption mechanism

- Hardware WAPI
- CCX5
- WFA Wi-Fi certification
  - WPA
  - WPA2
  - WMM
  - WMM PS
  - WPS 1.0 and 2.0
  - VoWiFi-Personal
  - VoWiFi-Enterrise
  - WiFi P2P
    - Group Owner Basic
    - Group Owner 11n
    - Group Client Basic
    - Coexistence of P2P and BT-over-WLAN
  - PMF
- BT-over-WLAN
  - QoS(WMM) Support
  - Supplicant of PSK engine
  - Coexistence of concurrent
- MSFT certification
  - CETK
  - LTK

4.3.2 PHY features

- Supports 802.11b, 11g, and 802.11n 1T1R
- Supports Short GI and Green Field modes in TX and RX
- Supports STBC in RX mode
- Supports 40MHz and 20MHz BW
- Enhanced and robust sensitivity for wider coverage range
- Improved performance in presence of signal tone interference and Bluetooth interference
- Supports calibration algorithm to handle no-idealities effects from CMOS RF block

4.4 BT / WLAN / Multi Radio co-existence interface

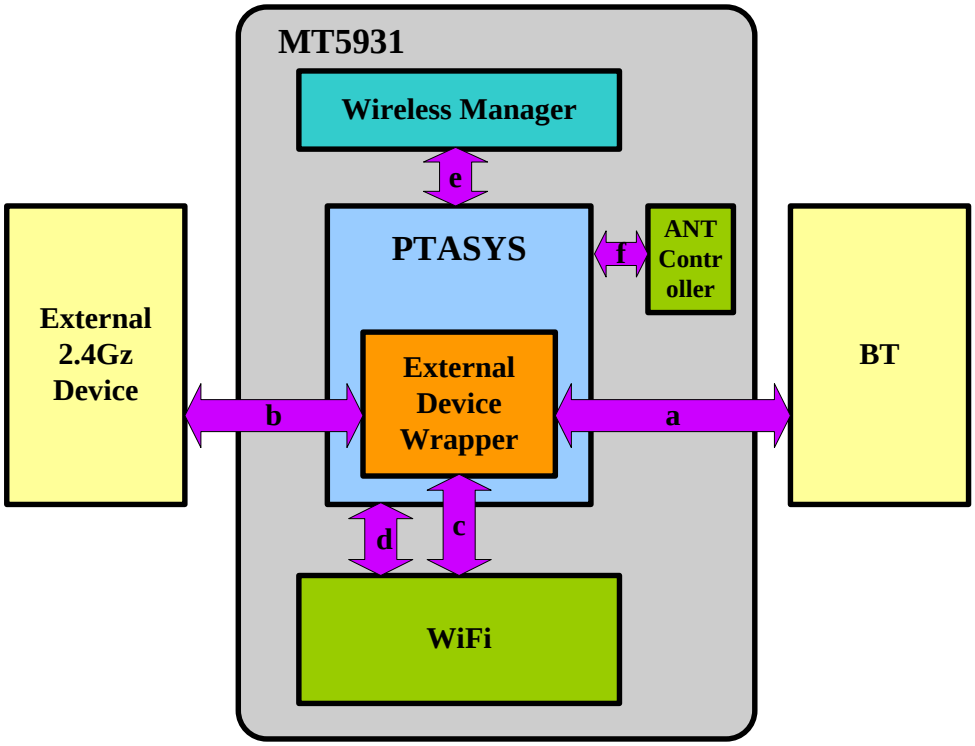


Figure 12 BT/WLAN/EXT coexistence design architecture

a. BT external interface.
   - 1 wire mode (MediaTek proprietary).
   - 1 wire extend mode (MediaTek proprietary).
   - 2 wire mode.
   - 3 wire mode (TFBGA only).
   - 4 wire mode (TFBGA only).
   - 1 wire extend serial interface (ESI) mode (MediaTek proprietary).
   - 2 wire extend serial interface (ESI) mode (MediaTek proprietary).

b. External 2.4Gz device interface (TFBGA only).
   - 2 wire mode.
   - 3 wire mode.
   - 3 wire extend mode (MediaTek proprietary, only for WiMAX).

c. WLAN/BT and WLAN/EXT coexistence interface.

d. WLAN/PTA internal interface.

e. WMT/PTA internal interface.

f. ANT control interface.

The detail descriptions are listed in the following sections.

4.4.1 External interface for co-existed and co-located 2.4GHz WLAN and BT

MT5931 supports an information exchange scheme for co-existed and co-located 2.4GHz WLAN and BT. The information exchange is mainly defined for

a. Scheduled coexistence mode (SCM)
b. Unscheduled coexistence mode (UCM)
c. Baseband enhancement in both Bluetooth and WLAN

SCM is aimed for low cost BT/WLAN coexistence design. When SCM is used, BT and WLAN share the antenna exclusively. UCM is aimed for high performance BT/WLAN coexistence design. When UCM is used, one additional coupler and switch are added compared with SCM. In this case, BT and WLAN can work simultaneously by the same antenna.

Scheduled coexistence mode is supported by adjusting Bluetooth and WLAN activities for the optimal signal coverage with acceptable throughput. BT voice/audio traffic is always in high priority. WLAN packets will be scheduled in Bluetooth idle period.

Unscheduled coexistence mode is supported by the extensive frequency planning and interference cancellation with Bluetooth and WLAN for optimal throughput (even in single antenna). In this scheme, WLAN adjusts its TX power based on the frequency of the Bluetooth device and adapts its receiver when Bluetooth traffic is busy. Bluetooth also adjusts its TX power to a proper stage when it has frequency collision with WLAN. When adopting this scheme, the receiver's anti-interference ability of Bluetooth and WLAN is the key to achieve better performance.

To obtain the best coexistence performance, the wireless manager task (WMT) will choose scheduled coexistence mode or unscheduled coexistence mode according to the criteria shown in the following figure. When both BT and WLAN have good signal quality, unscheduled coexistence mode is used for the best coexistence performance. In this case, BT and WLAN TX power is controlled in response to its RSSI change. When either the signal quality of BT or WLAN is poor, scheduled coexistence mode is used with restoring its normal TX power accordingly. Although BT/WLAN has to perform TX/RX operation exclusively to prevent the mutual interference, by using the proposed time domain solution, a fair coexistence performance can still be achieved.

4.4.2 External interface for all co-existed and co-located 2.4GHz devices

This interface supports 2/3-wire PTA modes and MediaTek proprietary ESI (extend serial interface) solution.

If external 2.4GHz device is a WiMAX device, the EXT interface has extra information of the WiMAX frame structure and signaling to inform WLAN block by interface e to do the following modes.

Unscheduled coexistence mode is supported by interference cancellation with WiMAX and WLAN for optimal throughput (even in a single antenna). In this scheme, WLAN adjusts its Tx power based on WiMAX's frequency and frame structure. If WiMAX also adjusts its Tx power by checking WLAN's frequency, this scheme can achieve optimum throughput in both devices.

Scheduled coexistence mode is supported by adjusting WLAN and WiMAX activities for optimal signal coverage with acceptable throughput. WLAN schedules all traffic in the WiMAX Tx idle period.

4.4.3 ANT control interface

MT5931 provides configurable antenna control interface to support BT/WLAN dual and single antenna architectures. All of them can be configured through the antenna controller. When SCM is used, antenna is chose for BT if BT takes the grant. Otherwise, antenna is chose for WLAN. When UCM is used, the antenna selection depends on the wanted attenuations of BT and WLAN, respectively.

5 Interface description

5.1 Host interface (HIF)

MT5931 HIF module provides 3 interfaces to connect to the host. One SDIO card interface, one SPI interface and one eHPI interface connected to the host.

SDIO provides high-speed data I/O with low power consumption for mobile electronic devices. During normal initialization and interrogation by the SDIO host, the SDIO client identifies itself as an SDIO card. The host software obtains the card information in a tuple (linked list) format and determines if that the I/O functions of the card are acceptable to activate.

For the SDIO bus driver provided by OS, it simply maintains a single First-In-First-Out queue for processing the SDIO bus requested from different client drivers. For the client driver operated on the OS, its function is registered to OS, and will be invoked by OS in its thread priority.

In the assumption of the host interface is the performance limitation for the functions attached to the HIF, several bus access management approaches can be taken toward differentiating the high and low priority traffic. However, the performance limitation may also exist under different user scenario.

5.1.1 Signal pins

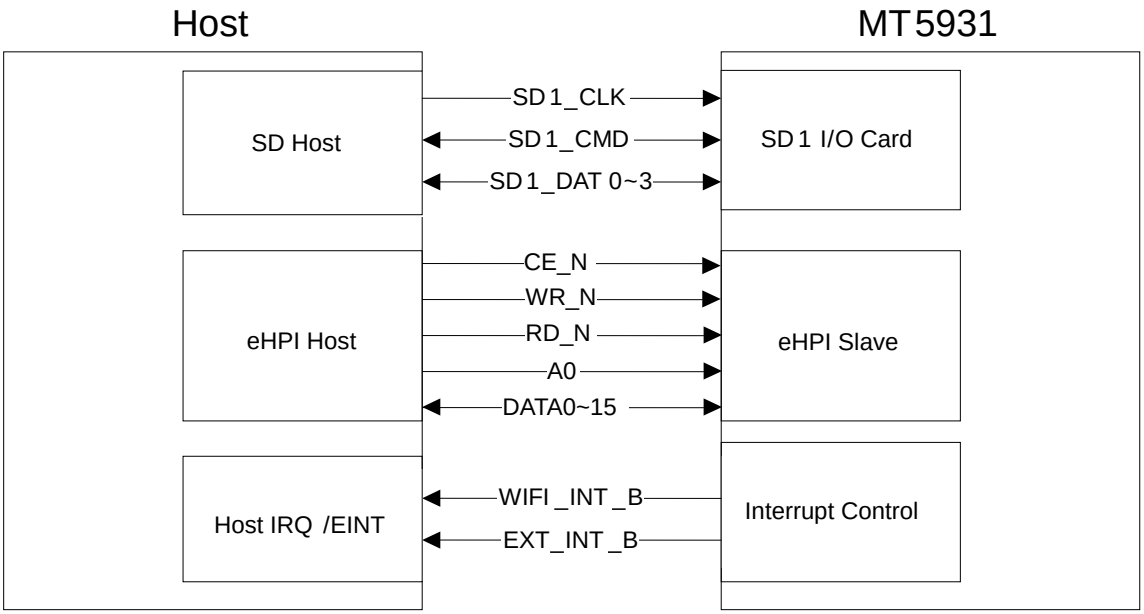


Figure 13 Signal connections to one 4-bit SDIO card and host interrupt

5.1.2 SDIO Timing Waveform

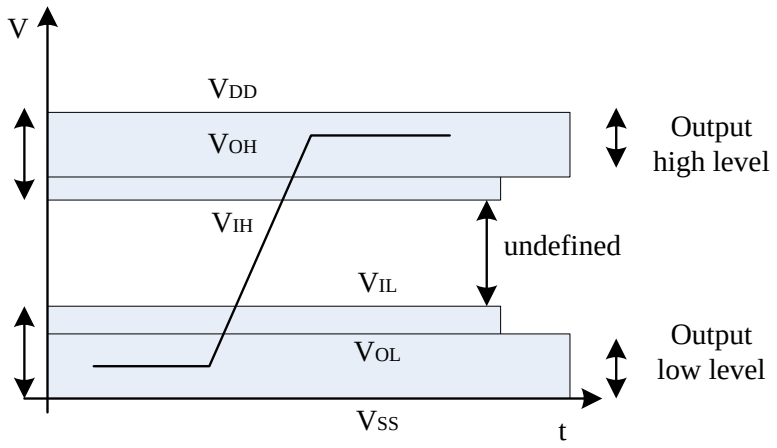


Figure 14 Bus signal levels

Parameter	Symbol	Min	Max	Unit	Conditions
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH}=-100uA V_{DD} min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL} = 100uA V_{DD} min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.25*V_{DD}	V	

Table 10 Bus signal voltage

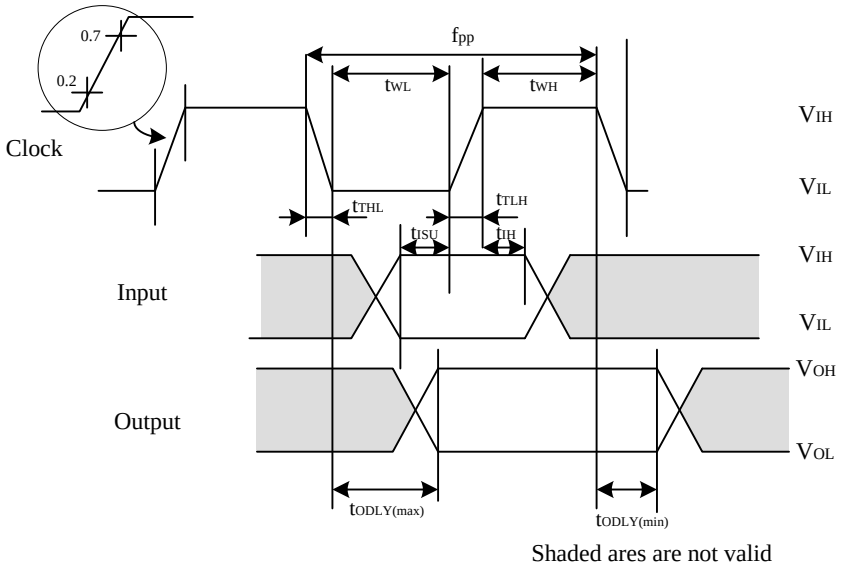


Figure 15 Bus timing diagram (default)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{CARD}<= 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0/100	400	kHz	C_{CARD}<= 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD}<= 10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{CARD}<= 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD}<= 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD}<= 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{CARD}<= 10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{CARD}<= 10 pF (1 card)

Parameter	Symbol	Min	Max	Unit	Remark
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{OLDY}	0	14	ns	C_L<= 10 pF (1 card)
Output Delay time during Identification Mode	t_{OLDY}	0	50	ns	C_L<= 10 pF (1 card)

Table 11 Bus timing parameter values (default)

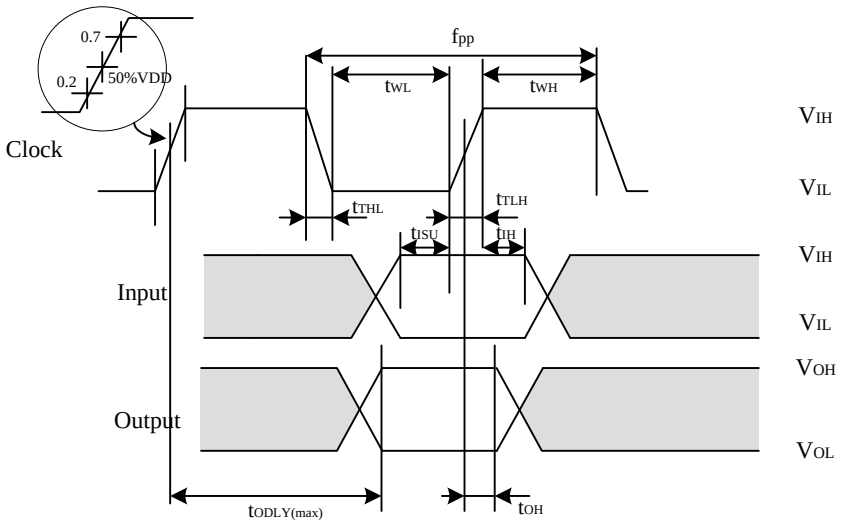


Figure 16 High-speed timing diagram

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{CARD}<= 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD}<= 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD}<= 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD}<= 10 pF (1 card)

Parameter	Symbol	Min	Max	Unit	Remark
Clock fall time	t_{THL}		3	ns	C_{CARD}<= 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{CARD}<= 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{CARD}<= 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{OLDY}		14	ns	C_L <= 10 pF (1 card)
Output Hold time	t_{OH}	2.5		ns	C_L>= 10 pF (1 card)
Total System capacitance for each line (1)	C_L		40	pF	1 card

(1) In Order to satisfy serve timing, host shall drive only one card

Table 12 High-Speed timing parameter values

5.1.3 SPI timing waveform

MT5931 supports SPI with T-mode and M-mode, 8-/16-/32-bit mode and big/little endian.

Select Pin (SPI_MODE_SEL)	Mode
0	M-Mode
1	T-Mode

Table 13 Table SPI mode selection table

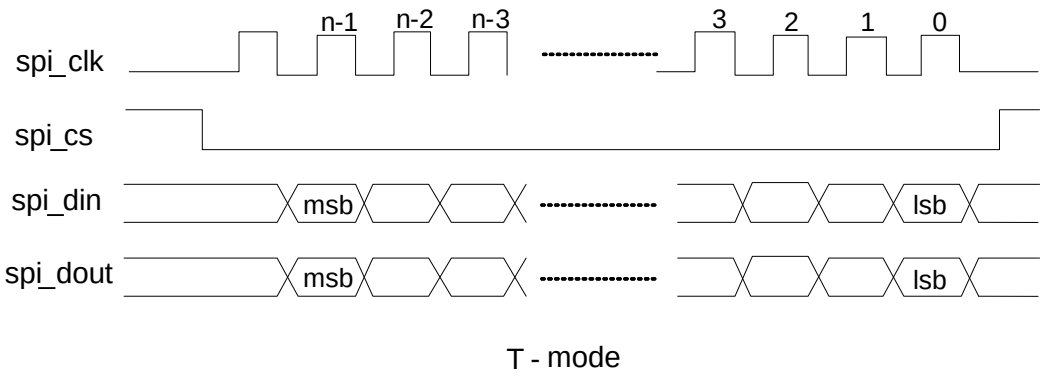


Figure 17 T-Mode SPI protocol

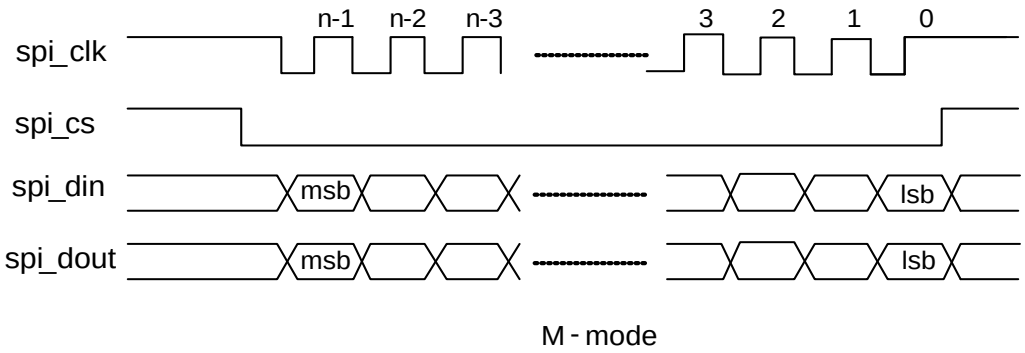
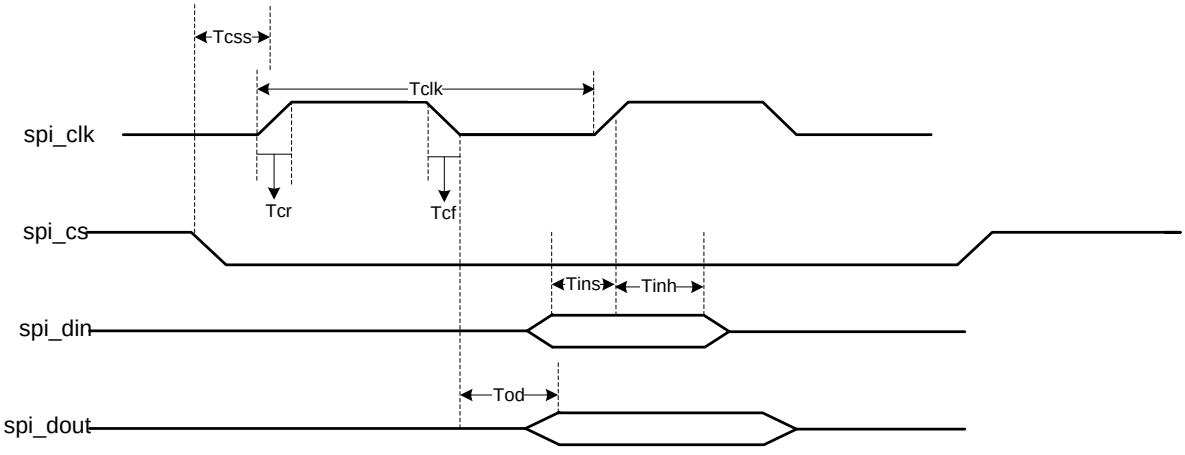


Figure 18 M-Mode SPI protocol



Symbol	Parameter	Min	Typ	Max	Units
Tclk	SPI clock period	40			ns
Tcr/Tcf	Clock Rise/Fall time			2.5	ns
Tcss	CS setup time	7.86			ns
Tins	Din setup time	5			ns
Tinh	Din hold time	5			ns
Tod	Dout output delay			14	ns
Note: This timing spec criterion is VIO=1.8V.It will gain better performance if set stronger VIO.					

5.1.4 eHPI timing waveform

Use section 2.1.1 strapping method to sel eHPI-8 or eHPI-16.With eHPI-8 being selected, we need 4 input control pins and 8 data pins, With eHPI-16 being selected, we need 4 input control pins and 16 data pins. However eHPI-16 could get almost twice the data rate for large amount burst data access.

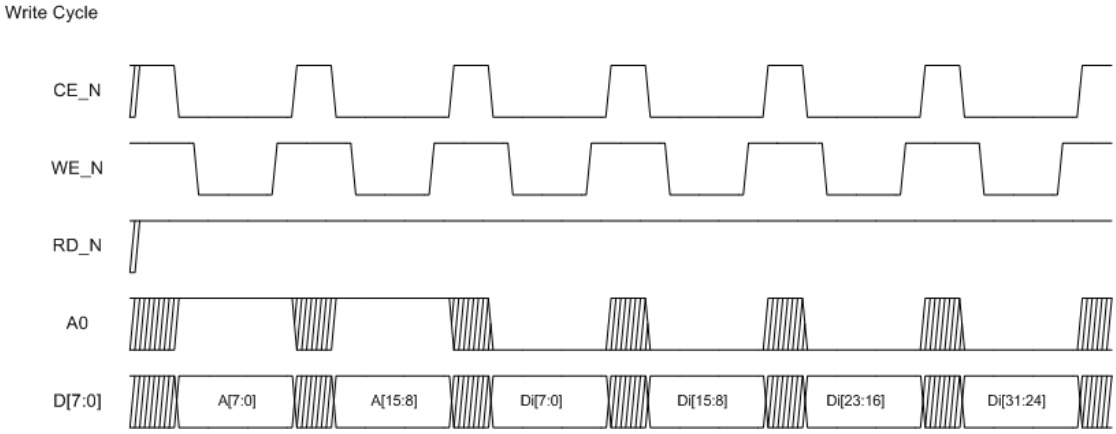


Figure 19 eHPI8 Single Write Access

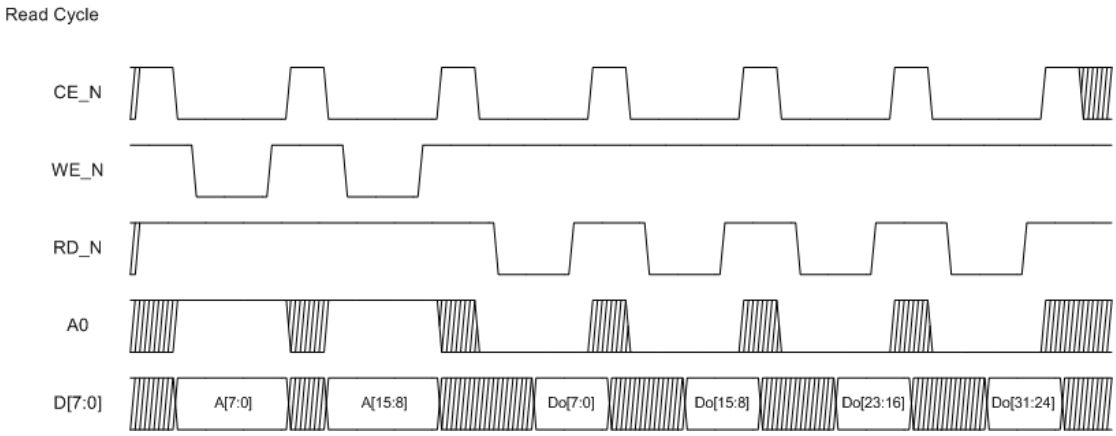


Figure 20 eHPI8 Single Read Access

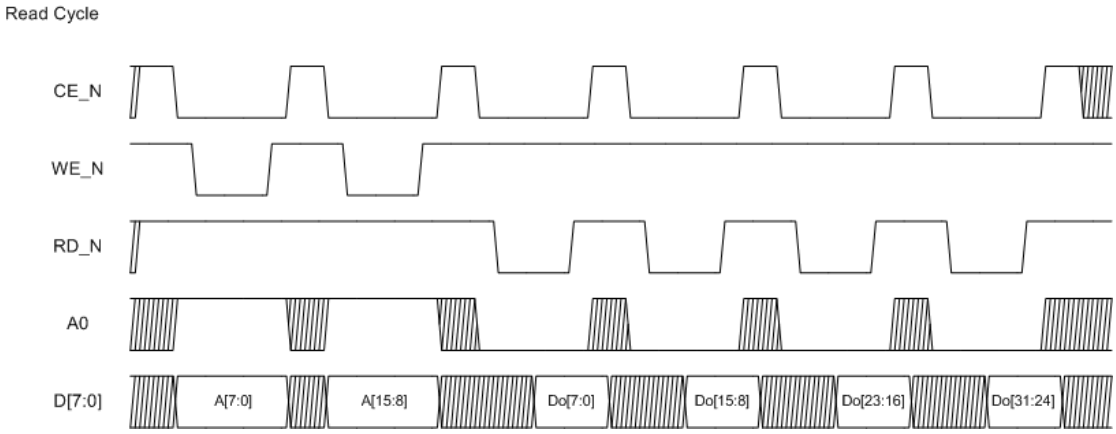


Figure 21 eHPI8 Burst Write Access (Data Port)

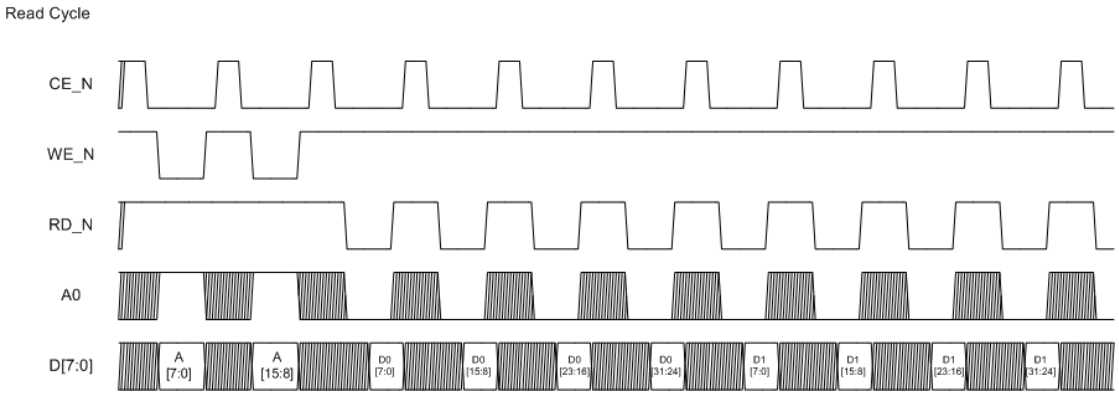


Figure 22 eHPI8 Burst Read Access (Data Port)

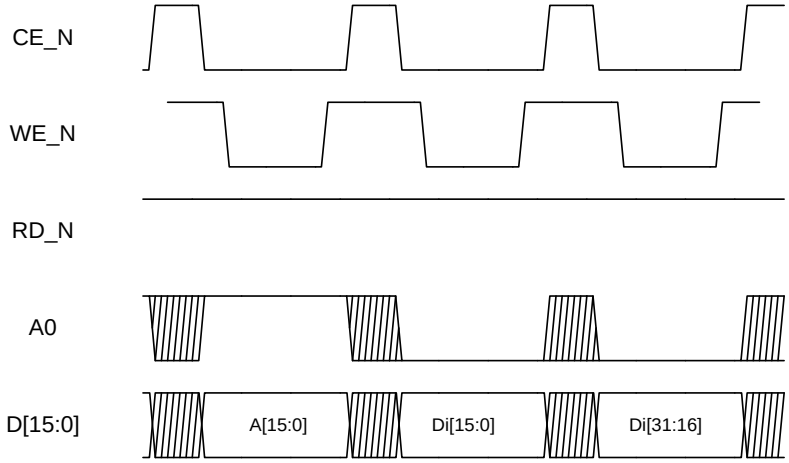


Figure 23 eHPI16 Single Write Access

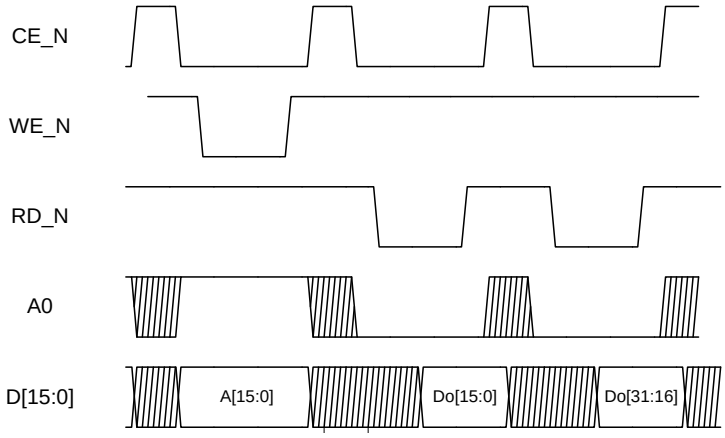


Figure 24 eHPI16 Single Read Access

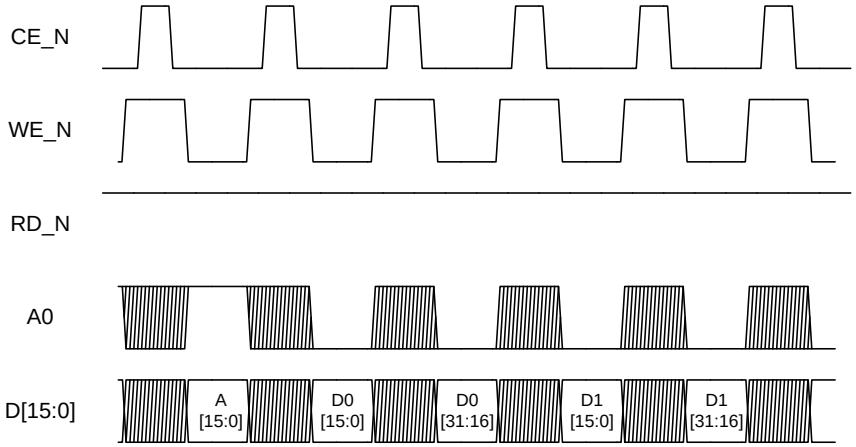


Figure 25 eHPI16 Burst Write Access (Data Port)

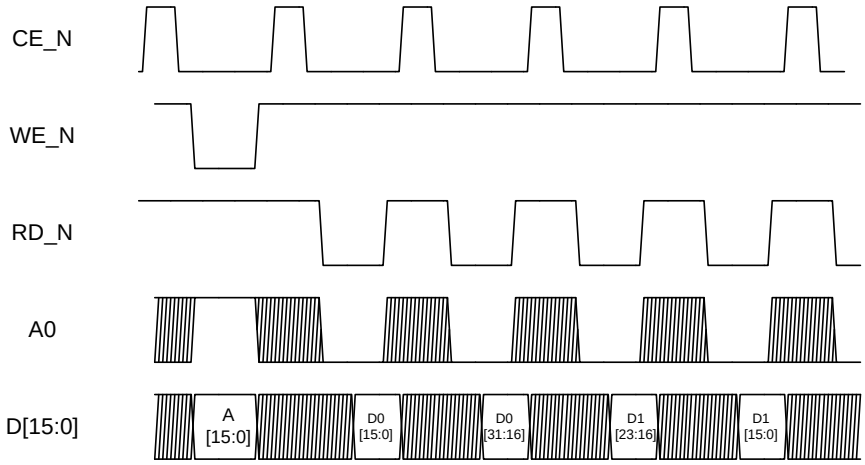


Figure 26 eHPI16 Burst Read Access (Data Port)

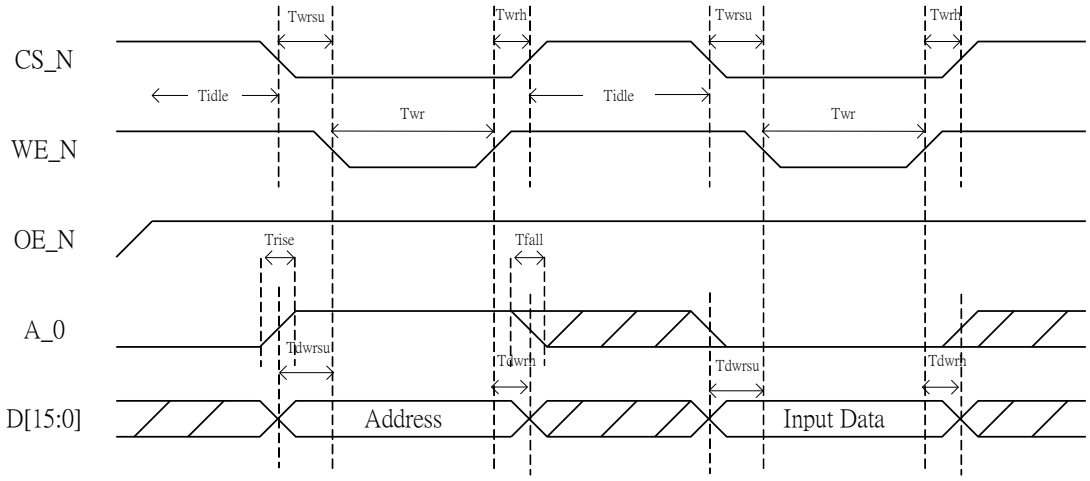


Figure 27 eHPI Write Cycle Timing Diagram

Symbol	Parameter	Min	Typ	Max	Units
Twr	Write Pulse Width	40			ns
Twrsu	CS_N vs WE_N setup time	0			ns
Twrh	CS_N vs WE_N hold time	0			ns
Tdwrsu	Data & A_0 vs WE_N setup time	10			ns
Tdwrh	Data & A_0 vs WE_N hold time	10			ns
Tidle	Twice Access cycle space Time	40			ns
Trise/Tfall	Control & Data signals' Rise/Fall time			5	ns

Table 14 Timing Parameter of eHPI Write Cycle

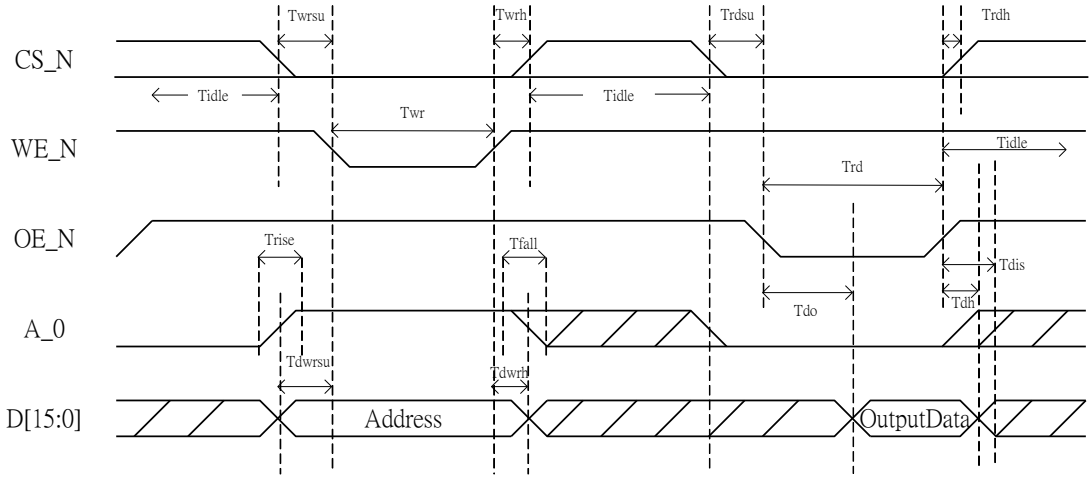


Figure 28 eHPI Read Cycle Timing Diagram

Symbol	Parameter	Min	Typ	Max	Units
Twr	Write Pulse Width	40			ns
Twrsu	CS_N vs WE_N setup time	0			ns
Twrh	CS_N vs WE_N hold time	0			ns
Tdwrsu	Data & A_0 vs WE_N setup time	10			ns
Tdwrh	Data & A_0 vs WE_N hold time	10			ns
Tidle*	Twice Access cycle space Time	40			ns
Trd	Read Pulse Width	40			ns
Trdsu	CS_N vs OE_N setup time	0			ns
Trdh	CS_N vs OE_N hold time	0			ns
Tdo	Output Data Delay Time			20	ns
Tdh	Output Data Hold Time	0			ns
Tdis	Output Disable Time			20	ns
Trise/Tfall	Control & Data signals' Rise/Fall time			5	ns

Table 15 Timing Parameter of eHPI Read Cycle

5.2 EEPROM interface

5.2.1 EEPROM controller introduction

MT5931 supports 3-wire serial EEPROM of which the size range is from 128 bytes to 2048 bytes. The controller operates on the 16-bit data protocol.

5.2.2 EEPROM content

Word Offset	Byte Offset	Content	Description	Default
0x00	0x00	Signature	EEPROM signature. The MAC will automatically load the contents in EEPROM to the corresponding registers if the EEPROM signature is right after being powered on; otherwise, the default values are used.	0x5931
0x01~0x1B	0x002~0x036	MT5931.CIS0. CISTPL_VERS_1	The content of MT5931 CIS0. Reserved 54 bytes for CISTPL_VERS_1 field.	
0x1C	0x38	Checksum	Checksum (Bit 15~Bit 8) The check sum of data is from word offset 0x01 to word offset 0x1C. The sum from byte 0x2 to byte 0x38 should be 0xFF.	

Table 16 EEPROM content

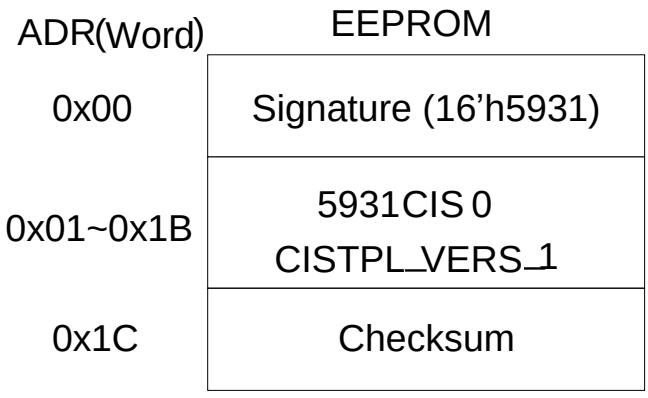


Figure 29 EEPROM configuration

5.2.3 EEPROM checksum function

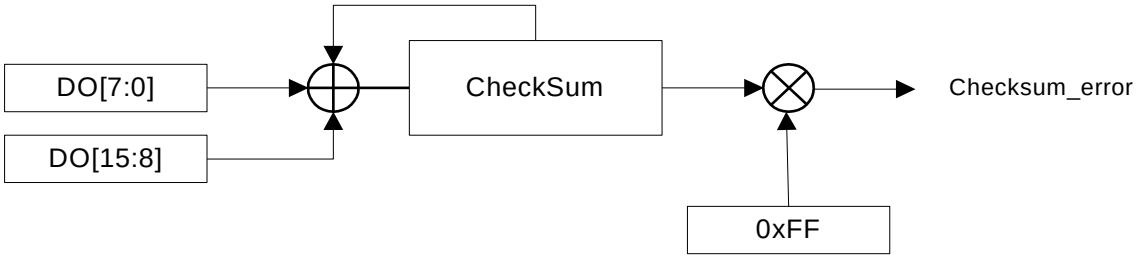


Figure 30 EEPROM CRC checksum diagram

After passing the signature of EEPROM controller check, data will be read from EEPROM. The checksum function will continue until the address reaches 0x1C.

5.2.4 EEPROM interface connection

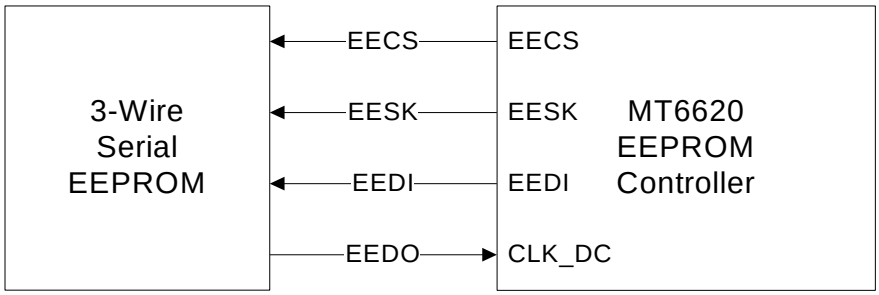


Figure 31 EEPROM interface connection

5.2.5 EEPROM interface timing

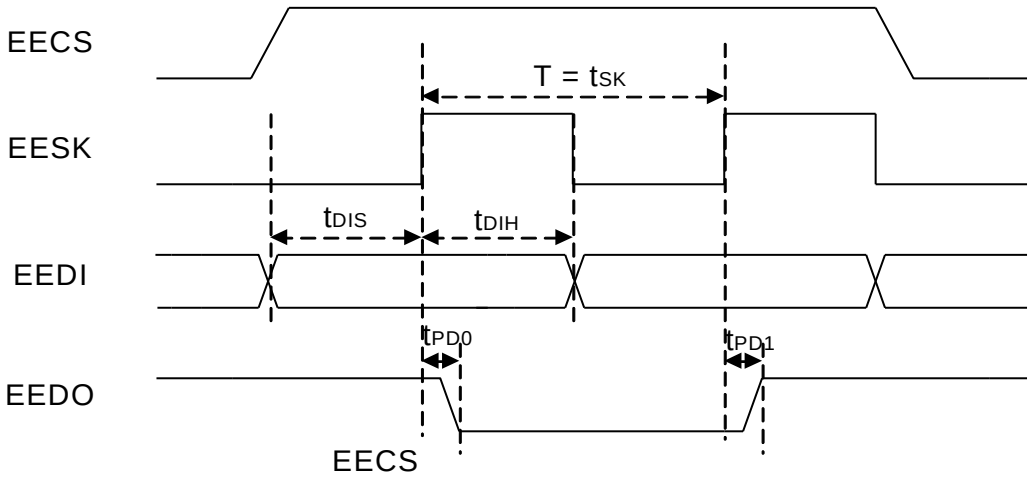


Figure 32 EEPROM data timing

Description	Symbol	Min.	Max.	Unit	Notes
I2C Serial Clock	t_{SK}		2500	ns	1
Data Input Setup Time	t_{DIS}	0.5T - 20	0.5T + 20	ns	
Data Input Hold Time	t_{DIH}	0.5T - 20	0.5T + 20	ns	
Data Output Delay to “0”	t_{PD0}		500	ns	2
Data Output Delay to “1”	t_{PD1}		500	ns	2

Note: 1. It supports I2C fast mode up to 400KHz. 2. Data output direction is from EEPROM Slave to MT5931 Master. This parameter depends on EEPROM device.

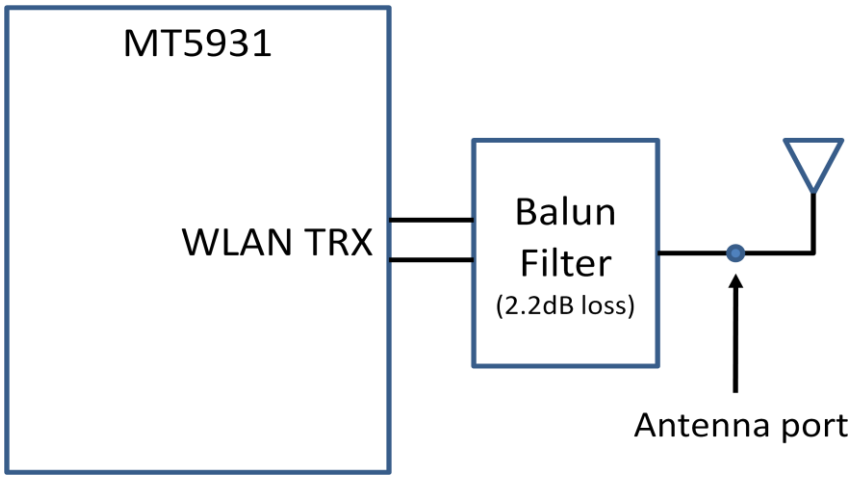
Table 17 EEPROM AC characteristics

5.3 EFUSE function

There are some EFUSE macros inside MT5931. EFUSE macro is a one-time-programming (OTP) non-volatile memory used to store sensitive and important data. EFUSE controller delivers EFUSE status and re-initializes EFUSE macro. Users can program the EFUSE via EFUSE controller with proper configuration and sequences.

6 Radio characteristics

6.1.1 2.4GHz receiver specification



Note: All specification is measured at the antenna port unless otherwise specified.

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency Range		2412	-	2484	MHz
RX Sensitivity	1 Mbps DSSS		-96		dBm
	2 Mbps DSSS		-94		dBm
	5.5 Mbps DSSS		-91		dBm
	11 Mbps DSSS		-88.5		dBm
RX Sensitivity	6 Mbps OFDM		-92.5		dBm
	9 Mbps OFDM		-90.5		dBm
	12 Mbps OFDM		-89.5		dBm
	18 Mbps OFDM		-87		dBm
	24 Mbps OFDM		-84		dBm
	36 Mbps OFDM		-80		dBm
	48 Mbps OFDM		-76.5		dBm
	54 Mbps OFDM		-75		dBm
RX Sensitivity BW=20MHz Green Field 800nS Guard Interval Non-STBC	MCS 0		-92		dBm
	MCS 1		-88.5		dBm
	MCS 2		-86.5		dBm
	MCS 3		-83.5		dBm
	MCS 4		-80.5		dBm
	MCS 5		-76		dBm
	MCS 6		-74.5		dBm
	MCS 7		-73		dBm
RX Sensitivity BW=40MHz Green Field 800nS Guard Interval Non-STBC	MCS 0		-89		dBm
	MCS 1		-85.5		dBm
	MCS 2		-83.5		dBm
	MCS 3		-80.5		dBm
	MCS 4		-77.5		dBm
	MCS 5		-73		dBm
	MCS 6		-71.5		dBm

Parameter	Description	Min.	Typ.	Max.	Unit
	MCS 7		-69.5		dBm
Maximum Receive Level	11 Mbps DSSS			-3	dBm
	6 Mbps OFDM			-3	dBm
	54 Mbps OFDM			-3	dBm
	MCS0			-3	dBm
	MCS7			-3	dBm
Adjacent Channel Rejection (30MHz offset)	1 Mbps DSSS			40	dB
Adjacent Channel Rejection (25MHz offset)	11 Mbps DSSS			40	dB
Adjacent Channel Rejection (25MHz offset)	6 Mbps OFDM			37	dB
	54 Mbps OFDM			25	dB
Adjacent Channel Rejection (25MHz offset), BW=20MHz	MCS 0			33	dB
	MCS 7			18	dB
Adjacent Channel Rejection (40MHz offset), BW=40MHz	MCS 0			33	dB
	MCS 7			18	dB
Blocking Level at RF Port	776~794 MHz CDMA2000		TBD		dBm
	824~849 MHz GSM		TBD		dBm
	880~915 MHz GSM		TBD		dBm
	1710~1785 MHz GSM		TBD		dBm
	1850~1910 MHz GSM		TBD		dBm
	1850~1910 MHz WCDMA		TBD		dBm
	1920~1980 MHz WCDMA		TBD		dBm

Table 18 2.4GHz receiver specification

6.1.2 2.4GHz transmitter specification

Parameter	Description	Min	Typ	Max	Unit
Frequency Range		2412	-	2484	MHz
Output Power	802.11b, 1~11 Mbps DSSS			18.5	dBm
	802.11g, 6 ~54Mbps OFDM		15.5		dBm
	802.11n, HT20 MCS0~7		15.5		dBm
	802.11n, HT40 MCS0~7		13.5		dBm
TX Power Accuracy				±1.5	dB
Carrier Suppression				30	dBc
Return Loss			8		dB
Transmitted Power	76~108 MHz			-143	dBm/Hz
	776~794MHz			-143	dBm/Hz
	869~960 MHz			-143	dBm/Hz
	925~960 MHz			-143	dBm/Hz
	1570~1580 MHz			-143	dBm/Hz
	1805~1880MHz			-143	dBm/Hz
	1930~1990MHz			-143	dBm/Hz

Parameter	Description	Min	Typ	Max	Unit
	2110~2170MHz			-143	dBm/Hz
Harmonic Output Power	2nd Harmonic			-47	dBm/MHz
	3rd Harmonic			-76	dBm/MHz

Table 19 2.4GHz transmitter specification

6.2 Current consumption

Note: All result is measured at the antenna port and VBAT is 3.6V.

Description	Performance	
	TYP	UNITS
OFF	13.5	µA
RX Active, BW40, HT40 MCS7	53.8	mA
RX Active, BW20, All supported rates	48.9	mA
RX Listen	36.2	mA
RX Sleep	67	µA
RX Power saving, DTIM=1	0.54	mA
TX HT40, MCS7@11dBm	164	mA
TX HT20, MCS7@14dBm	170	mA
TX OFDM, 54M@16dBm	187	mA
TX CCK, 11M@19dBm	225	mA

Table 20 WLAN 2.4GHz Current Consumption

ESD CAUTION

MT5931 is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT5931 is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.