Low-power high performance 3-axes magnetometer

1、Features

1.1、Functions Features:

- 3-axis magnetometer
- Wide supply voltage:2.2v to 3.6v
- Independent IOs supply(1.65v) and supply voltage compatible
- Idle mode(power down mode)power consumption down to 2uA(max:3uA)
- I2C/SPI digital output interface
  - I2C bus interface
    Standard mode and fast mode
  - 3-wire SPI or 4-wire SPI
- 16-bit resolution
  - Built-in 19-bit A to D converter for magnetometer data out
  - The highestSensitivity:1.88mG/LSB(0.188uT/LSB)
- Operation mode
  - Power-down mode
  - Burst mode
  - Single measurement mode
  - Wake-up on change mode
  - External trigger measurement mode
- One programmable interrupt generator for DRDY or Trig function
  - DRDY function for measurement data ready
- Built-in oscillator for internal clock source
- Power on reset circuit
- Embedded temperature sensor to compensate sensor temperature effect
- Embedded self-test to built-in internal magnetic field generator
- Full scale:±48Gauss
- RoHS and “Green” compliant

Operating temperatures:

- -40℃ to +85℃

Operating supply voltage:

- Analog power supply :+2.2v to +3.6v
- Digital interface supply :+1.65v to analog supply voltage

Current consumption:

- Power-down: 2uA typ.
- Measurement:
  - Average power consumption at 10Hz repetition rate:280uA type.

1.2、Order information

Model name	Full scale range	Package description
dm110	±48Gauss	14PIN/BGA/1.6mm*1.6mm*0.81mm

1.3、Applications

- Electronic compass
- Handheld devices
- Navigation System
- Frequency changer
- Smartphone
- Tablet PC
- UPS system
- Weld system
- Solar device
- Wind turbine

1.4、General Description

The device is a low-power high performance three axes linear magnetometer belonging to the ”dm” family, based on the hall-effect technology. The output signals(raw X,Y and Z data)will be provided through the I2C standard mode and fast mode protocol, or via half-duplex SPI protocol（3-wire SPI or 4-wire SPI）.

The device provides excellent temperature stability and high resolution over the whole operating temperature range from -40℃ to +85℃. And there is an on-board non-volatile memory to store calibration data on-chip.

The self-test function with internal magnetic source allows the user to check the functioning of the sensor in the final application. The device may be configured to generate interrupt signals by the inertial DARY events. The timing of interrupt generators is programmable by the end user on the fly.
The IC is available in small thin plastic ball grid array package (BGA),it incorporates magnetic sensors for detecting terrestrial magnetism in the X-axis, Y-axis, and Z-axis, a sensor driving circuit, signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor.

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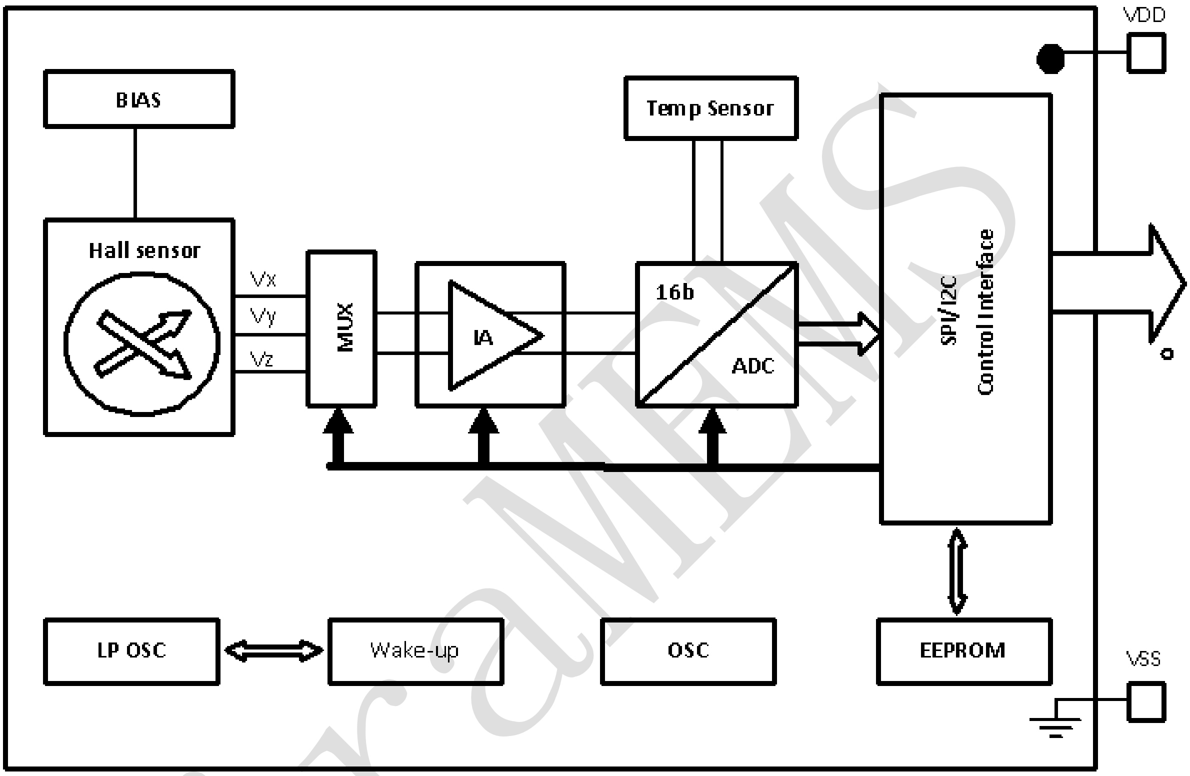
2、Functional circuit

2.1、Functional Block Diagram



2.2、Block function

Block	Function
BIAS	Bias circuit for constant-current driving of hall elements
Hall sensor	Monolithic Hall elements
MUX	Multiplexer for selecting hall elements
IA	Amplifier used to amplify the magnetic sensor signal.
16b/ADC	Obtain 16-bit analog-to-digital conversion data
Temp Sensor	Temperature sensor
SPI/I2C control interface	Exchanges data with an external CPU DRDY pin indicates sensor measurement end and data is ready to be read. I2C bus interface using two pins, namely, SCL and SDA. Standard mode and Fast mode are supported. The low-voltage specification can be supported by applying

	1.65V to the Vdd_IO pin. 4-wire SPI is also supported by SK,SI,SO and CSB pins. 4-wire SPI works in Vdd_IO pin voltage down to 1.65V,too
LP OSC	Generates a Low-power operating clock for sequencer
Wake-up	Wakeup module, for change sensor mode of sleep and operation mode
OSC	Generates an operating clock for sensor measurement
EEPROM	store calibration data

2.3、Pin Function

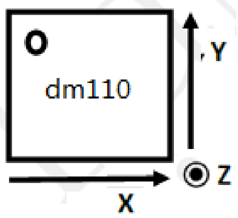
BGA Pin No.	**Pin name**	**I/O**	**Power supply system**	Type	**Function**
A1	INT/TRIG	I/O	VDD_IO	CMOS	INT mode: Data ready output pin. ”H” active, Informs measurement ended and data is ready to be read. TRIG mode: external trigger pulse input pin. Enable only in external trigger mode.
A2	CS	I	VDD_IO	CMOS	I2C/SPI mode selection(1:I2C mode enable;0:SPI mode enable)
A3	SCL/SCLK	I/O	VDD_IO	CMOS	SCL: control data clock input pin Input: Schmidt trigger SCLK: serial clock input pin when the SPI mode is selected.
A4	SDA/MOSI	I/O	VDD_IO	CMOS	SDA: control data input/output pin Input: Schmidt trigger; MOSI: serial data input pin when the SPI mode is selected. Output: Open drain
B1	VDD	-	-	Power	Analog power supply pin
B2	NC	-	-	-	Not connected
B3	NC	-	-	-	Not connected
B4	MISO	-	-	-	Serial data output pin when the 4-wire SPI mode is selected.
C1	VSS	-	-	Power	Ground pin
C2	NC	-	-	-	Not connected
C3	INT/TRIG	I/O	VDD_IO	CMOS	INT mode: Data ready output pin. ”H” active, Informs measurement ended and data is

					ready to be read. TRIG mode: external trigger pulse input pin. Enable only in external trigger mode.
C4	VDD_IO	-	-	Power	Digital interface positive power supply pin
D1	A0	I	VDD	CMOS	When the I2C mode is selected,A0 is slave address 0 input pin.0:connect to VSS;1:connect to VDD
D2	A1	I	VDD	CMOS	When the I2C mode is selected,A1 is slave address 1 input pin. 0:connect to VSS;1:connect to VDD
D3	NC	-	-	-	Not connected
D4	NC	-	-	-	Not connected

3、 Functional Specification

3.1、Magnetic sensor

The measurement data increases as the magnetic flux density increases in the arrow directions.



3.3、Operation Mode

The dm110 can operate in 3 modes:

- Burst mode
- Single Measure mode
- Wake-Upon Change

3.3.1、Burst mode

The ASIC will have a programmable data rate (BURST_DATA_RATE[6:0] of ox01 register) at which it will operate. This data rate implies auto-wake up and sequencing of the ASIC, flagging that data is ready on a dedicated pin (INT/DRDY).The maximum data rate will correspond to 1/n*TCONV (n=3) incase of3axes magnetic data. The time during which the ASIC has a counter running, but is not doing an actual conversion is called the Standby mode (STBY).

When the sensor is operating in burst mode, it will make conversions at specific time intervals. The programmability of the user is the following:

- Burst speed(TINTERVAL)
- Conversion time(TCONV)
- Axes/Temperature (MDATA)

Whenever the sensor has made the selected conversions (based on MDATA), the INT/DRDY pin will be set (active H) to indicate that the data is ready. It will remain high until the master has sent the command to read out at least one of the converted quantities (ZYXT). Should the master have failed to read out any of them by the time the sensor has made a new conversion, the INT/DRDY pin will be strobed low for 10us, and the next rising edge will indicate a new set of data is ready.

3.3.2、Single Measure mode

The master will ask for data via the corresponding protocol (I^2C or SPI), waking up the ASIC to make a single conversion, immediately followed by an automatic return to sleep mode(IDLE) until the next polling of the master. This polling can also be done by strobing the TRG pin, which has the same effect as sending a protocol command for a single measurement.

Whenever the sensor is set to this mode (or after start up) the sensor goes to the IDLE state where it awaits a command from the master to perform a certain acquisition. The duration of the acquisition will be the concatenation of the T_{STBY}, T_{ACTIVE} and $n*T_{CONV}$ (n=numbers of axes). The conversion time will effectively be programmable by the user, but is equally a function of the required axes/temperature to be measured.

Upon reception of such a polling command from the master, the sensor will make the necessary acquisitions, and set the INT/DRDY pin high to signal that the measurement has been performed and the master can read out the data on the bus at his convenience. The INT/DRDY will be cleared either when:

- The master has issued a command to read out at least one of the measured components
- The master issues an Exit(EX) command to cancel the measurement
- The chip is reset, after POR(Power-on reset) or Reset command(RT)

3.3.4、Wake-Up on Change

This mode is similar to the burst mode in the sense that the device will be auto-sequencing, with the difference that the measured component(s) is/are compared with a reference and in case the difference is bigger than a user-defined threshold, the INT/DRDY pin is set. The user can select which axes and/or temperature fall under this cyclic check, and which thresholds are allowed.

The Wake-Upon Change (WOC) functionality can be set by the master with as main purpose to only receive an interrupt when a certain threshold is crossed. The WOC mode will always compare a new burst value with a reference value in order to assess if the difference between both exceeds a user-defined threshold. The reference value is defined as one of the following:

- The first measurement of WOC mode is stored as reference value once, as a result of a measurement. This measurement at "t=0"note1 is then the basis for comparison.
- The reference for acquisition (t) is always acquisition (t-1), in such a way that the INT/DRDY will only be set if the derivative of any component exceeds a threshold.

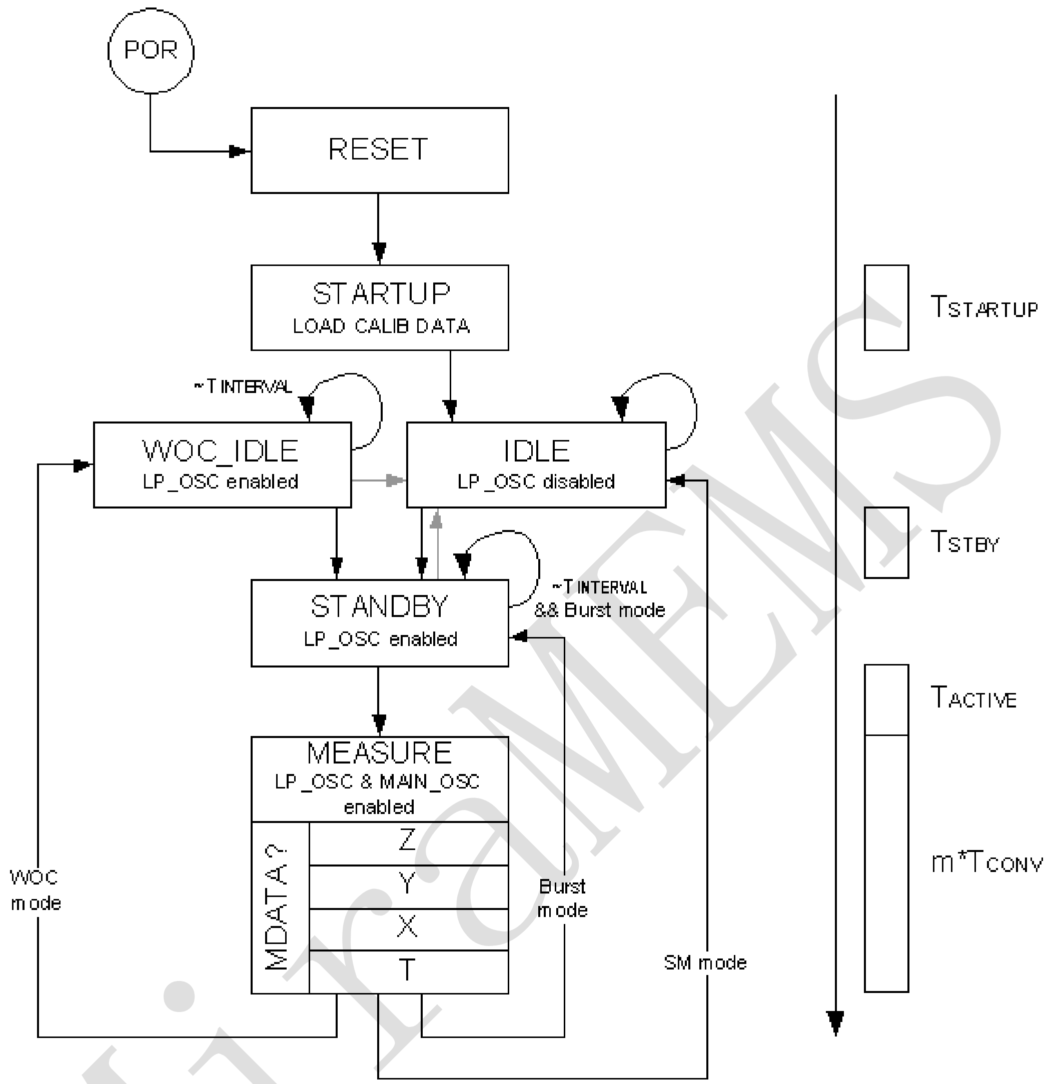
The in-application programmability is the same as for burst mode, but now the thresholds for setting the interrupt are also programmable by the user, as well as the reference, if the latter is data(t=0) or data(t-1) note1.

Note1:
WOC mode means when the device signal changes over threshold value, device interrupt pin will be pull-up high level and data output will be ready, or else device still keep in sleep mode.
There are two modes signal changes in data comparison:
1) The sampling data of current time (t) compare with the first sampling data of WOC mode.
2) The sampling data of current time (t) compare with the data of last time (t=t-1)

3.3.5、change operating mode

The user can change the operating mode at all time through a specific command on the bus. The default start-up mode is Single Measurement mode (in IDLE state), but with a proper user command any mode can be set after power-up. Changing to Burst or WOC mode, coming from Single Measure mode is always accompanied by a measurement first. The top-level state diagram indicating the different mode sand some relevant timing is shown below in this figure. In the Measure state, the MDATA flag will define which components will be measured (ZYXT). The sequential order can't be modified by the user.
Arrows indicated in grey are the direct result of a command to return to Single Measure mode. The main difference between STANDBY and WOC_IDLE is that in STANDBY mode, all analog

circuitry is ready to make a conversion, but this is accompanied by a larger current consumption. For burst mode this extra current consumption is justified because the emphasis is more on accurate timing intervals, avoiding the delay of T_{STBY} before conversion.



4、 Overall Characteristics

4.1、Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	VDD	2.2V	3.6V	V
I/O pins supply voltage	VDD_IO	1.71V	VDD	V
Operating temperature range	TOP	-40	85	℃
Storage temperature range	TST	-50	125	℃
Electrostatic discharge protection: Human Body Model	ESD_HBM		2	KV
Electrostatic discharge protection: Machine Model	ESD_MM		N/A	V
Electrostatic discharge protection: Charged Device Model	ESD_CMD		750	V

Note:

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

4.2、Recommended operating conditions

Parameter	Remark	Symbol	Min.	Typ.	Max.	Unit
Operating temperature		Ta	-40	25	85	℃
Power supply voltage	VDD pin voltage	VDD	2.2	3	3.6	V
	VDD_IO pin voltage	VDD_IO	1.65	1.8	VDD	V

4.3、Sensor Specification

All sensor specification parameter are specified VDD=3.0V,VDD_IO=3.0V and T=25℃

Parameter	Remark	Min.	Typ.	Max.	Unit
Full Range	Each axis		±48		Gauss

Non Linearity	±48Gauss		0.1		% of FS
Sensitivity	X/Y axis		667		LSBs/Gauss
	Z axis		400		LSBs/Gauss
Magnetic Resolution	X/Y axis		1.5		mG/LSB
	Z axis		2.5		mG/LSB
T_{CONV}	Conversion time[Note1]:From IDLE to data ready	1		128	ms
T_{STBY}	From IDLE to STBY		250		us
T_{ACTIVE}	From STBY to ACTIVE		8		us
$T_{INTERVAL}$	Time in between 2 conversions(burst mode or wake-up on change)[Note2]	20		5000	ms

Note:

1: Standby current corresponds to the current consumed in the digital, where not the main oscillator is running which is used for analog sequencing, but only the low-power oscillator. This standby current is present in Burst mode and WOC mode; whenever the ASIC is counting down to start a new conversion.

2: Idle current is the current that is drawn by the ASIC in the IDLE mode, where it can only receive new commands on the communication bus, but all other blocks are disabled. The analog is disconnected, and only the digital IO part allows clocking of a few vital gates.

4.4、 Electrical Specification

The specifications are applicable at 25℃,unless specified otherwise, and for the complete supply voltage range(VDD=2.2V to 3.6V,VDD_IO=1.65V to VDD).

Parameter	Remark	Min	Nom	Max	Unit
VDD	Analog Supply Voltage	2.2	3	3.6	V
VIO	Digital IO Supply	1.71	1.8	VDD	V
IDD,CONV	Conversion Current		2.35	2.6	mA
IDD,STBY	Standby Current(1)		40		µA
IDD,IDLE	Idle Current(2)		2	3	µA
IDD,NOM	Nominal Current (Data-rate = 10Hz, TCONV = 4ms)		280	320	µA

5、Serial interface

5.1、SPI protocol

The IC can handle SPI communication at a bit-rate of 10Mhz. The SPI communication is implemented in a half-duplex way, showing high similarities with I2C communication, but addressing through the CS (Chip Select) pin instead of through bus arbitration. The half-duplex nature is at the basis of the 3-wire or 4-wireSPI support.

SPI Mode:

Mode	data changed on leading(trailing) edge and captured on trailing(leading) edge	High(low) level is inactive state
0	CPHA =0	CPOL =0
1	CPHA =0	CPOL =1
2	CPHA =1	CPOL =0
3	CPHA =1	CPOL =1

The implemented SPI mode is mode 3: CPHA=1 (data changed on leading edge and captured on trailing edge , and CPOL=1 (high level is inactive state). The Chip Select line is active-low.

5.1.1、SPI slave timing values

Symbol	parameter	Value [note]		unit
		Min	Max	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		
th(CS)	CS hold time	10		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	ns
th(SO)	SDO output hold	5		

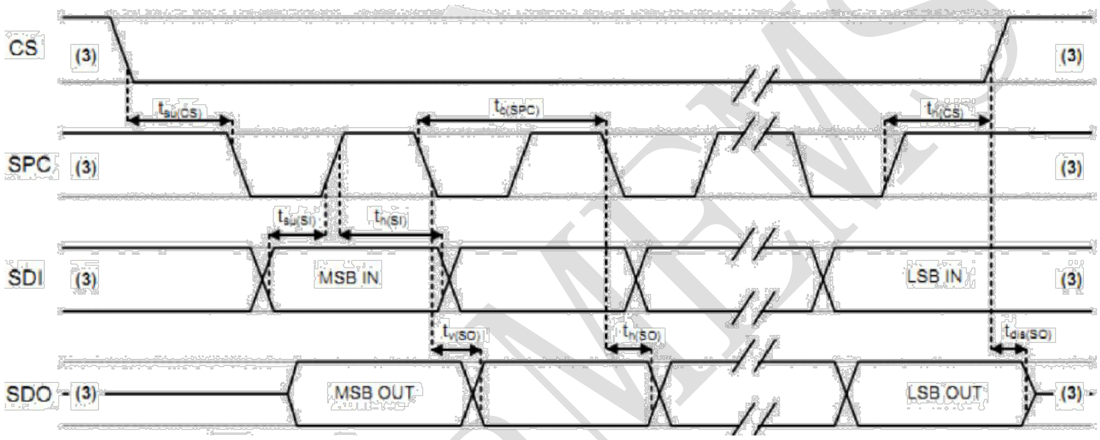
	time			
tdis(SO)	SDO output disable time		50	

Note：

Values are guaranteed at 10 MHz clock frequency for SPI with both4 and 3 wires, based on characterization results, not tested in production.

5.1.2、SPI slave timing diagram note

The communication is also bundled in bytes, equally MSB first and MS Byte first.



Note:

Measurement points are done at 0.2*Vdd_IO and 0.8*Vdd_IO, for both input and output port

5.2、I2C protocol

5.2.1、I2C Address(slave address)

TheI2Caddressismadeupof some hard-coded bits and a memory written value as following:

- I2C_ADDR[6:0] ={EE_I2C_ADDR[4:0],A_1,A_0} with A_i the user-selectable active-high value of the input pads of the device, referred to the V_{DD}supplysystemandEE_I2C_ADDR[4:0] default programmed to 03h.
- When the R/W bit is set to "1", READ instruction is executed. When the R/W bit is set to "0", WRITE instruction is executed.
- If Ai pin is connected to VDD, Ai bit of slave address will be set"1"; and if Ai pin is connected to VSS, Ai bit of slave address will be set"0"

MSB							LSB

0	0	0	1	1	A1	A0	R/W

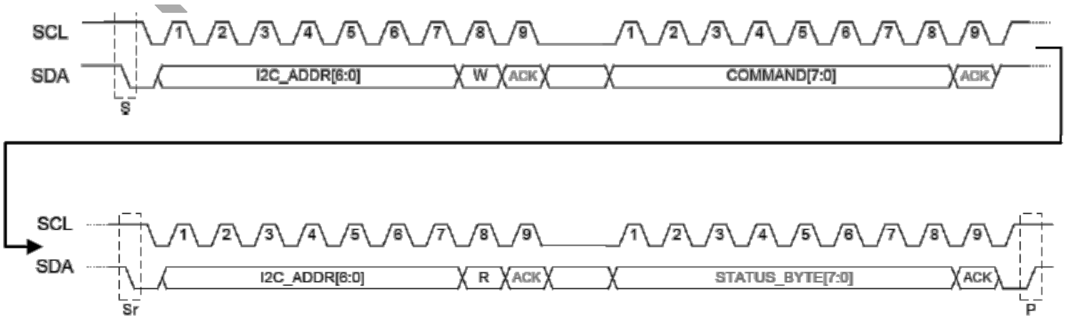
Command	EE_I2C_ADDR[4:0]	A1	A0	R/W	I2C_ADDR[6:0]+R/W
Read	00011	0	1	1	00011011(1BH)
Read	00011	0	0	1	00011001(19H)
Read	00011	1	1	1	00011111(1FH)
Read	00011	1	0	1	00011101(1DH)
Write	00011	0	1	0	00011010(1AH)
Write	00011	0	0	0	00011000(18H)
Write	00011	1	1	0	00011110(1EH)
Write	00011	1	0	0	00011100(1CH)

5.2.2、I2C Principle

The device supports I2C communication in both standard mode and fast mode. Bytes are transmitted MSB first, and in order to reconstruct words, the bytes need to be concatenated MS Byte first. The general principle of communication is always the same:

- Initiating the communication is always done by the Master (Start condition S).
- Addressing the Slave (dm110) followed by a cleared bit to indicate the Master intends to write something to the specific addressed Slave.
- Acknowledging by the Slave if the transmitted address corresponds to the Slave's I2C address. If the latter isn't the case, any further activity on the bus except a Sr(Start Repeat) and P (Stop) condition will be ignored by the dm110.
- Sending a Command Byte by the Master, as depicted in I2C Figure. The Slave will always acknowledge this, even if it is an unrecognized command.
- Issuing a Start Repeat (Sr) condition by the Master in order to restart the addressing phase
- Addressing the Slave(dm110) followed by a set bit to indicate the Master intends to read something from the specific addressed Slave
- Acknowledging by the Slave if the transmitted address corresponds to the Slave's I2C address. If the latter isn't the case, any further activity on the bus except a Sr(Start Repeat) and P (Stop) condition will be ignored by the dm110
- Transmitting the Status Byte by the Slave, who is in control of the bus
- Acknowledging by the Master if the data is well received
- Generating a Stop condition(P) by the master

The Master controlled bus activity is shown in grey body, the Slave controlled bus activity is shown in black body. In case a command is longer than a single byte(see command list), the bytes are transmitted sequentially before generating the Start Repeat(Sr) condition.



The same applies to the Slave responses: following RR and RM commands, the Slave response is more than just the Status Byte. There as well, the data is partitioned in bytes that are transmitted sequentially by the slave. It is the Master's responsibility to issue enough clocking pulses to read back all the data. Finding out how many bytes is possible by decoding the Status Byte information, see Section Status Byte.

5.2.3、I2C slave timing values

Table 7. I^2C slave timing values

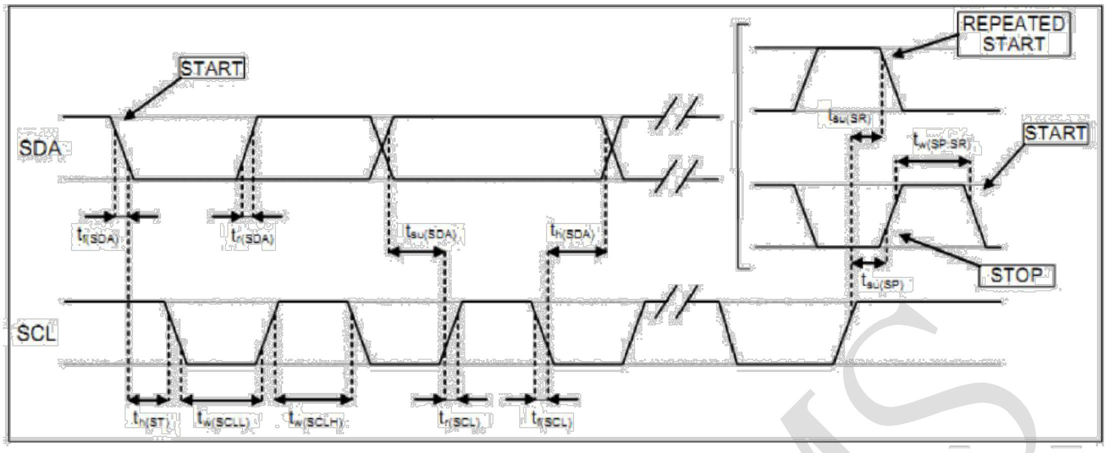
Symbol	Parameter	I^2C standard mode (1)		I^2C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	ns
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		µs
$t_{su(SP)}$	STOP condition setup time	4		0.6		µs
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		µs

Note:

1、 Data based on standard I2C protocol requirement, not tested in production.

2、 Cb=total capacitance of one bus line, in pF .

5.2.4、I2C slave timing diagram note



Note:

Measurement points are done at 0.2*Vdd_IO and 0.8*Vdd_IO, for both input and output port.

6、Memory Map

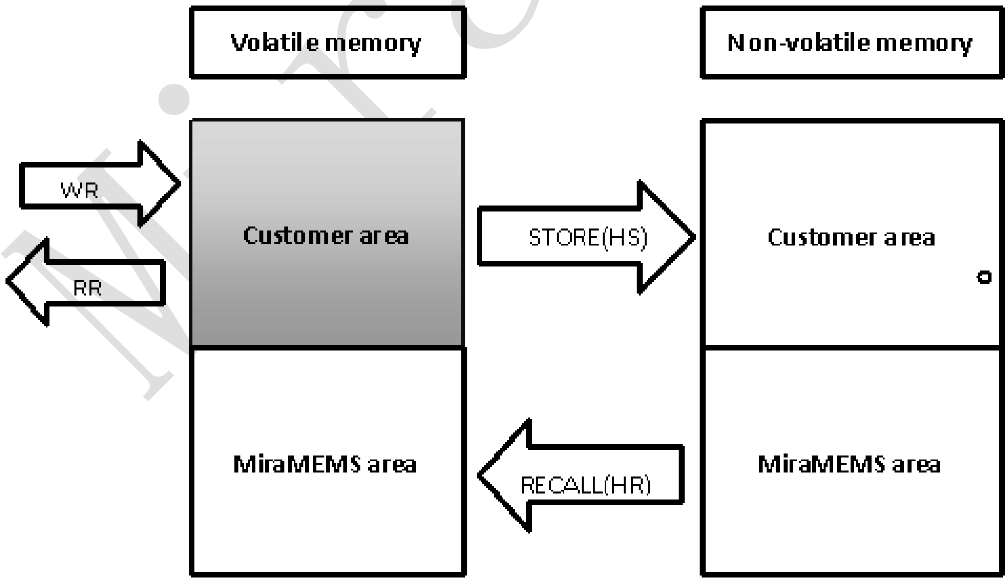
Thedm110has1kbitofnon-volatile memory, and the same amount of volatile memory. Each memory consists out of 64 addresses containing 16 bit words. The non-volatile memory has automatic 2-bit error detection and 1-bit error correction capabilities per address. The handling of such corrections & detections is explained in Section Status Byte.

The memory is split in 2 areas:

- Customer area: [address 0x00 to 0x1f]
- MiraMEMS area: [address 0x20 to 0x3f]

The RR and WR commands impact the volatile memory only, there no direct access possible to the non-volatile memory. The customer area of the volatile memory is bidirection-accessible to the customer; the MiraMEMS area is write-protected. Only modifications in the grey area are allowed with the WR command. The adjustments in the customer area can be stored in the permanent non-volatile memory with the Memory Store command (HS), which copies the entire volatile memory including the MiraMEMS area to the non-volatile one. With the Memory Recall (HR) command the non-volatile memory content can be recalled to the volatile memory, which can restore any modifications due to prior WR commands. The HR step is performed automatically at start-up of the ASIC, either through cold reset or warm reset with the RT command.

The above is graphically shown in this figure.



The customer area houses 3 types of data:

- Analog configuration bits
- Digital configuration bits

◆ Informative(free) bits

6.1、Register Table

The latter can be filled with customer content freely, and covers the address span from (and including) 0x0Ah to 0x1Fh, a total of 352 bits. The memory mapping of volatile and non-volatile memory on address level is identical. The volatile memory map is given in this table.

	Bit Number															
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ANA_RESERVED_LOW							BIST		GAIN_SEL			HALLCONF			
0x01	TRIG/INT	COMM_MODE		WOC_DIFF	EXT_TRIG	TCMP_EN	BURST_SET(zyxt)				BURST_DATA_RATE					
0x02				OSR2		RES_XYZ						DIG_FILT			OSR	
0x03	SENS_TC_HT								SENS_TC_LT							
0x04	OFFSET_X															
0x05	OFFSET_Y															
0x06	OFFSET_Z															
0x07	WOXY_THRESHOLD															
0x08	WOZ_THRESHOLD															
0x09	WOT_THRESHOLD															
0x0A	FREE															
0x0B	FREE															
0x0C	FREE															
0x0D	FREE															
0x0E	FREE															
0x0F	FREE															
0x10	FREE															
0x11	FREE															
0x12	FREE															
0x13	FREE															
0x14	FREE															
0x15	FREE															
0x16	FREE															
0x17	FREE															
0x18	FREE															
0x19	FREE															
0x1A	FREE															
0x1B	FREE															
0x1C	FREE															
0x1D	FREE															
0x1E	FREE															
0x1F	FREE															

6.2、Register Description

The meaning of each customer accessible parameter is explained in this section. The customer area of both the volatile and the non-volatile memory can be written through standard SPI and I^{2}C communication, within the application. No external high-voltages are needed to perform such operations, nor access to dedicated pins that need to be grounded in the application.

6.2.1、Register:0x00

MSByte:

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
ANA_RESERVED_LOW							BIST

LSByte:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	GAIN_SEL[2]	GAIN_SEL[1]	GAIN_SEL[0]	HALLCONF[3]	HALLCONF[2]	HALLCONF[1]	HALLCONF[0]

Register(0x00) description

ANA_RESERVED_LOW	Reserved IO trimming bits
BIST	Enabled the on-chip coil, applying a Z-field [Built-In Self Test][note1] 0: normal 1: generate magnetic field for self-test
0	undefined bit
GAIN_SEL[2:0]	Analog chain gain setting, factor5[note2]betweenminandmaxcode
HALLCONF[3:0]	Hall plate spinning rate adjustment

GAIN_SEL specify the gain of the analog chain (relative to GAIN_SEL=0)

GAIN_SEL<2:0>	Multiplication
0	1
1	1.25
2	1.66
3	2
4	2.5
5	3
6	3.75
7	5

Note:

1:When the BIST=1, Self test mode is enabled, in this mode we can detect magnetic output of Z axi s to acknowledge device status. Pls refer to application note to know how to detect device in self t est mode.

2:factor 5 is multiplication between GAIN_SEL=7(MAX) and GAIN_SEL=0(MIN).

6.2.2、Register:0x01

MSByte:

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
TRIG/INT	COMM_MODE[1]	COMM_MODE[0]	WOC_DIFF	EXT_TRIG	TCMP_EN	BURST_SET(zyxt)[z]	BURST_SET(zyxt)[y]

LSByte:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BURST_SET (zyxt)[x]	BURST_SET (zyxt)[t]	BURST_DATA _RATE[5]	BURST_DATA _RATE[4]	BURST_DATA _RATE[3]	BURST_DATA _RATE[2]	BURST_DATA _RATE[1]	BURST_DATA _RATE[0]

Register(0x01) description

TRIG/INT	Puts TRIG_INT pin in TRIG mode when cleared, INT mode otherwise
COMM_MODE[1:0]	Allow only SPI [10b], only I^{2}C [11b] or both [0Xb] according to CS pin
WOC_DIFF	Sets the Wake-up On Change based on Δ{sample(t),sample(t-1)} 0: The sampling data of current time (t) compare with the first sampling data of WOC mode. 1: The sampling data of current time (t) compare with the data of last time (t=t-1)
EXT_TRIG	Allows external trigger inputs when EXT_TRIG is set, if TRIG/INT = 0
TCMP_EN	Enables on-chip sensitivity drift compensation
BURST_DATARATE[6:0]	Defines TINTERVAL as BURST_DATA_RATE * 20ms

To make sure the activity on the SPI bus can't be accidentally interpreted as I2C protocol, programming bits are available in the memory of the dm110 to select the protocol. It concerns the COMM_MODE [1:0] bits with the following effect:

COMM_MODE[1]	COMM_MODE[0]	Description
0	X	The mode in which the first valid command is transmitted to the dm211 defines the operating mode (SPI or I^{2}C) for all its future commands, until a reset (hard or soft) is done.
1	0	SPI mode only
1	1	I^{2}C mode only

6.2.3、Register:0x02

MSByte:

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
			OSR2[1]	OSR2[0]	RES_XYZ_Z[1]	RES_XYZ_Z[0]	RES_XYZ_Y[1]

LSByte:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RES_XYZ_Y[0]	RES_XYZ_X[1]	RES_XYZ_X[0]	DIG_FILT[2]	DIG_FILT[1]	DIG_FILT[0]	OSR[1]	OSR[0]

Register(0x02) description

OSR2[1:0]	Temperature sensor ADC oversampling ratio
RES_XYZ[5:0]	Selectsthedesired16-bitoutput valuefromthe19-bitADC Every direction(X/Y/Z) has its own 2-bit parameter
DIG_FILT[2:0]	Digital filter applicable to ADC
OSR[1:0]	Magnetic sensor ADC oversampling ratio

RES_XYZ specify the resolution of the measurement：

The output of ADC is unsigned 19bits data. The output of the sensor would be 16bits which is selected from 19bits. Please refer to the table below:

Unsigned 16 bits sensor output(B_{OUT}):

RES_x/y/z<1:0>																			
0	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Change unsigned 16bits to signed 16bits:

RES_i	Unsigned 16bits	Signed 16bits
0	B_{OUT}	B_{OUT}
1	B_{OUT}	B_{OUT}
2	B_{OUT}	$B_{OUT}-2^{15}$
3	B_{OUT}	$B_{OUT}-2^{14}$

6.2.4、Register:0x03

MSByte:

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
SENS_TC_HT[7]	SENS_TC_HT[6]	SENS_TC_HT[5]	SENS_TC_HT[4]	SENS_TC_HT[3]	SENS_TC_HT[2]	SENS_TC_HT[1]	SENS_TC_HT[0]

LSByte:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SENS_TC_LT[7]	SENS_TC_LT[6]	SENS_TC_LT[5]	SENS_TC_LT[4]	SENS_TC_LT[3]	SENS_TC_LT[2]	SENS_TC_LT[1]	SENS_TC_LT[0]

Register(0x03) description

SENS_TC_HT[7:0]	Sensitivity drift compensation factor for $T<T_{REF}$

SENS_TC_LT[7:0]	Sensitivity drift compensation factor for $T>T_{REF}$

6.2.5、Register:0x04

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OFFSET_X[15:0]															

Register(0x04) description

OFFSET_X[15:0]	Constant X-offset correction

6.2.6、Register:0x05

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OFFSET_Y[15:0]															

Register(0x05) description

OFFSET_Y[15:0]	Constant Y-offset correction

6.2.7、Register:0x06

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OFFSET_Z[15:0]															

Register(0x06) description

OFFSET_Z[15:0]	Constant Z-offset correction

6.2.8、Register:0x07

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
WO_XY_THRESHOLD[15:0]															

Register(0x07) description

WO_XY_THRESHOLD[15:0]	Wake-up On Change XY-threshold

6.2.9、Register:0x08

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
WO_Z_THRESHOLD[15:0]															

Register(0x08) description

WO_Z_THRESHOLD[15:0]	Wake-up On Change Z-threshold

6.2.10、Register:0x09

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
WO_T_THRESHOLD[15:0]															

Register(0x09) description

WO_T_THRESHOLD[15:0]	Wake-up On Change T-threshold

7、Command List

Thedm110onlylistenstoaspecificsetofcommands.ApartfromtheResetcommand,allcommands generateastatusbytethatcanbereadout.Thetablebelowindicatesthe12differentcommandsthatare(c onditionally)acceptedbythedm110.

7.1、Command Table

Command					
Command Name	**Symbol**	**CMD1 byte[3]**	**CMD2 byte[3]**	**CMD3 byte[3]**	**CMD4 byte[3]**
No Operation	NOP	0000 0000	N/A	N/A	N/A
Start Burst Mode	SB	0001 zyxt[1]	N/A	N/A	N/A
Start Wake-up on Change Mode	SW	0010 zyxt[1]	N/A	N/A	N/A
Start Single Measurement Mode	SM	0011 zyxt[1]	N/A	N/A	N/A
Read Measurement	RM	0100 zyxt[1]	N/A	N/A	N/A
Read Register	RR	0101 0abc[2]	{A5… A0 ,0,0}	N/A	N/A
Write Register	WR	0110 0abc[2]	D 15 …D8	D 7… D0	{A5… A0 ,0 ,0 }
Exit Mode	EX	1000 0000	N/A	N/A	N/A
Memory Recall	HR	1101 0000	N/A	N/A	N/A
Memory Store	HS	1110 0000	N/A	N/A	N/A
Reset	RT	1111 0000	N/A	N/A	N/A

Note:

1. The argument in all mode-starting commands (SB/SW/SM) is a nibble specifying the conversions to be performed by the sensor in the following order «zyxt». For example, if only Y axis and temperature are to be measured in Single Measurement mode the correct command to be transmitted is 0x35h.
2. The argument for the volatile memory access commands (RR/WR) «abc» should be set to 0x0h, in order to get normal read-out and write of the memory.
3. CMD byte have to been sent before start repeat.

7.2、Status byte

The status byte is the first byte transmitted by the dm211 in response to a command issued by the master. It is composed of a fixed combination of informative bits:

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BURST_MODE	WOC_MODE	SM_MODE	ERROR	SED	RS	D1	D0

MODE bits

These bits define in which mode the dm211 is currently set. Whenever a mode transition command is rejected, the first status byte after this command will have the expected mode bit cleared, which serves as an indication that the command has been rejected, next to the ERROR bit. The SM_MODE flag can be the result of an SM command or from raising the TRIG pin when TRIG mode is enabled in the volatile memory of the dm211.

ERROR bit

This bit is set in case a command has been rejected or in case an uncorrectable error is detected in the memory, a so called ECC_ERROR. A single error in the memory can be corrected (see SED bit), two errors can be detected and will generate the ECC_ERROR. In such a case all commands but the RT (Reset) command will be rejected.

SED bit

The single error detection bit simply flags that a bit error in the non-volatile memory has been corrected. It is purely informative and has no impact on the operation of the dm211.

RS bit

Whenever the dm211 gets out of a reset situation – both hard and soft reset – the RS flag is set to highlight this situation to the master in the first status byte that is read out. As soon as the first status byte is read, the flag is cleared until the next reset occurs.

D[1:0] bits

These bits only have a meaning after the RR and RM commands, when data is expected as a response from the dm211. The number of response bytes correspond to 2*D[1:0] + 2, so the expected byte counts are either 2, 4, 6 or 8.

7.3、Command Usage:

All of the command usage should follow the sequence, each command has its own input and output bytes, output byte can be found in the command list table, only RR and RM has input bytes.

7.3.1、Example of command usage

Start	I2C _ADDR[6:0]	Write bit “0”	A	CMD1byte	A	CMD bytes[1]

Sr	I2C _ADDR[6:0]	Read bit “1”	A	Status byte	A	Input bytes	NA	P

7.3.2、Read measurement RM

The command read measurement can get the sensor rate while the dm110 set out a int signal, generally speaking, the amounts of input bytes depends on the argument of <zyxt> in mode command, each bit represent two bytes of rate data, the RATA data order is fixed as temperature rate, rateX, rateY, rateZ. If we want's rateZ only, the sequence of I2C should follow the rule:

Start	I2C _ADDR[6:0]	Write bit "0"	A	CMD bytes	A

Sr	I2C _ADDR[6:0]	Read bit "1"	A	Status byte	A	Z-rate high byte	A	Z-rate low byte	NA	P

If we want to acquire all of the data, the sequence of I2C should be organized as bellow:

Start	I2C _ADDR[6:0]	Write bit "0"	A	RM	A

Sr	I2C _ADDR[6:0]	Read bit "1"	A	Status byte	A	Temperature high byte	A

Temperature low byte	A	X Rate high byte	A	X Rate low byte	A	Y Rate high byte	A

Y Rate low byte	A	Z Rate high byte	A	Z Rate low byte	NA	P

From dm110 to master

From master to dm110

7.3.3、Read Register(RR)

The volatile memory data can be read out by the command of read register(RR). The command byte should be followed while the I2C writing address has been sent out. Before a restart of I2C protocol, the register address needed, then the register data will be received following a read I2C address.

Start	I2C _ADDR[6:0]	Write bit “0”	A	CMD1byte(RR)	A	Register address	A

Sr	I2C _ADDR[6:0]	Read bit “1”	A	Status byte	A	Data high byte	A	Data low byte	NA	P

From dm110 to master

From master to dm110

7.3.4、Other commands

The usage of left commands is quite easy for they do not have input or output bytes, just follow the sequence bellow completely.

Start	I2C _ADDR[6:0]	Write bit “0”	A	CMD1byte	A	Sr	I2C _ADDR[6:0]	Read bit “1”	A	Status byte	NA	P

From dm110 to master

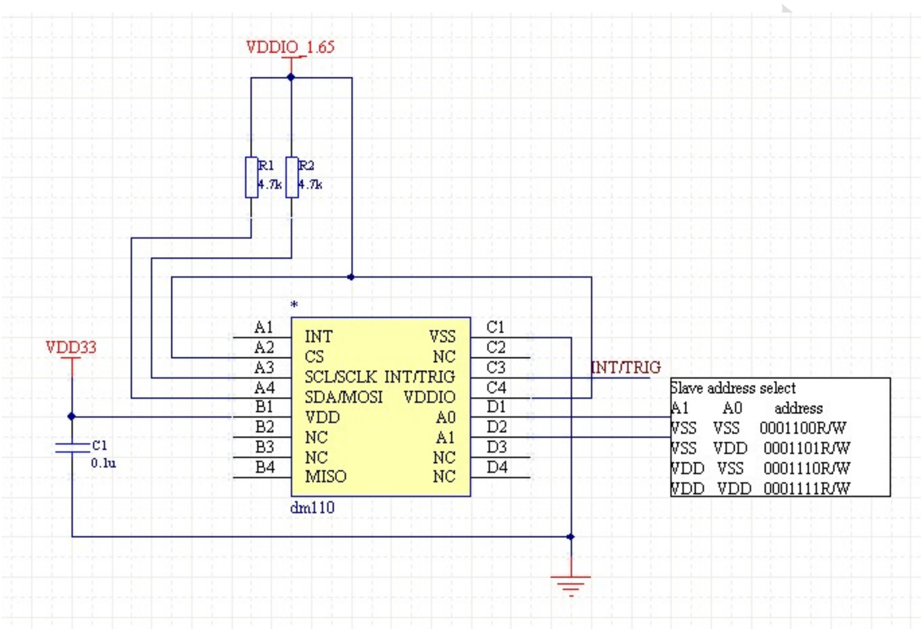
From master to dm110

8、Typical application

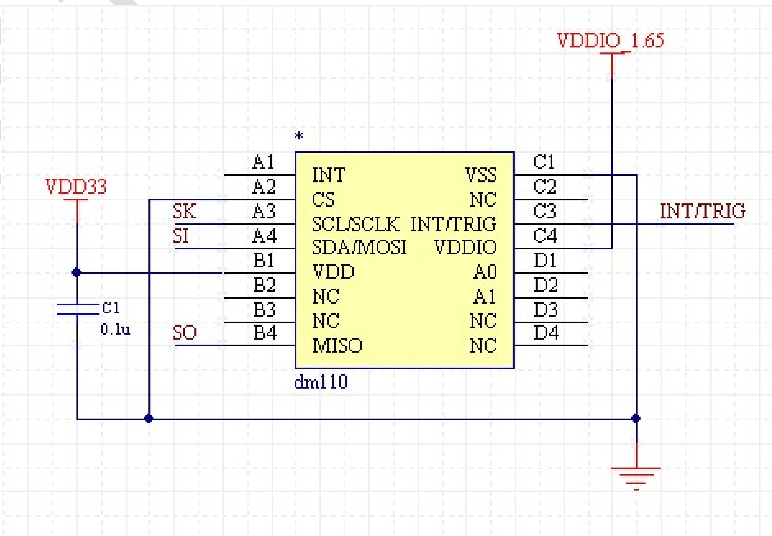
Recommended external electrical connection:

- I2C bus interface
- 4-wire SPI interface

8.1、I2C bus interface external connection

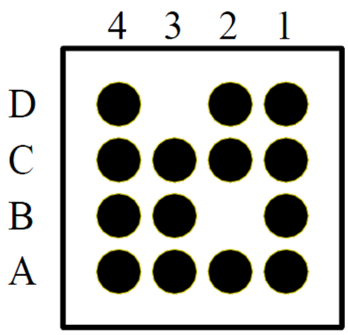


8.2、4-wire SPI interface external connection



9、Package information

9.1、Pin Assignment

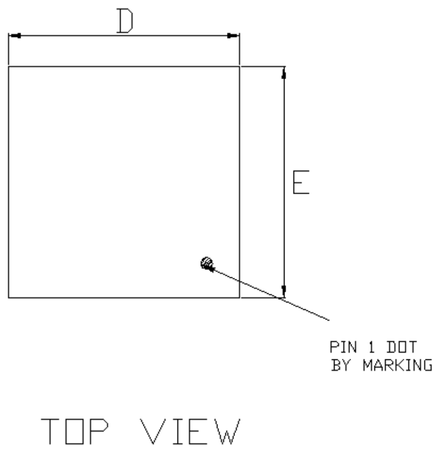


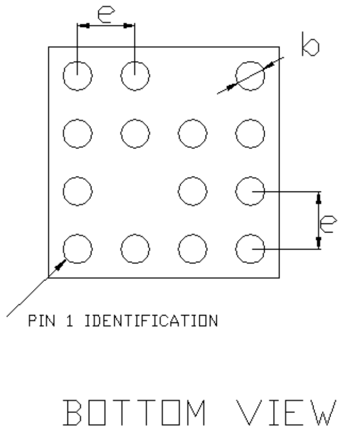
<Top view>

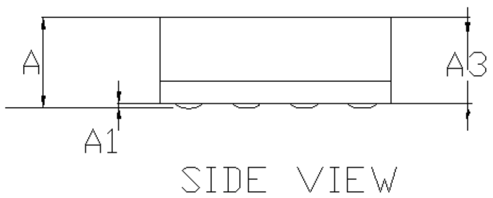
TOP VIEW	4	3	2	1
D	NC	NC	A1	A0
C	VDDIO	INT/TRIG	NC	VSS
B	MISO	NC	NC	VDD
A	SDA/MOSI	SCL/SCLK	CS	INT

9.2、 outline dimensions

dm110 Flip-BGA package







COMMON DIMENSIONS(MM)			
PKG.	WVERYVERY THIN		
REF.	MIN.	NOM.	MAX
A	0.79	0.84	0.89
A1	0.1	0.13	0.15
A3	0.71 REF.		
D	1.5	1.6	1.7
E	1.5	1.6	1.7
b	D 0.2 REF		
e	0.4 BSC		

10、Revision History

Data	Revision	Changes
2013-7-8	1.0	Initial release

11、Sales and support

Products supported by a preliminary data sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

AE:
TEL: 86-512-65926260-8017
Website:www.miramems.com

PLEASE READ CAREFULLY

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