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TPD3E001 Low-Capacitance 3-Channel ESD-Protection for High-Speed Data Interfaces

1 Features

- IEC61000-4-2 Level-4 ESD Protection
  - ±8-kV IEC 61000-4-2 Contact Discharge
  - ±15-kV IEC 61000-4-2 Air-Gap Discharge
- 5.5-A Peak Pulse Current (8/20-µs Pulse)
- I/O Capacitance: 1.5 pF (Typical)
- Low Leakage Current: 1-nA (Maximum)
- Low Supply Current: 1-nA (Typical)
- 0.9-V to 5.5-V Supply-Voltage Range
- Space-Saving DRY, DRL, and DRS Package Options
- Alternate 2-, 4-, and 6-Channel Options Available: TPD2E2U06, TPD4E1U06, and TPD6E001

2 Applications

- End Equipments
  - Blood Glucose Meters
  - Video Surveillance Equipment
  - Portable Data Terminal
  - Industrial Monitor
- Interfaces
  - USB2.0
  - SDIO
  - Precision Analog Interface
  - SVGA Video Connections

3 Description

The TPD3E001 is a three-channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array. The TPD3E001 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4). This device has a 1.5-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces. The ultra low leakage current (<1 nA max) is suitable for precision analog measurements in applications like glucose meters and heart rate monitors.

The TPD3E001 is available in space saving DRY (USON), DRL (SOT), and DRS (WSON) packages and is specified for –40°C to 85°C operation. Also see TPD2E2U06, TPD4E1U06, and TPD6E001 which are 2, 4, and 6 channel ESD protection options, respectively, for ESD protection diode arrays with a different number of channels. The TPD2E2U06 provides a higher level of IEC ESD protection, when compared to the TPDxE001 family, and removes the need for an input capacitor. The TPD4E1U06 removes the need for an input capacitor, provides higher IEC ESD protection, and provides lower capacitance, when compared to the TPDxE001 family.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD3E001	SOT (5)	1.60 mm × 1.20 mm
	WSON (6)	3.00 mm × 3.00 mm
	USON (6)	1.45 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Schematic

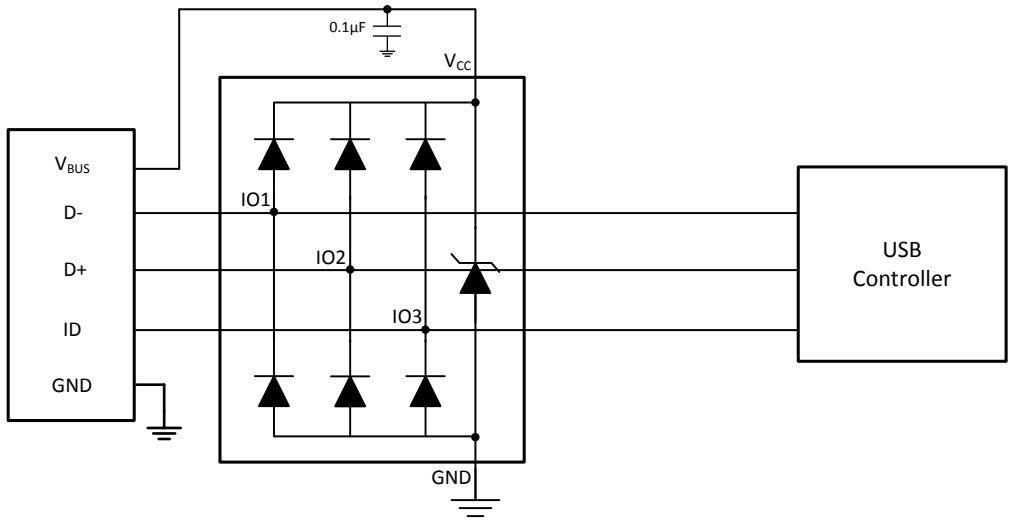


Table of Contents

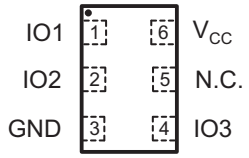
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

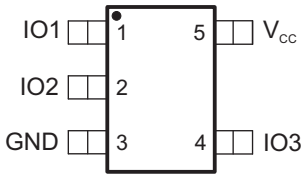
Changes from Revision E (April 2013) to Revision F	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

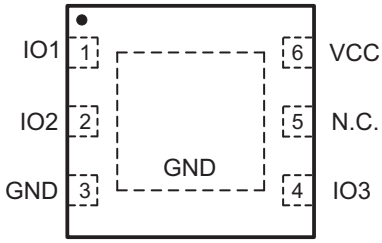
DRY Package
6-Pin USON
Top View



DRL Package
5-Pin SOT
Top View



DRS Package
6-Pin WSON
Top View



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	DRY NO.	DRL NO.	DRS NO.		
IOx	1, 2, 4	1, 2, 4	1, 2, 4	I/O	ESD-protected channel
GND	3	3	3	GND	Ground
V_{CC}	6	5	6	Power	Power-supply input. Bypass V_{CC} to GND with a 0.1-µF ceramic capacitor.
N.C.	5	–	5	–	No connection. Not internally connected.
EP	–	–	Exposed Thermal Pad	GND	Exposed thermal pad. Connect to GND or leave floating.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}		–0.3	7	V
$V_{I/O}$	IO voltage tolerance	–0.3	V_{CC} + 0.3	V
T_J	Junction temperature		150	°C
	Lead temperature (soldering, 10 s)		300	°C
	Peak pulse power (tp = 8/20 µs)		90	W
	Peak pulse power (tp = 8/20 µs)		5.5	A
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±15000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		IEC 61000-4-2 Contact Discharge	±8000	
		IEC 61000-4-2 Air-gap Discharge	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Operating Voltage	V_{CC} Pin	0.9		5.5	V
	IOx Pin	0		V_{CC}	
Operating free-air temperature, T_A		-40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPD3E001			UNIT
		DRL (SOT)	DRS (WSON)	DRY (USON)	
		5 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	266.3	91.9	374.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	111.5	106.9	223.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.5	64.8	227.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.0	10.2	52.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.0	64.9	224.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	29.9	87.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

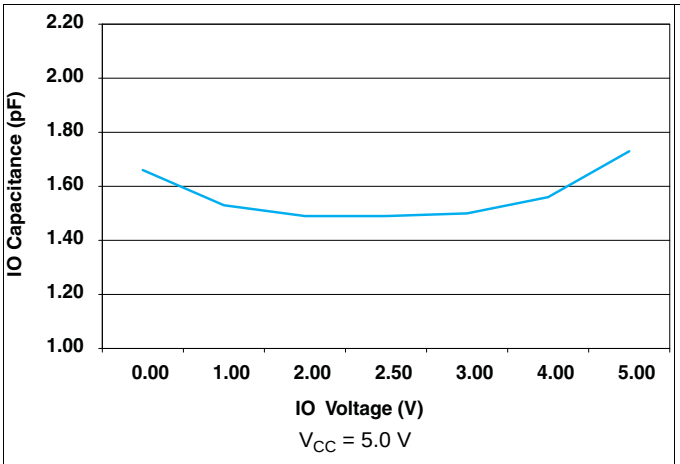
6.5 Electrical Characteristics

V_{CC} = 5 V ± 10%, T_A = -40°c to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{CC}	Supply voltage			0.9		5.5	V
I_{CC}	Supply current				1	100	nA
V_F	Diode forward voltage	I_F = 10 mA		0.65		0.95	V
V_{BR}	Breakdown Voltage	I_{BR} = 10mA		11			V
V_C	Channel clamp voltage(2)	T_A = 25°C, ±15-kV HBM, I_F = 10 A	Positive transients			V_{CC} + 25	V
			Negative transients			–25	
		T_A = 25°C, ±8-kV Contact Discharge (IEC 61000-4-2), I_F = 24 A	Positive transients			V_{CC} + 60	
			Negative transients			–60	
		T_A = 25°C, ±15-kV Air-Gap Discharge (IEC 61000-4-2), I_F = 45 A	Positive transients			V_{CC} + 100	
			Negative transients			–100	
$I_{i/o}$	Channel leakage current	$V_{i/o}$ = GND or V_{CC}				±1	nA
C_{io}	Channel input capacitance	V_{CC} = 5 V, bias of V_{CC}/2			1.5		pF
R_{dyn}	Dynamic resistance	$I_{i/o}$ = 1 A, between IO pin and ground			1.2		Ω

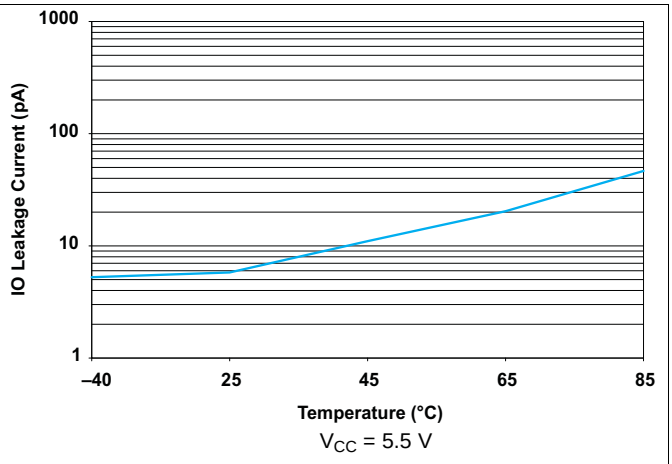
(1) Typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) Channel clamp voltage is not production tested.

6.6 Typical Characteristics



V_{CC} = 5.0 V

Figure 1. IO Capacitance vs IO Voltage



V_{CC} = 5.5 V

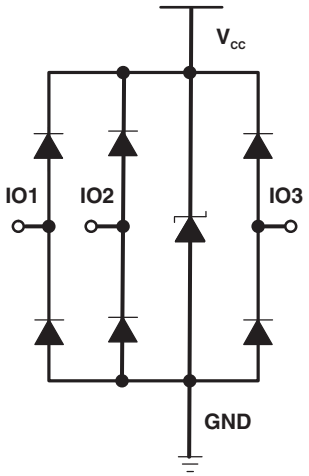
Figure 2. IO Leakage Current vs Temperature

7 Detailed Description

7.1 Overview

The TPD3E001 is a three-channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array. The TPD3E001 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4). This device has a 1.5-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces. The ultra low leakage current (< 1 nA maximum) is suitable for precision analog measurements in applications like glucose meters and heart rate monitors. The wide voltage range on V_{CC} (up to 5.5V) gives this device the flexibility to be used in a wide variety applications. Having 3-channels of ESD protection makes this device particularly well suited to protect a micro-AB USB connector, which has three signal lines to be protected (D+, D-, ID). The V_{BUS} pin can also be protected by connecting it to V_{CC} on TPD3E001. Therefore, TPD3E001 is a one-chip solution to provide Level 4 IEC 61000-4-2 ESD protection on every pin of the micro-AB USB connector.

7.2 Functional Block Diagram



7.3 Feature Description

TPD3E001 is a uni-directional ESD protection device with low capacitance. The device is constructed with a central ESD clamp that features two hiding diodes per line to reduce the capacitive loading. This central ESD clamp is also connected to V_{CC} to provide protection for the V_{CC} line. Each IO line is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 level 4 international standard. The TPD3E001's low loading capacitance makes it ideal for protection high-speed signal terminals.

7.4 Device Functional Modes

TPD3E001 is a passive-integrated circuit that activates whenever voltages above V_{BR} or below the lower diodes $V_{forward}$ (–0.6V) are present upon the circuit being protected. During ESD events, voltages as high as ±15 kV can be directed to ground and V_{CC} via the internal diode network. Once the voltages on the protected lines fall below the trigger voltage of the TPD3E001 (usually within 10's of nano-seconds) the device reverts back to a high-impedance state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPD3E001 is a diode array type Transient Voltage Suppressor (TVS) which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

8.2 Typical Application

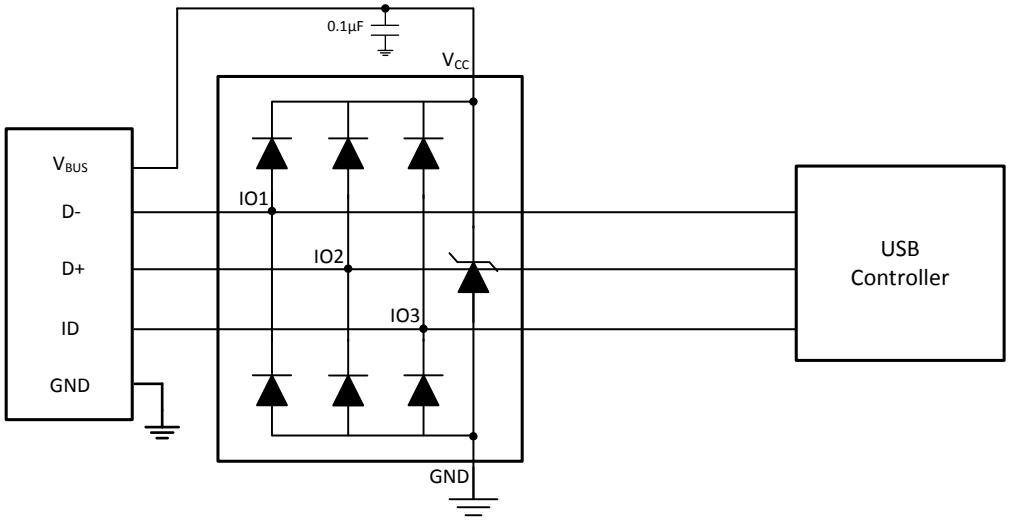


Figure 3. Typical Application Schematic

8.2.1 Design Requirements

For this design example, a single TPD3E001 is used to protect all the pins of a USB2.0 micro-AB connector. The micro-AB connector has an extra pin, the ID pin, which is used by the device to determine whether it is to perform the "A" role or the "B' role. This functionality the ID offers is part of the USB On-the-Go (OTG) Standard. The TPD3E001 offers 3-channels of IEC Level ESD protection to provide complete protection for the USB micro-AB style connector, plus V_{CC} (V_{BUS}, D+, D-, ID).

Given the USB application, the following parameters are known.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Signal range on IO1, IO2	0 V to 3.6 V
State of IO3 (ID)	GND or Floating
Signal voltage range on V_{CC}	0 V to 5.25 V
Operating Frequency	240 MHz

8.2.2 Detailed Design Procedure

When placed near the USB connectors, the TPD3E001 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD3E001 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, the following layout/ design guidelines should be followed:

1. Place the TPD3E001 solution close to the connectors. This allows the TPD3E001 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1-µF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD3E001 consumes approximately 1 nA (typ.) supply current through the V_{CC} and GND loop. But during the ESD event, V_{CC} and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating. In this example of protecting a micro-AB type USB port, none of the IO pins will be left unused.
5. The V_{CC} pin can be connected in two different ways:
   (a) If the V_{CC} pin is connected to the system power supply, the TPD3E001 works as a transient suppressor for any signal swing above V_{CC} + V_F. A 0.1-µF capacitor on the device V_{CC} pin is recommended for ESD bypass.
   (b) If the V_{CC} pin is not connected to the system power supply, the TPD3E001 can tolerate higher signal swing in the range up to 10 V. Please note that a 0.1-µF capacitor is still recommended at the V_{CC} pin for ESD bypass.

8.2.3 Application Curve

Figure 4 is a capture of the voltage clamping waveform of TPD3E001 on IO1 during a +8kV Contact IEC61000-4-2 ESD strike.

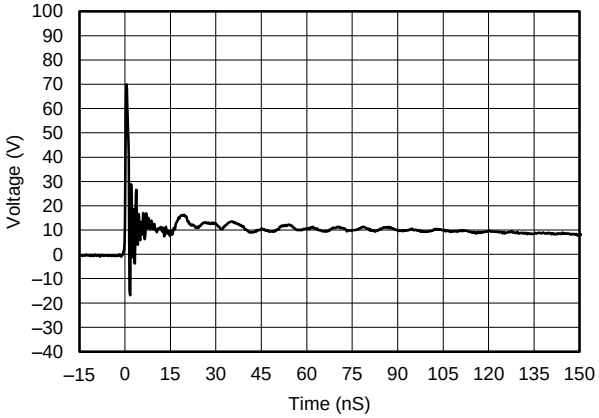


Figure 4. TPD3E001 +8kV Contact IEC61000-4-2 Voltage Clamping Waveform

9 Power Supply Recommendations

TPD3E001 is a passive TVS diode, so there is no requirement to power this device. However, for best IEC 61000-4-2 ESD performance and lowest capacitance performance, it is recommended that the V_{CC} pin is biased with a 5V supply and that a 0.1µF capacitor is placed near the V_{CC} pin. Take care to make sure that the maximum voltage specification for the V_{CC} pin is not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

Figure 5 is an example of how to layout three data lines with the TPD3E001. One example could be protecting a USB micro-AB connector from IEC ESD, as discussed in the Application and Implementation section.

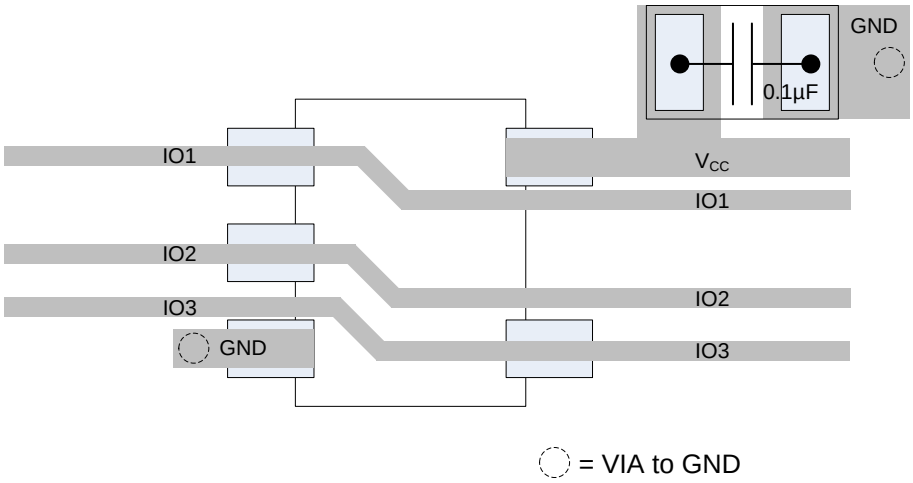


Figure 5. Routing with the DRL Package

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

1. TPD2E2U06 Data Sheet, SLLSEG9
2. TPD4E1U06 Data Sheet, SLVSBQ9
3. TPD6E001 Data Sheet, SLLS685

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD3E001DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2BR 2BH	Samples
TPD3E001DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2BR 2BH	Samples
TPD3E001DRSR	ACTIVE	SON	DRS	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWL	Samples
TPD3E001DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2B	Samples
TPD3E001DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

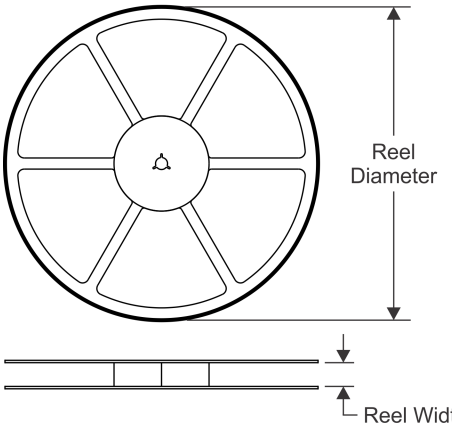
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

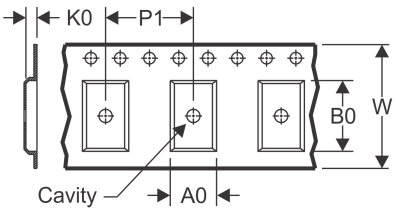
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

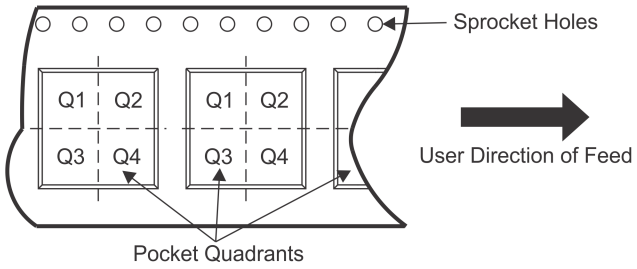


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

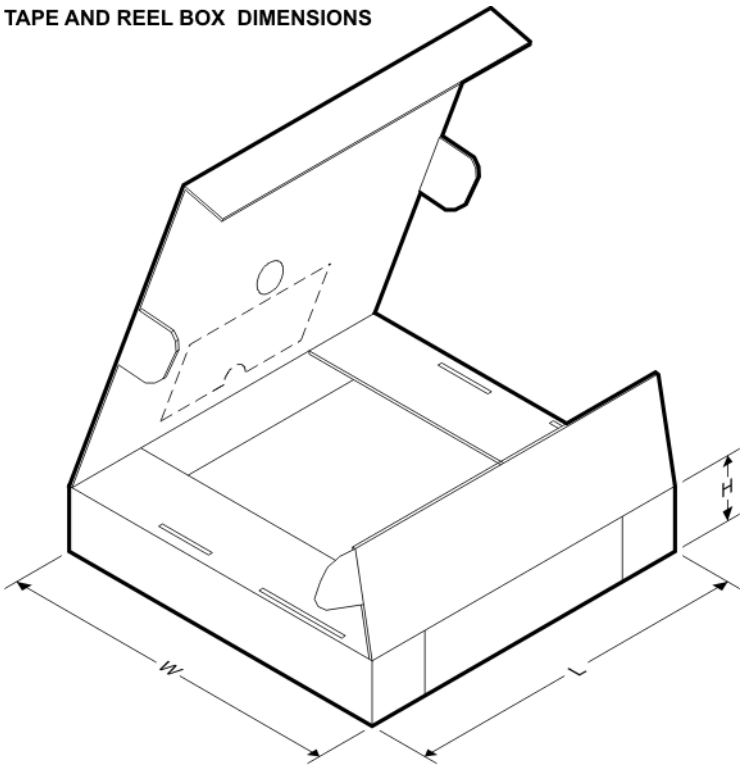
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

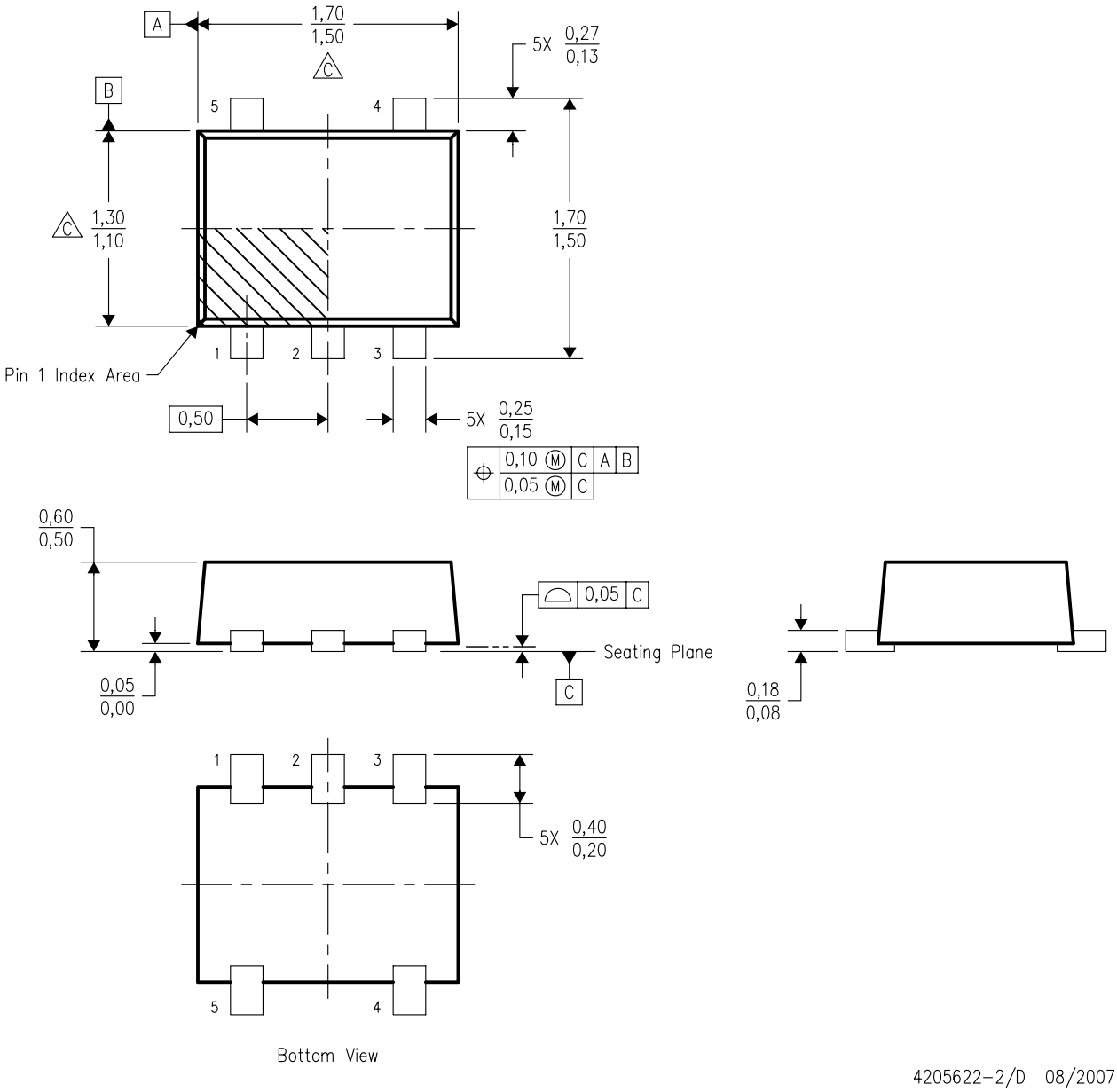
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD3E001DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TPD3E001DRSR	SON	DRS	6	1000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPD3E001DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

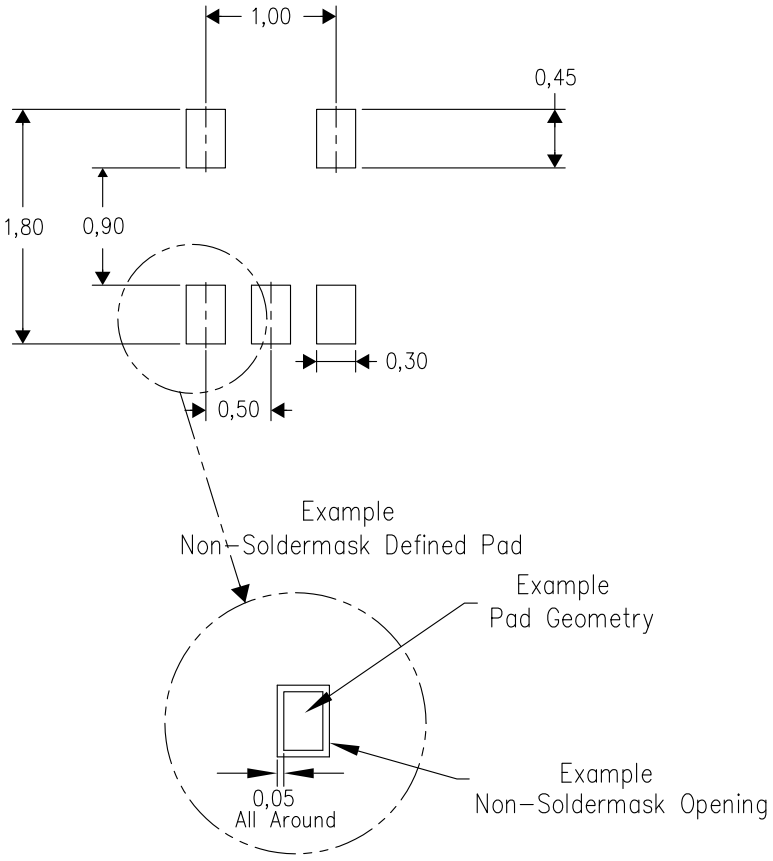
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD3E001DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
TPD3E001DRSR	SON	DRS	6	1000	367.0	367.0	35.0
TPD3E001DRYR	SON	DRY	6	5000	203.0	203.0	35.0



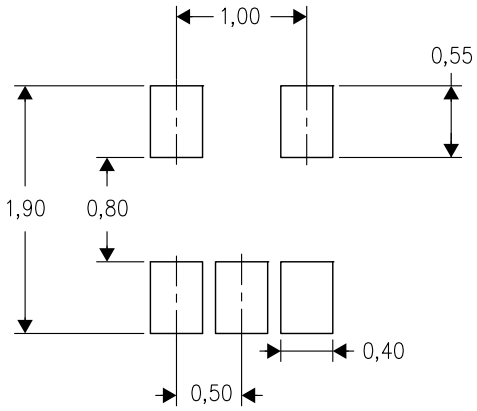
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE

Example Board Layout



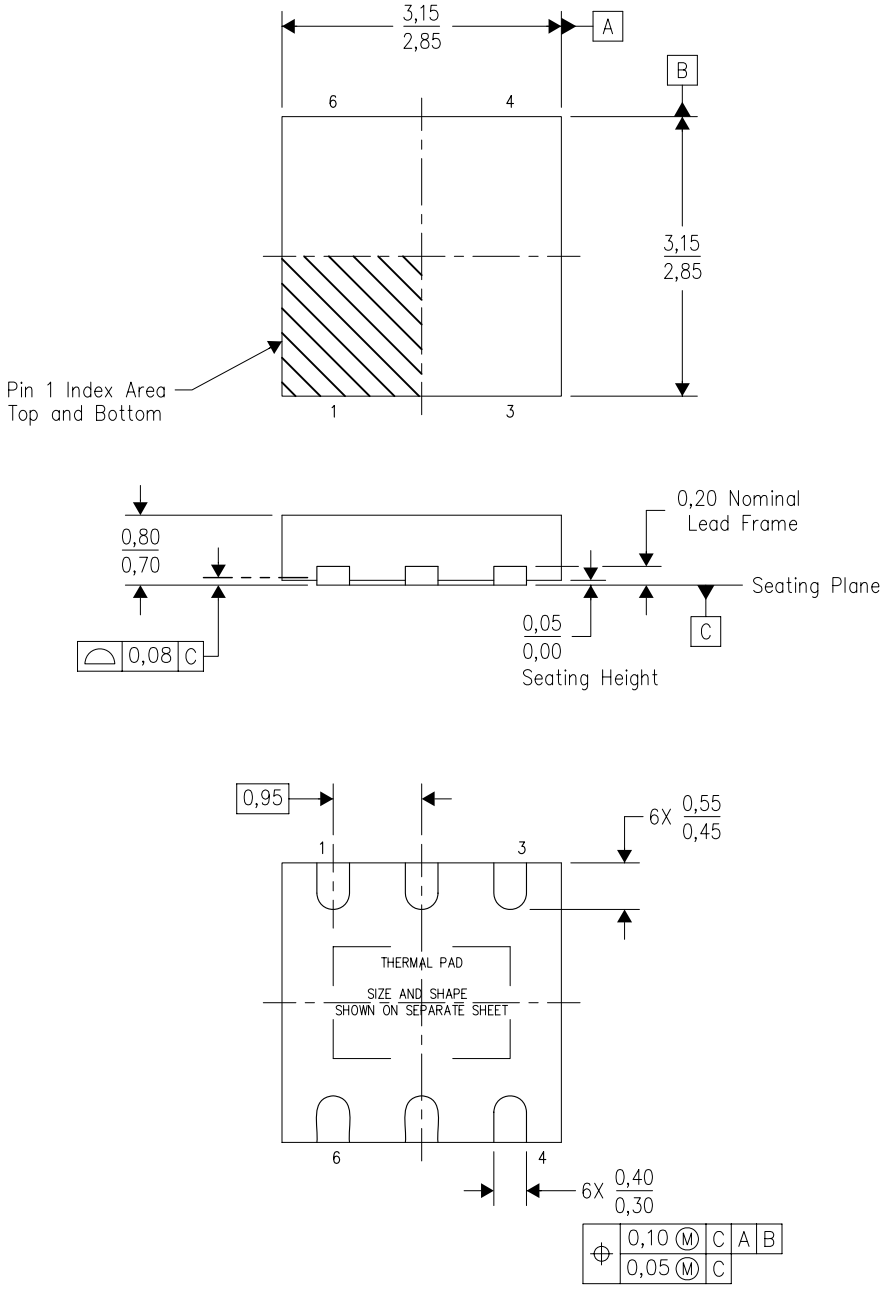
Example Stencil Design
(Note E)



4208207–2/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206219/F 07/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

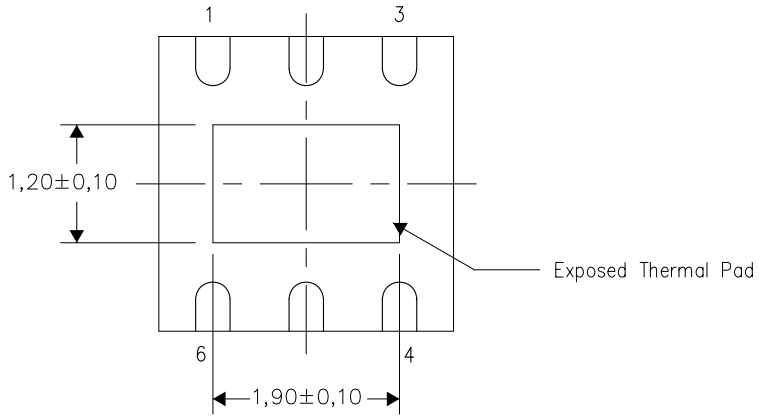
DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



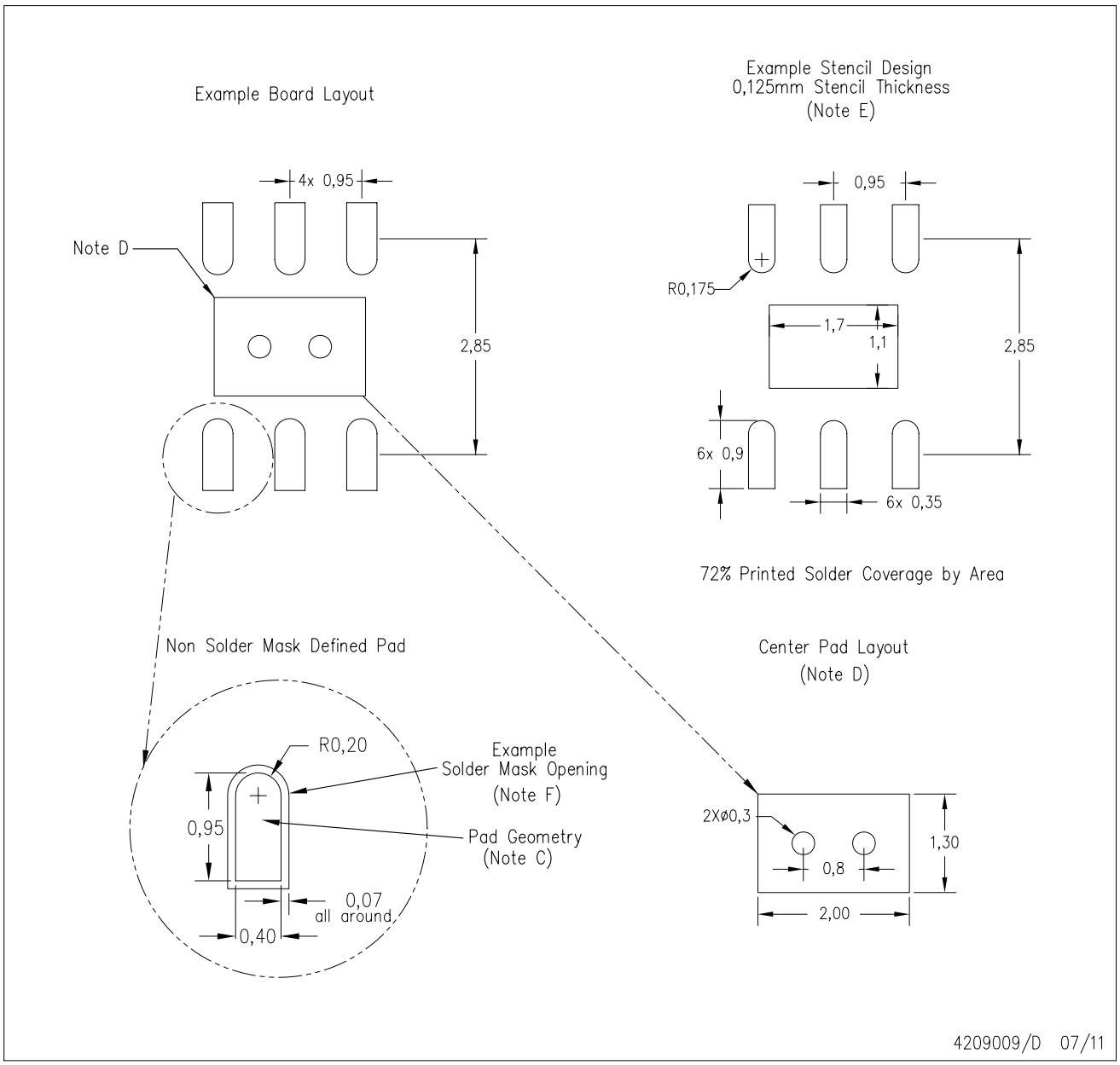
Bottom View

Exposed Thermal Pad Dimensions

4207663/E 07/11

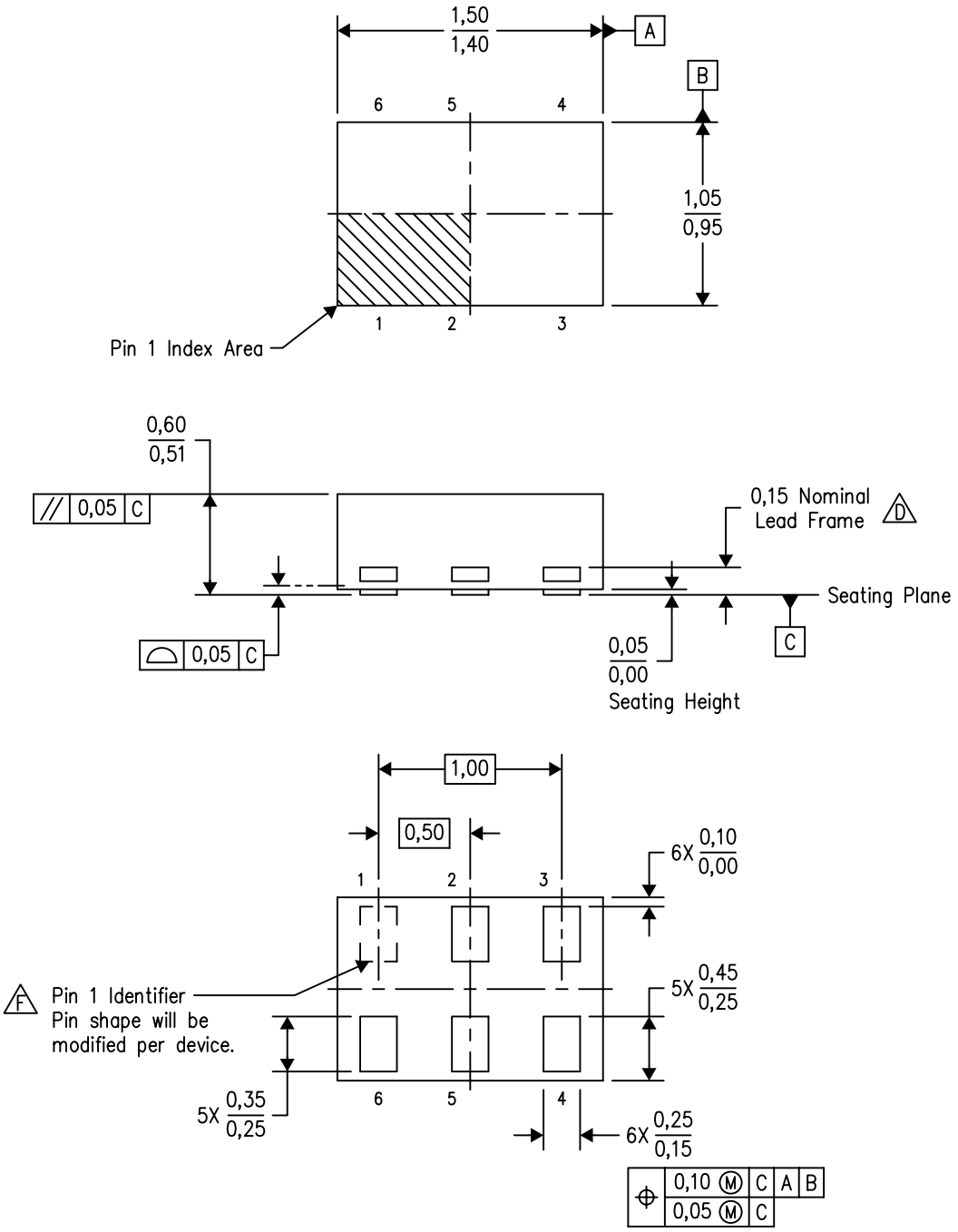
NOTE: All linear dimensions are in millimeters

DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

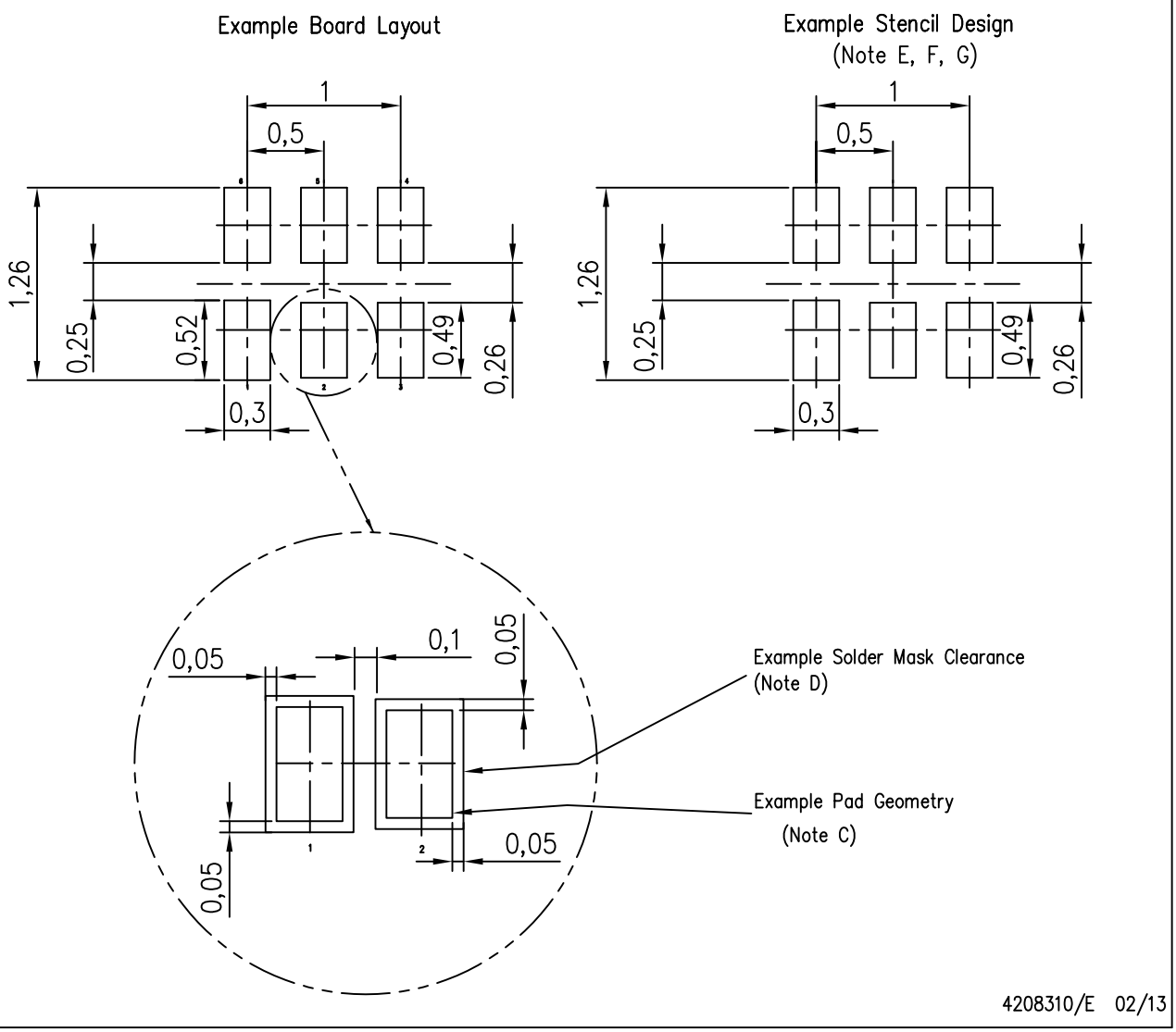
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4207181/F 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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