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International IƆR Rectifier

SMPS MOSFET

IRFR220NPbF
IRFU220NPbF

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max (mΩ)	I_D
200V	600	5.0A
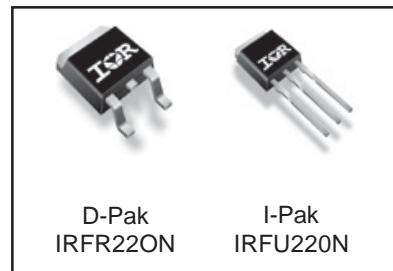
Applications
- High frequency DC-DC converters
- Lead-Free

Benefits
- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

D-Pak
IRFR22ON

I-Pak
IRFU220N

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	5.0	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	3.5	A
I_{DM}	Pulsed Drain Current ①	20	
P_D @T_C = 25°C	Power Dissipation	43	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ③	7.5	V/ns
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Typical SMPS Topologies

- Telecom 48V input Forward Converters

Notes ①   through ⑤ are on page 10

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.23	—	V/°C	Reference to 25°C, I_D = 1mA ④
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	600	mΩ	V_{GS} = 10V, I_D = 2.9A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 200V, V_{GS} = 0V
		—	—	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	2.6	—	—	S	V_{DS} = 50V, I_D = 2.9A
Q_g	Total Gate Charge	—	15	23	nC	I_D = 2.9A
Q_{gs}	Gate-to-Source Charge	—	2.4	3.6		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	6.1	9.2		V_{GS} = 10V,
$t_{d(on)}$	Turn-On Delay Time	—	6.4	—	ns	V_{DD} = 100V
t_r	Rise Time	—	11	—		I_D = 2.9A
$t_{d(off)}$	Turn-Off Delay Time	—	20	—		R_G = 24Ω
t_f	Fall Time	—	12	—		V_{GS} = 10V ④
C_{iss}	Input Capacitance	—	300	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	53	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	15	—		f = 1.0MHz
C_{oss}	Output Capacitance	—	300	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	23	—		V_{GS} = 0V, V_{DS} = 160V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	46	—		V_{GS} = 0V, V_{DS} = 0V to 160V ⑤
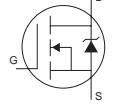
Avalanche Characteristics
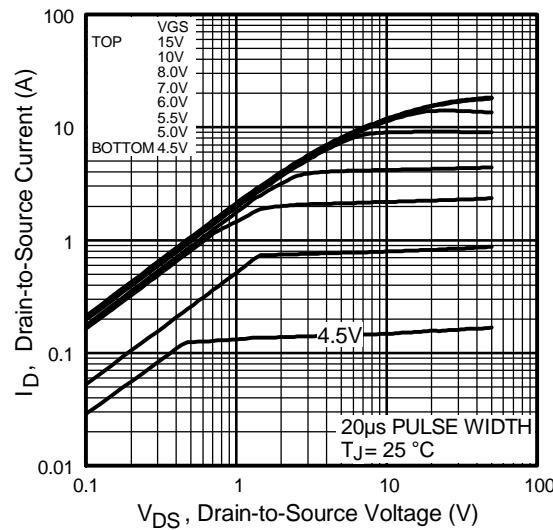
	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	46	mJ
I_{AR}	Avalanche Current①	—	2.9	A
E_{AR}	Repetitive Avalanche Energy①	—	4.3	mJ

Thermal Resistance
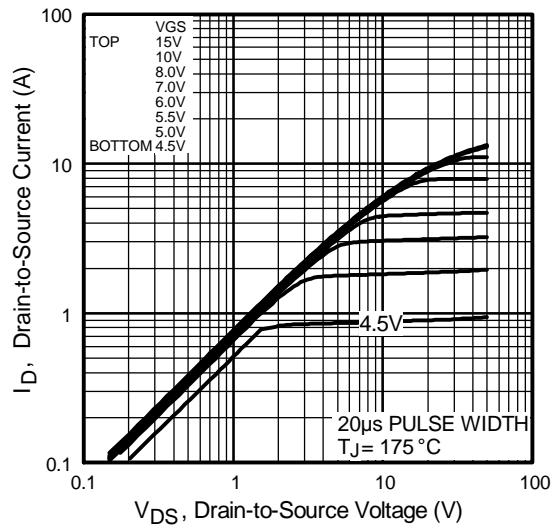
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.5	
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Diode Characteristics
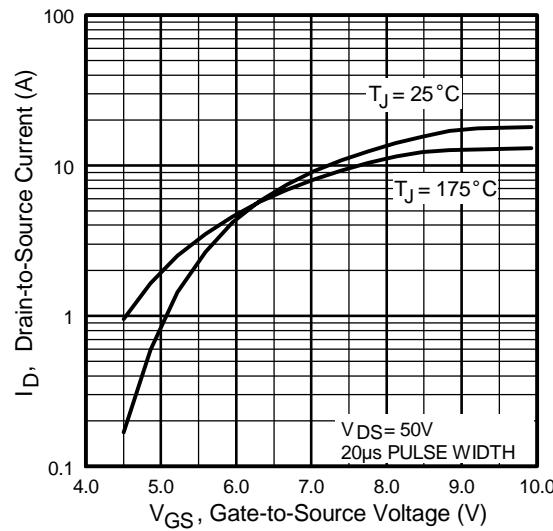
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	20		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 2.9A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	90	140	ns	T_J = 25°C, I_F = 2.9A
Q_{rr}	Reverse RecoveryCharge	—	320	480	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				
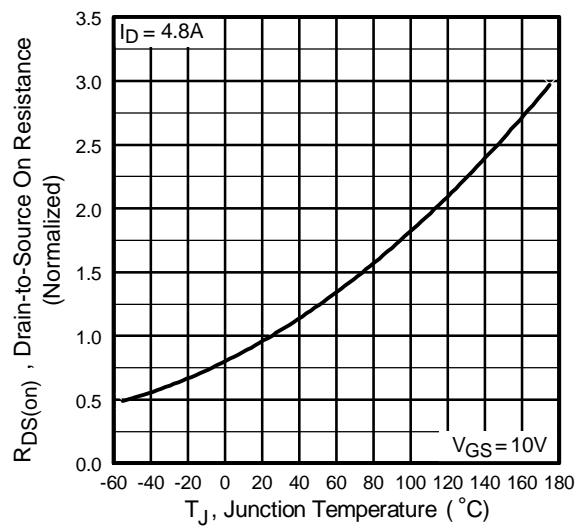
# IRFR/U220NPbF

**Fig 1.** Typical Output Characteristics

Fig 2. Typical Output Characteristics
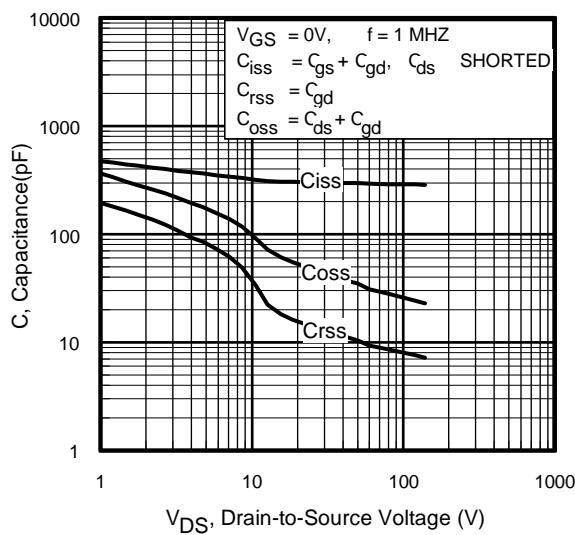

**Fig 3.** Typical Transfer Characteristics
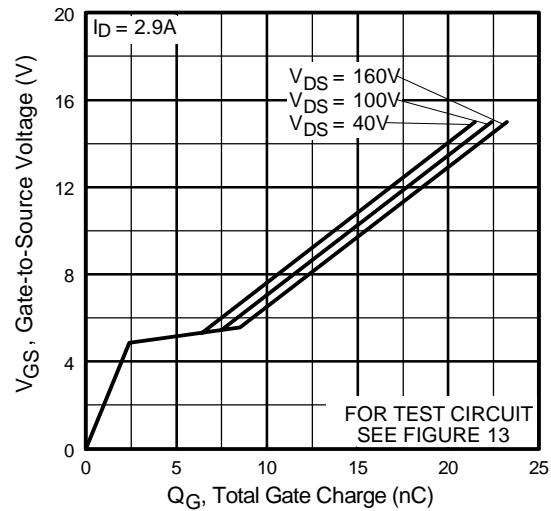
**Fig 4.** Normalized On-Resistance
Vs. Temperature

IRFR/U220NPbF
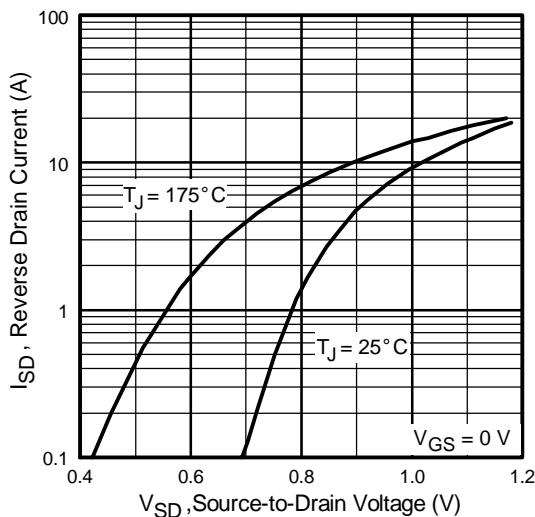
International
I⊕R Rectifier
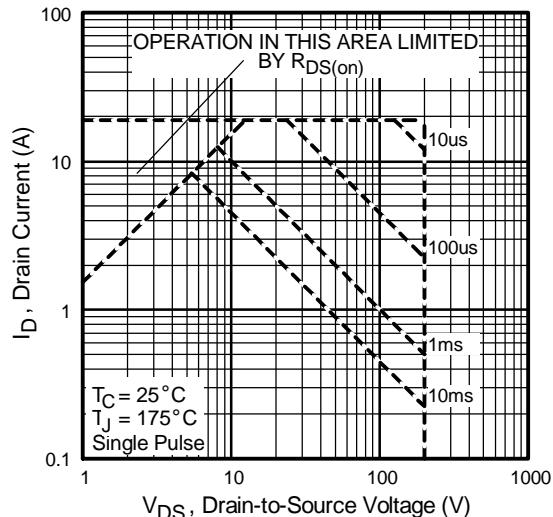
Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

In Fig 5:
$V_{GS} = 0V$, $f = 1$ MHZ
$C_{iss} = C_{gs} + C_{gd}$, C_{ds} SHORTED
$C_{rss} = C_{gd}$
$C_{oss} = C_{ds} + C_{gd}$

C, Capacitance(pF)
Ciss
Coss
Crss
V_{DS}, Drain-to-Source Voltage (V)
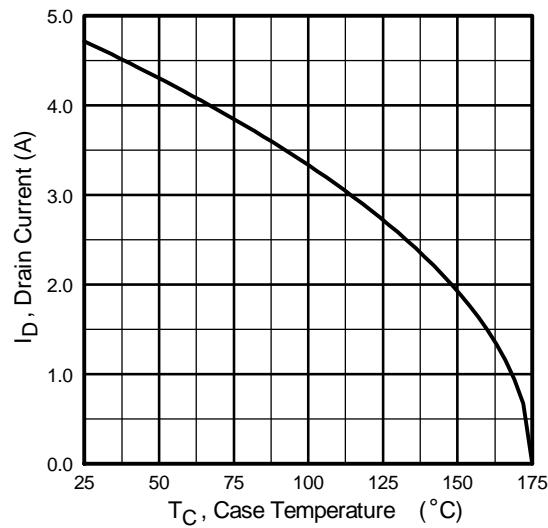
Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

In Fig 6:
$I_D = 2.9A$
$V_{DS} = 160V$
$V_{DS} = 100V$
$V_{DS} = 40V$
FOR TEST CIRCUIT SEE FIGURE 13
V_{GS}, Gate-to-Source Voltage (V)
Q_G, Total Gate Charge (nC)
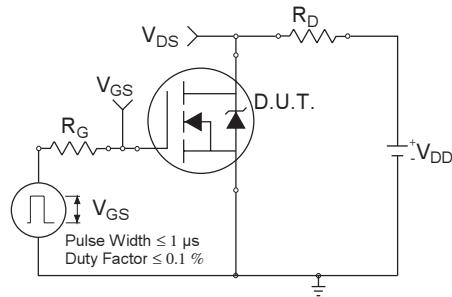
Fig 7. Typical Source-Drain Diode
Forward Voltage

In Fig 7:
I_{SD}, Reverse Drain Current (A)
$T_J = 175°C$
$T_J = 25°C$
$V_{GS} = 0$ V
V_{SD}, Source-to-Drain Voltage (V)
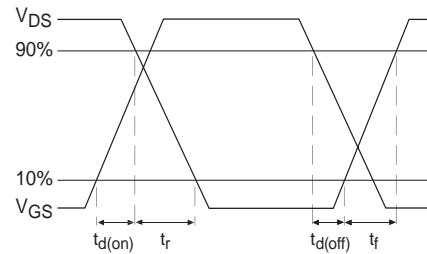
Fig 8. Maximum Safe Operating Area

In Fig 8:
OPERATION IN THIS AREA LIMITED BY $R_{DS(on)}$
10us
100us
1ms
10ms
$T_C = 25°C$
$T_J = 175°C$
Single Pulse
I_D, Drain Current (A)
V_{DS}, Drain-to-Source Voltage (V)

4
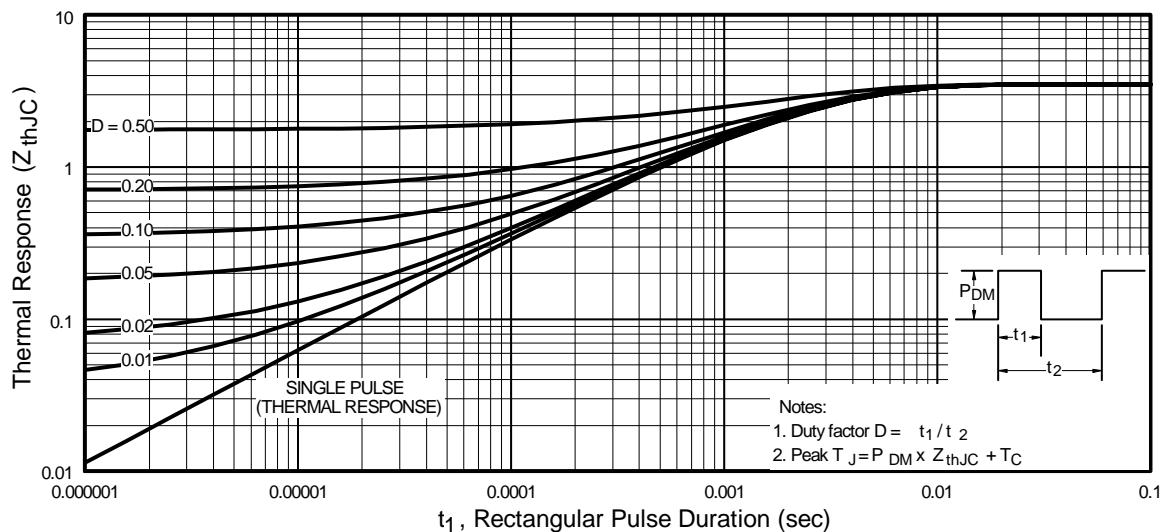
**Fig 9.** Maximum Drain Current Vs. Case Temperature

Fig 10a. Switching Time Test Circuit
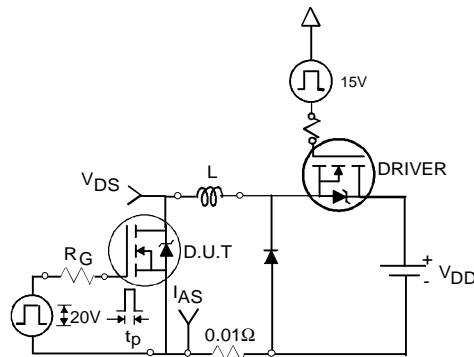

Fig 10b. Switching Time Waveforms

Notes:
1. Duty factor $D = t_1 / t_2$
2. Peak $T_J = P_{DM} \times Z_{thJC} + T_C$
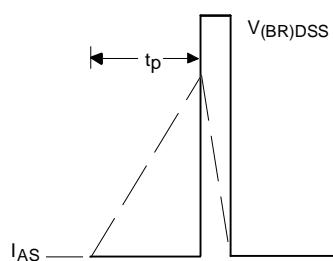
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRFR/U220NPbF

**Fig 12a.** Unclamped Inductive Test Circuit
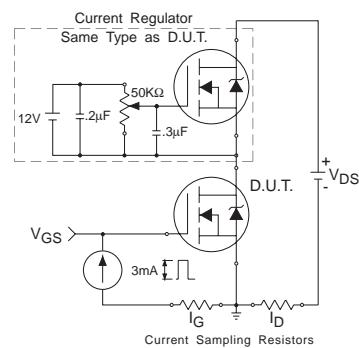
Fig 12b. Unclamped Inductive Waveforms


Fig 12c. Maximum Avalanche Energy Vs. Drain Current
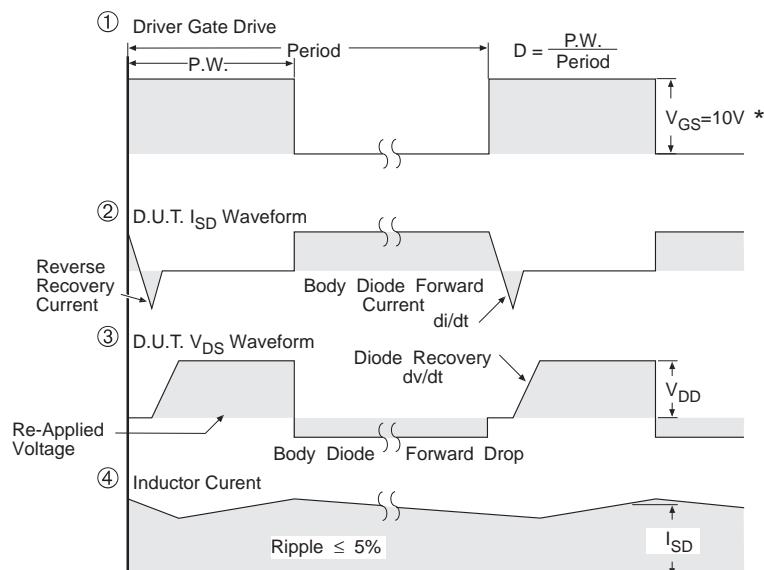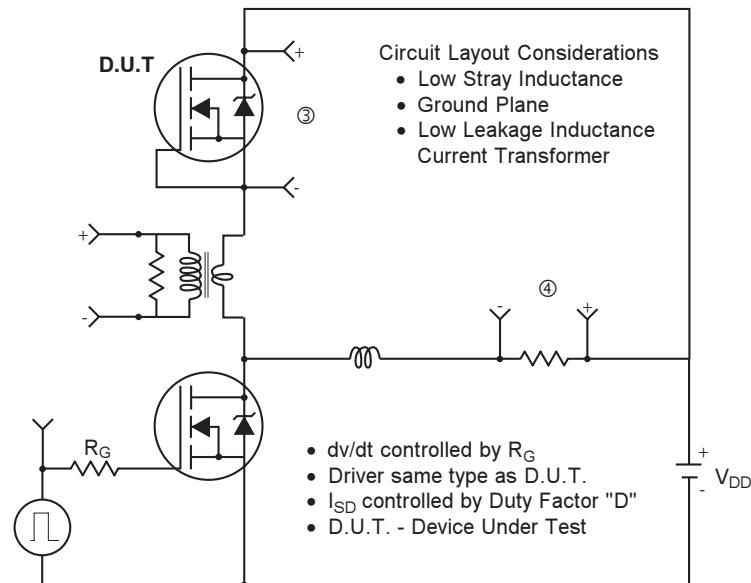
Fig 13a. Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

6

IRFR/U220NPbF

Peak Diode Recovery dv/dt Test Circuit

D.U.T

③

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

④

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

R_G

V_{DD}

① Driver Gate Drive

$D = \dfrac{P.W.}{Period}$

P.W.

Period

$V_{GS}=10V$ *

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current

di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

V_{DD}

Re-Applied Voltage

Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%

I_{SD}

* V_{GS} = 5V for Logic Level Devices
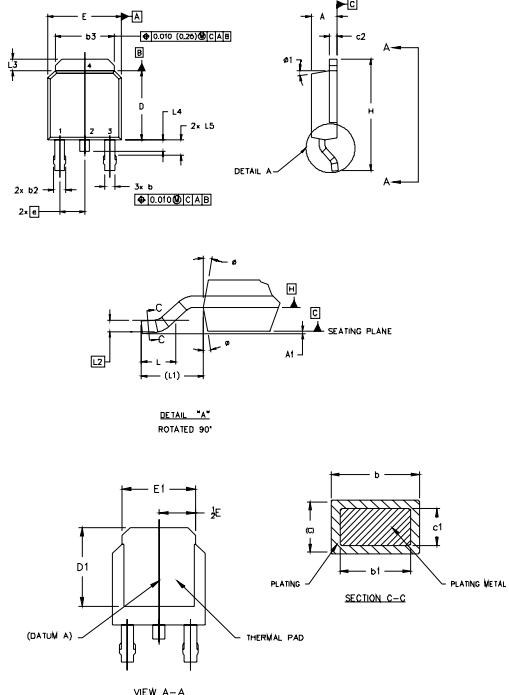
Fig 14. For N-Channel HEXFET® Power MOSFETs

D-Pak (TO-252AA) Package Outline
Dimensions are shown in millimeters (inches)

NOTES:
1.0   DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2.0   DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.0   LEAD DIMENSION UNCONTROLLED IN L5
4.0   DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.0   SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND
       .010 [0.2540 FROM THE LEAD TIP.
6.0   DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED
       .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST
       EXTREMES OF THE PLASTIC BODY.
7.0   OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

| SYMBOL | DIMENSIONS | | | | NOTES |
| | MILLIMETERS | | INCHES | | |
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.13		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	.031	5
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	5
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170		4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		108 REF		
L2	0.051 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN
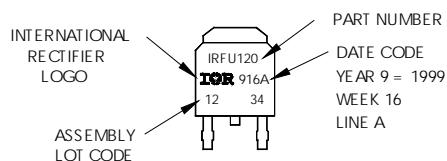
IGBTs, CoPACK
1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR
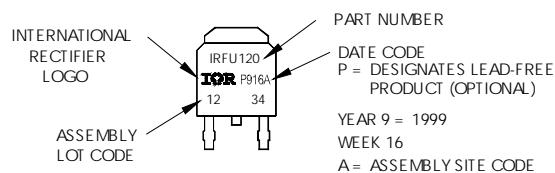
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
                  WITH ASSEMBLY
                  LOT CODE 1234
                  ASSEMBLED ON WW 16, 1999
                  IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
         indicates "Lead-Free"

INTERNATIONAL
RECTIFIER
LOGO

PART NUMBER
DATE CODE
YEAR 9 = 1999
WEEK 16
LINE A

ASSEMBLY
LOT CODE

OR

INTERNATIONAL
RECTIFIER
LOGO

PART NUMBER
DATE CODE
P = DESIGNATES LEAD-FREE
      PRODUCT (OPTIONAL)
YEAR 9 = 1999
WEEK 16
A = ASSEMBLY SITE CODE

ASSEMBLY
LOT CODE
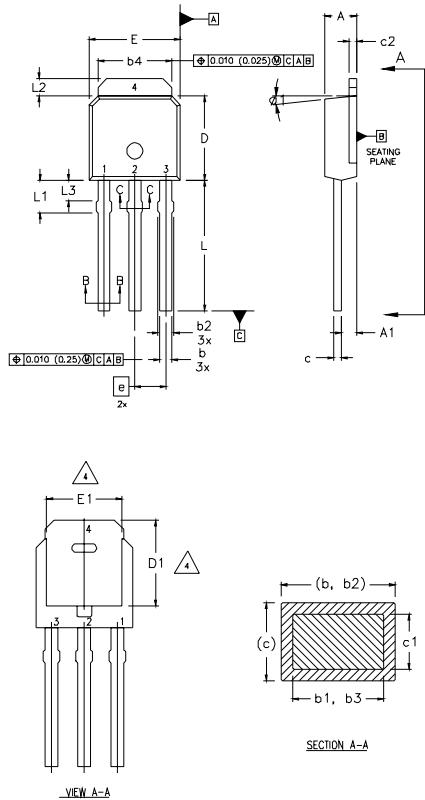
I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

NOTES:
1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M– 1994.
2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
5 LEAD DIMENSION UNCONTROLLED IN L3.
6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
7 OUTLINE CONFORMS TO JEDEC OUTLINE TO–251AA.
8 CONTROLLING DIMENSION : INCHES.
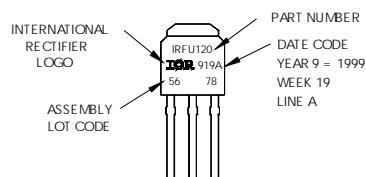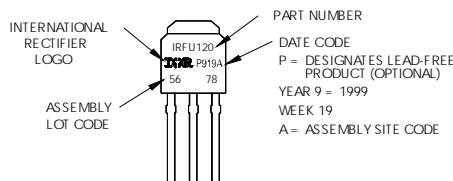
| SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	–	0.205	–	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	–	0.170	–	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0'	15'	0'	15'	

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW 19, 1999 IN THE ASSEMBLY LINE "A"

**Note:** "P" in assembly line position indicates "Lead-Free"

PART NUMBER
DATE CODE
YEAR 9 = 1999
WEEK 19
LINE A

INTERNATIONAL RECTIFIER LOGO

ASSEMBLY LOT CODE

OR

INTERNATIONAL RECTIFIER LOGO

ASSEMBLY LOT CODE

PART NUMBER
DATE CODE
P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)
YEAR 9 = 1999
WEEK 19
A = ASSEMBLY SITE CODE
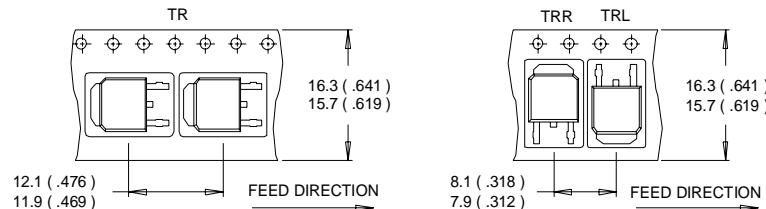
IRFR/U220NPbF

D-Pak (TO-252AA) Tape & Reel Information
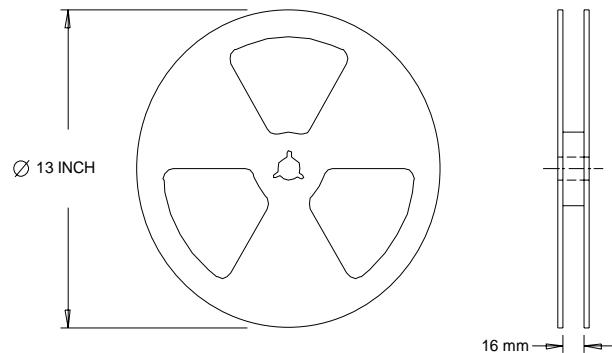
Dimensions are shown in millimeters (inches)

TR   TRR   TRL

16.3 (.641)
15.7 (.619)

16.3 (.641)
15.7 (.619)

12.1 (.476)
11.9 (.469)   FEED DIRECTION

8.1 (.318)
7.9 (.312)   FEED DIRECTION

NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

$\varnothing$ 13 INCH

16 mm

NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by
    max. junction temperature.

② Starting $T_J = 25°C$, $L = 11mH$
    $R_G = 25\Omega$, $I_{AS} = 2.9A$.

③ $I_{SD} \leq 2.9A$, di/dt $\leq 320A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
    $T_J \leq 175°C$

④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time
    as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

* When mounted on 1" square PCB (FR-4 or G-10 Material).
    For recommended footprint and soldering techniques refer to application note #AN-994.

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/

Mouser Electronics

Authorized Distributor

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