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# ANY8008B

## Low Power Programmable Oscillator

# AnyCLK

Service depends on time

### Features

- Any frequency between 1 MHz and 110 MHz accurate to 6 decimal places
- 100% pin-to-pin drop-in replacement to quartz-based XO
- Excellent total frequency stability as low as  $\pm 20$  ppm
- Operating temperature from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . For  $125^{\circ}\text{C}$  and/or  $-55^{\circ}\text{C}$  options, refer to [ANY1618](#), [ANY8918](#), [ANY8920](#)
- Low power consumption of 3.5 mA typical at 1.8V
- Standby mode for longer battery life
- Fast startup time of 5 ms
- LVC MOS/HCMOS compatible output
- Industry-standard packages: 2.0 x 1.6, 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm
- Instant samples with [Time Machine II](#) and [field programmable oscillators](#)
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free
- For AEC-Q100 oscillators, refer to [ANY8924](#) and [ANY8925](#)

### Applications

- Ideal for DSC, DVC, DVR, IP CAM, Tablets, e-Books, SSD, GPON, EPON, etc
- Ideal for high-speed serial protocols such as: USB, SATA, SAS, Firewire, 100M / 1G / 10G Ethernet, etc.



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## Electrical Specifications

**Table 1. Electrical Characteristics**

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at  $25^{\circ}\text{C}$  and nominal supply voltage.

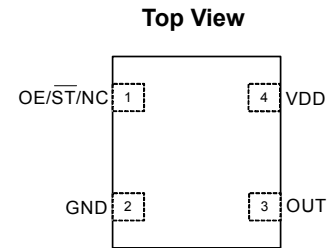
Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Frequency Range</b>						
Output Frequency Range	f	1	–	110	MHz	
<b>Frequency Stability and Aging</b>						
Frequency Stability	F_stab	-20	–	+20	ppm	Inclusive of initial tolerance at $25^{\circ}\text{C}$ , 1st year aging at $25^{\circ}\text{C}$ , and variations over operating temperature, rated power supply voltage and load.
		-25	–	+25	ppm	
		-50	–	+50	ppm	
<b>Operating Temperature Range</b>						
Operating Temperature Range	T_use	-20	–	+70	$^{\circ}\text{C}$	Extended Commercial
		-40	–	+85	$^{\circ}\text{C}$	Industrial
<b>Supply Voltage and Current Consumption</b>						
Supply Voltage	Vdd	1.62	1.8	1.98	V	Contact <a href="#">Anyclk</a> for 1.5V support
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd	–	3.8	4.5	mA	No load condition, f = 20 MHz, Vdd = 2.8V to 3.3V
		–	3.7	4.2	mA	No load condition, f = 20 MHz, Vdd = 2.5V
		–	3.5	4.1	mA	No load condition, f = 20 MHz, Vdd = 1.8V
OE Disable Current	I_OD	–	–	4.2	mA	Vdd = 2.5V to 3.3V, OE = GND, Output in high-Z state
		–	–	4.0	mA	Vdd = 1.8V, OE = GND, Output in high-Z state
Standby Current	I_std	–	2.1	4.3	$\mu\text{A}$	ST = GND, Vdd = 2.8V to 3.3V, Output is weakly pulled down
		–	1.1	2.5	$\mu\text{A}$	ST = GND, Vdd = 2.5V, Output is weakly pulled down
		–	0.2	1.3	$\mu\text{A}$	ST = GND, Vdd = 1.8V, Output is weakly pulled down
<b>LVC MOS Output Characteristics</b>						
Duty Cycle	DC	45	–	55	%	All Vdds. See Duty Cycle definition in <a href="#">Figure 3</a> and Footnote 6
Rise/Fall Time	Tr, Tf	–	1	2	ns	Vdd = 2.5V, 2.8V, 3.0V or 3.3V, 20% - 80%
		–	1.3	2.5	ns	Vdd = 1.8V, 20% - 80%
		–	–	2	ns	Vdd = 2.25V - 3.63V, 20% - 80%
Output High Voltage	VOH	90%	–	–	Vdd	IOH = -4 mA (Vdd = 3.0V or 3.3V) IOH = -3 mA (Vdd = 2.8V and Vdd = 2.5V) IOH = -2 mA (Vdd = 1.8V)
Output Low Voltage	VOL	–	–	10%	Vdd	IOL = 4 mA (Vdd = 3.0V or 3.3V) IOL = 3 mA (Vdd = 2.8V and Vdd = 2.5V) IOL = 2 mA (Vdd = 1.8V)

**Table 1. Electrical Characteristics (continued)**

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Input Characteristics</b>						
Input High Voltage	V <sub>IH</sub>	70%	–	–	V <sub>dd</sub>	Pin 1, OE or $\overline{ST}$
Input Low Voltage	V <sub>IL</sub>	–	–	30%	V <sub>dd</sub>	Pin 1, OE or $\overline{ST}$
Input Pull-up Impedance	Z <sub>in</sub>	50	87	150	k $\Omega$	Pin 1, OE logic high or logic low, or $\overline{ST}$ logic high
		2	–	–	M $\Omega$	Pin 1, $\overline{ST}$ logic low
<b>Startup and Resume Timing</b>						
Startup Time	T <sub>start</sub>	–	–	5	ms	Measured from the time V <sub>dd</sub> reaches its rated minimum value
Enable/Disable Time	T <sub>oe</sub>	–	–	130	ns	f = 110 MHz. For other frequencies, T <sub>oe</sub> = 100 ns + 3 * cycles
Resume Time	T <sub>resume</sub>	–	–	5	ms	Measured from the time ST pin crosses 50% threshold
<b>Jitter</b>						
RMS Period Jitter	T <sub>jitt</sub>	–	1.8	3	ps	f = 75 MHz, V <sub>dd</sub> = 2.5V, 2.8V, 3.0V or 3.3V
		–	1.8	3	ps	f = 75 MHz, V <sub>dd</sub> = 1.8V
Peak-to-peak Period Jitter	T <sub>pk</sub>	–	12	25	ps	f = 75 MHz, V <sub>dd</sub> = 2.5V, 2.8V, 3.0V or 3.3V
		–	14	30	ps	f = 75 MHz, V <sub>dd</sub> = 1.8V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.5	0.9	ps	f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz
		–	1.3	2	ps	f = 75 MHz, Integration bandwidth = 12 kHz to 20 MHz

**Table 2. Pin Description**

Pin	Symbol		Functionality
1	OE/ $\overline{ST}$ /NC	Output Enable	H <sup>[1]</sup> : specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby	H <sup>[1]</sup> : specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I <sub>std</sub> .
		No Connect	Any voltage between 0 and V <sub>dd</sub> or Open <sup>[1]</sup> : Specified frequency output. Pin 1 has no function.
2	GND	Power	Electrical ground
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage <sup>[2]</sup>



**Figure 1. Pin Assignments**

**Notes:**

- In OE or  $\overline{ST}$  mode, a pull-up resistor of 10 k $\Omega$  or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
- A capacitor of value 0.1  $\mu$ F or higher between V<sub>dd</sub> and GND is required.

**Table 3. Absolute Maximum Limits**

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Vdd	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Junction Temperature <sup>[3]</sup>	–	150	°C

Note:

- Exceeding this temperature for extended period of time may damage the device.

**Table 4. Thermal Consideration<sup>[4]</sup>**

Package	$\theta_{JA}$ , 4 Layer Board (°C/W)	$\theta_{JA}$ , 2 Layer Board (°C/W)	$\theta_{JC}$ , Bottom (°C/W)
7050	142	273	30
5032	97	199	24
3225	109	212	27
2520	117	222	26
2016	152	252	36

Note:

- Refer to JESD51 for  $\theta_{JA}$  and  $\theta_{JC}$  definitions, and reference layout used to determine the  $\theta_{JA}$  and  $\theta_{JC}$  values in the above table.

**Table 5. Maximum Operating Junction Temperature<sup>[5]</sup>**

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	80°C
85°C	95°C

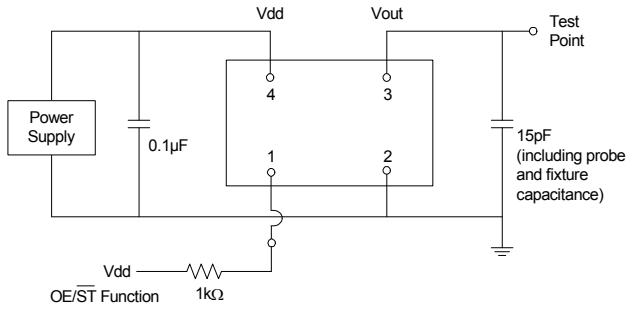
Note:

- Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

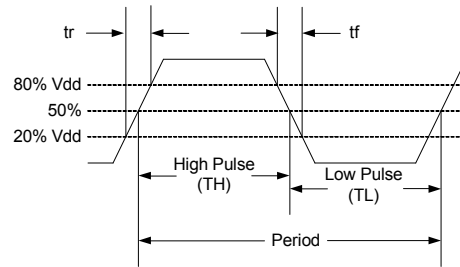
**Table 6. Environmental Compliance**

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

### Test Circuit and Waveform<sup>[6]</sup>



**Figure 2. Test Circuit**

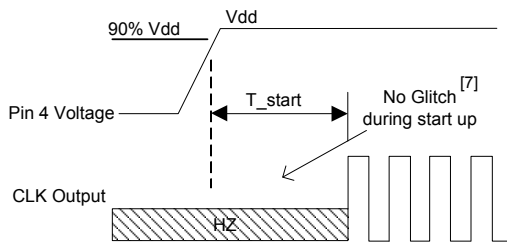


**Figure 3. Waveform**

**Note:**

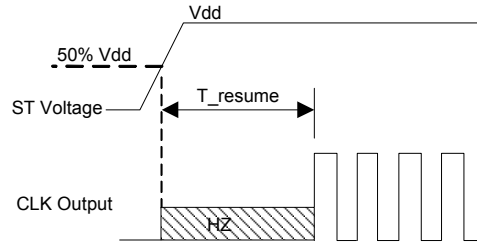
6. Duty Cycle is computed as  $Duty\ Cycle = TH/Period$ .

### Timing Diagrams



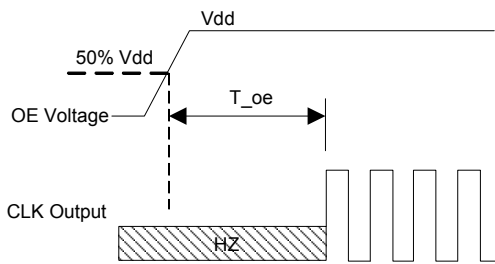
$T_{start}$ : Time to start from power-off

**Figure 4. Startup Timing (OE/ST Mode)**



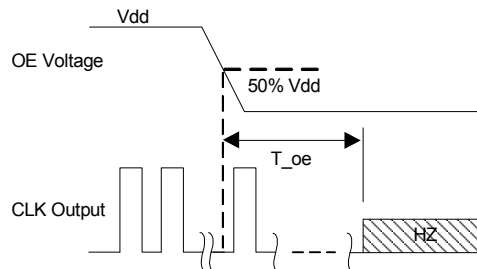
$T_{resume}$ : Time to resume from ST

**Figure 5. Standby Resume Timing (ST Mode Only)**



$T_{oe}$ : Time to re-enable the clock output

**Figure 6. OE Enable Timing (OE Mode Only)**



$T_{oe}$ : Time to put the output in High Z mode

**Figure 7. OE Disable Timing (OE Mode Only)**

**Note:**

7. ANY8008 has “no runt” pulses and “no glitch” output during startup or resume.

### Performance Plots<sup>[8]</sup>

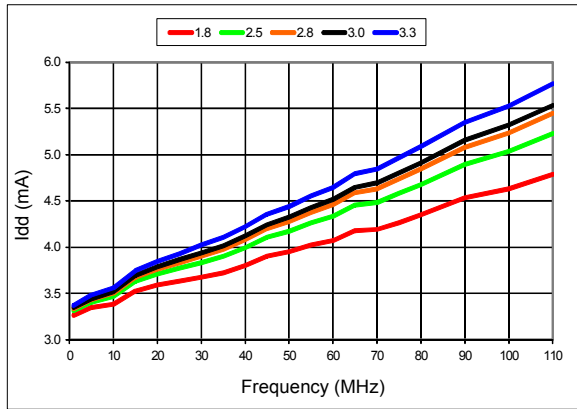


Figure 8. Idd vs Frequency

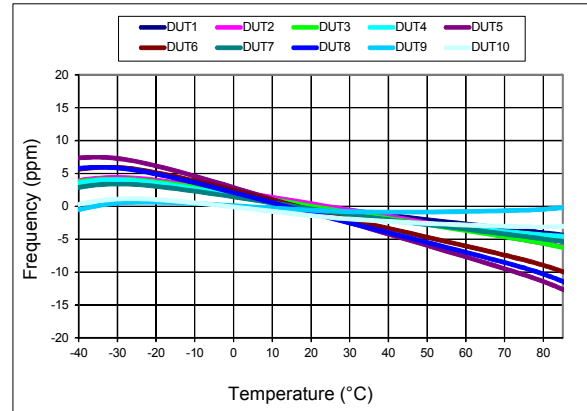


Figure 9. Frequency vs Temperature

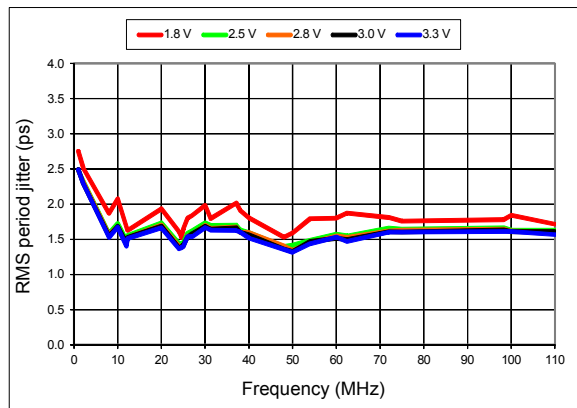


Figure 10. RMS Period Jitter vs Frequency

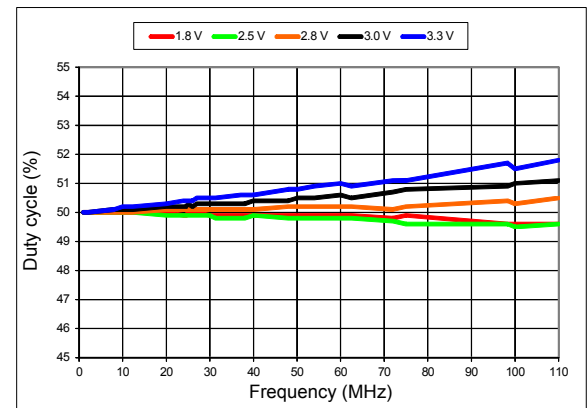


Figure 11. Duty Cycle vs Frequency

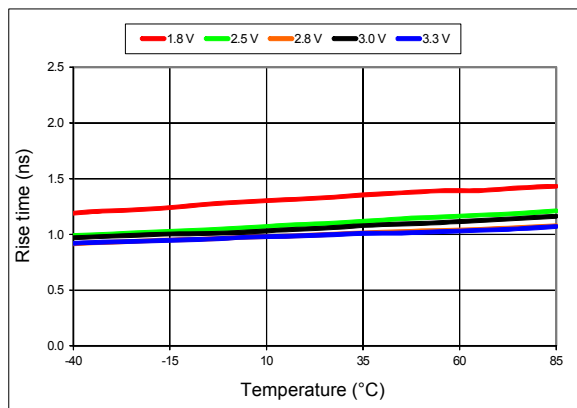


Figure 12. 20%-80% Rise Time vs Temperature

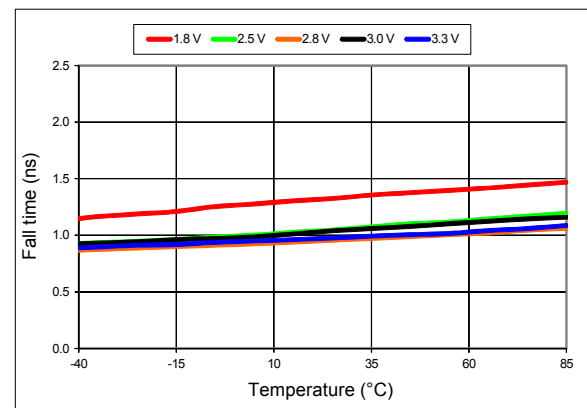


Figure 13. 20%-80% Fall Time vs Temperature

### Performance Plots<sup>[8]</sup>

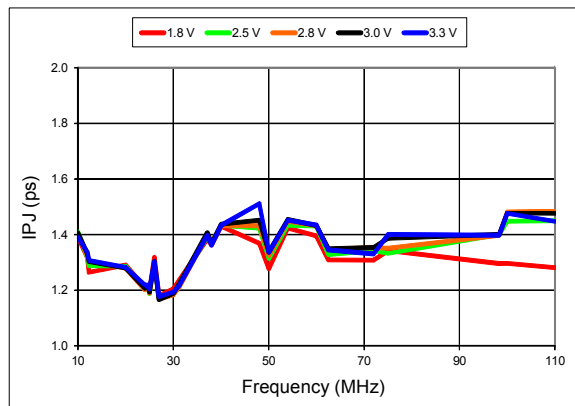


Figure 14. RMS Integrated Phase Jitter Random (12 kHz to 20 MHz) vs Frequency<sup>[9]</sup>

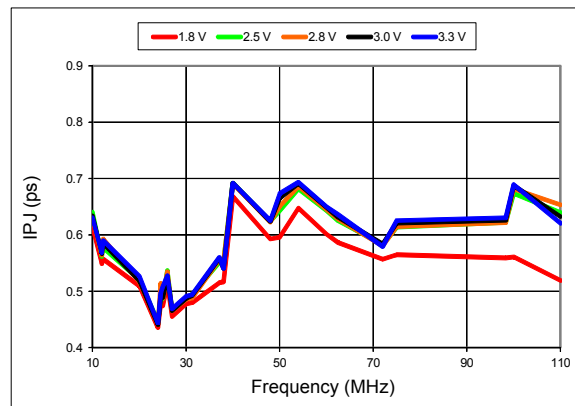


Figure 15. RMS Integrated Phase Jitter Random (900 kHz to 20 MHz) vs Frequency<sup>[9]</sup>

#### Notes:

8. All plots are measured with 15 pF load at room temperature, unless otherwise stated.

9. Phase noise plots are measured with Agilent E5052B signal source analyzer. Integration range is up to 5 MHz for carrier frequencies below 40 MHz.

### Programmable Drive Strength

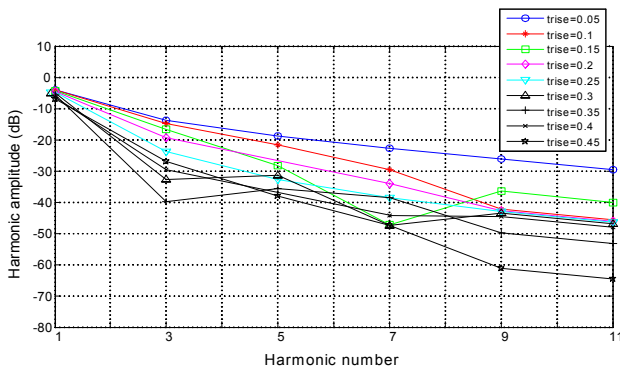
The ANY8008 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the Anyclk Application Notes

### EMI Reduction by Slowing Rise/Fall Time

Figure 16 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.



**Figure 16. Harmonic EMI reduction as a Function of Slower Rise/Fall Time**

### Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the [Rise/Fall Time Tables \(Table 7 to Table 11\)](#) to determine the proper drive strength.

### High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V ANY8008 device with default drive strength setting, the typical rise/fall time is 1 ns for 15 pF output load. The typical rise/fall time slows down to 2.6 ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.83 ns by then increasing the drive strength setting on the ANY8008.

The ANY8008 can support up to 60 pF or higher in maximum capacitive loads with drive strength settings. Refer to the [Rise/Fall Time Tables \(Table 7 to 11\)](#) to determine the proper drive strength for the desired combination of output load vs. rise/fall time. ANY8008 Drive Strength Selection

### ANY8008 Drive Strength Selection

Tables 7 through 11 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the ANY8008 nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

### Maximum Frequency Calculation

Any given rise/fall time in Table 7 through 11 dictates the maximum frequency under which the oscillator can operate with guaranteed full output swing over the entire operating temperature range. This max frequency can be calculated as the following:

$$\text{Max Frequency} = \frac{1}{5 \times \text{Trf}_{20/80}}$$

where  $\text{Trf}_{20/80}$  is the typical value for 20%-80% rise/fall time.

### Example 1

Calculate  $f_{\text{MAX}}$  for the following condition:

- Vdd = 1.8V (Table 1)
- Capacitive Load: 30 pF
- Desired Tr/f time = 3 ns (rise/fall time part number code = E)
- $f_{\text{MAX}} = 66.666660$

Part number for the above example:

ANY8008IE12-18E-66.666660



Drive strength code is inserted here. Default setting is “-”



### Rise/Fall Time (20% to 80%) vs $C_{LOAD}$ Tables

Table 7. Vdd = 1.8V Rise/Fall Times for Specific  $C_{LOAD}$

Rise/Fall Time Typ (ns)					
Drive Strength \ $C_{LOAD}$	5 pF	15 pF	30 pF	45 pF	60 pF
L	6.16	11.61	22.00	31.27	39.91
A	3.19	6.35	11.00	16.01	21.52
R	2.11	4.31	7.65	10.77	14.47
B	1.65	3.23	5.79	8.18	11.08
T	0.93	1.91	3.32	4.66	6.48
E	0.78	1.66	2.94	4.09	5.74
U	0.70	1.48	2.64	3.68	5.09
F or "-": default	0.65	1.30	2.40	3.35	4.56

Table 8. Vdd = 2.5V Rise/Fall Times for Specific  $C_{LOAD}$

Rise/Fall Time Typ (ns)					
Drive Strength \ $C_{LOAD}$	5 pF	15 pF	30 pF	45 pF	60 pF
L	4.13	8.25	12.82	21.45	27.79
A	2.11	4.27	7.64	11.20	14.49
R	1.45	2.81	5.16	7.65	9.88
B	1.09	2.20	3.88	5.86	7.57
T	0.62	1.28	2.27	3.51	4.45
E or "-": default	0.54	1.00	2.01	3.10	4.01
U	0.43	0.96	1.81	2.79	3.65
F	0.34	0.88	1.64	2.54	3.32

Table 9. Vdd = 2.8V Rise/Fall Times for Specific  $C_{LOAD}$

Rise/Fall Time Typ (ns)					
Drive Strength \ $C_{LOAD}$	5 pF	15 pF	30 pF	45 pF	60 pF
L	3.77	7.54	12.28	19.57	25.27
A	1.94	3.90	7.03	10.24	13.34
R	1.29	2.57	4.72	7.01	9.06
B	0.97	2.00	3.54	5.43	6.93
T	0.55	1.12	2.08	3.22	4.08
E or "-": default	0.44	1.00	1.83	2.82	3.67
U	0.34	0.88	1.64	2.52	3.30
F	0.29	0.81	1.48	2.29	2.99

Table 10. Vdd = 3.0V Rise/Fall Times for Specific  $C_{LOAD}$

Rise/Fall Time Typ (ns)					
Drive Strength \ $C_{LOAD}$	5 pF	15 pF	30 pF	45 pF	60 pF
L	3.60	7.21	11.97	18.74	24.30
A	1.84	3.71	6.72	9.86	12.68
R	1.22	2.46	4.54	6.76	8.62
B	0.89	1.92	3.39	5.20	6.64
T or "-": default	0.51	1.00	1.97	3.07	3.90
E	0.38	0.92	1.72	2.71	3.51
U	0.30	0.83	1.55	2.40	3.13
F	0.27	0.76	1.39	2.16	2.85

Table 11. Vdd = 3.3V Rise/Fall Times for Specific  $C_{LOAD}$

Rise/Fall Time Typ (ns)					
Drive Strength \ $C_{LOAD}$	5 pF	15 pF	30 pF	45 pF	60 pF
L	3.39	6.88	11.63	17.56	23.59
A	1.74	3.50	6.38	8.98	12.19
R	1.16	2.33	4.29	6.04	8.34
B	0.81	1.82	3.22	4.52	6.33
T or "-": default	0.46	1.00	1.86	2.60	3.84
E	0.33	0.87	1.64	2.30	3.35
U	0.28	0.79	1.46	2.05	2.93
F	0.25	0.72	1.31	1.83	2.61

### Pin 1 Configuration Options (OE, $\overline{ST}$ , or NC)

Pin 1 of the ANY8008 can be factory-programmed to support three modes: Output Enable (OE), standby ( $\overline{ST}$ ) or No Connect (NC). These modes can also be programmed with the Time Machine using field programmable devices.

#### Output Enable (OE) Mode

In the OE mode, applying logic Low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in  $<1 \mu\text{s}$ .

#### Standby ( $\overline{ST}$ ) Mode

In the  $\overline{ST}$  mode, a device enters into the standby mode when Pin 1 pulled Low. All internal circuits of the device are turned off. The current is reduced to a standby current, typically in the range of a few  $\mu\text{A}$ . When  $\overline{ST}$  is pulled High, the device goes through the “resume” process, which can take up to 5 ms.

#### No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and outputs the specified frequency regardless of the logic level on pin 1.

Table 12 below summarizes the key relevant parameters in the operation of the device in OE,  $\overline{ST}$ , or NC mode.

**Table 12. OE vs.  $\overline{ST}$  vs. NC**

	OE	$\overline{ST}$	NC
Active current 20 MHz (max, 1.8V)	4.1 mA	4.1 mA	4.1 mA
OE disable current (max, 1.8V)	4 mA	N/A	N/A
Standby current (typical 1.8V)	N/A	0.6 $\mu\text{A}$	N/A
OE enable time at 20 MHz (max)	200 ns	N/A	N/A
Resume time from standby (max, all frequency)	N/A	5 ms	N/A
Output driver in OE disable/standby mode	High Z	weak pull-down	N/A

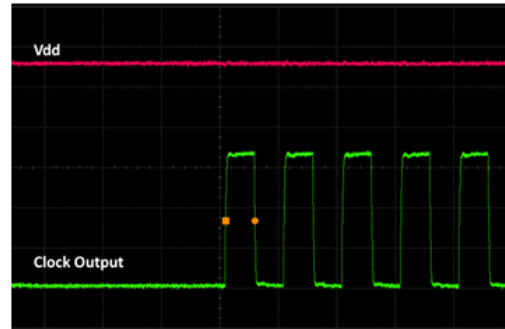
#### Output on Startup and Resume

The ANY8008 comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup or resume from the standby mode.

In addition, the ANY8008 features “no runt” pulses and “no glitch” output during startup or resume as shown in the waveform captures in Figure 17 and Figure 18.



**Figure 17. Startup Waveform vs. Vdd**



**Figure 18. Startup Waveform vs. Vdd (Zoomed-in View of Figure 17)**

### Instant Samples with Time Machine and Field Programmable Oscillators

Anyclk supports a field programmable version of the [ANY8008 low power oscillator](#) for fast prototyping and real time customization of features. The [field programmable devices](#) (FP devices) are available for all five standard ANY8008 package sizes and can be configured to one’s exact specification using the [Time Machine II](#), an USB powered MEMS oscillator programmer.

Customizable Features of the ANY8008 FP Devices Include

- Frequency between 1 MHz to 110 MHz
- Three frequency stability options,  $\pm 20$  ppm,  $\pm 25$  ppm,  $\pm 50$  ppm
- Two operating temperatures,  $-20$  to  $70^\circ\text{C}$  or  $-40$  to  $85^\circ\text{C}$
- Six supply voltage options, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V and 2.25 to 3.63V continuous
- Output drive strength
- OE, ST or NC mode

ANY8008 is typically factory-programmed per customer ordering codes for volume delivery.

### Dimensions and Patterns

Package Size – Dimensions (Unit: mm) <sup>[10]</sup>	Recommended Land Pattern (Unit: mm) <sup>[11]</sup>
<p><b>2.0 x 1.6 x 0.75 mm</b></p>	
<p><b>2.5 x 2.0 x 0.75 mm</b></p>	
<p><b>3.2 x 2.5 x 0.75 mm</b></p>	
<p><b>5.0 x 3.2 x 0.75 mm</b></p>	

### Dimensions and Patterns

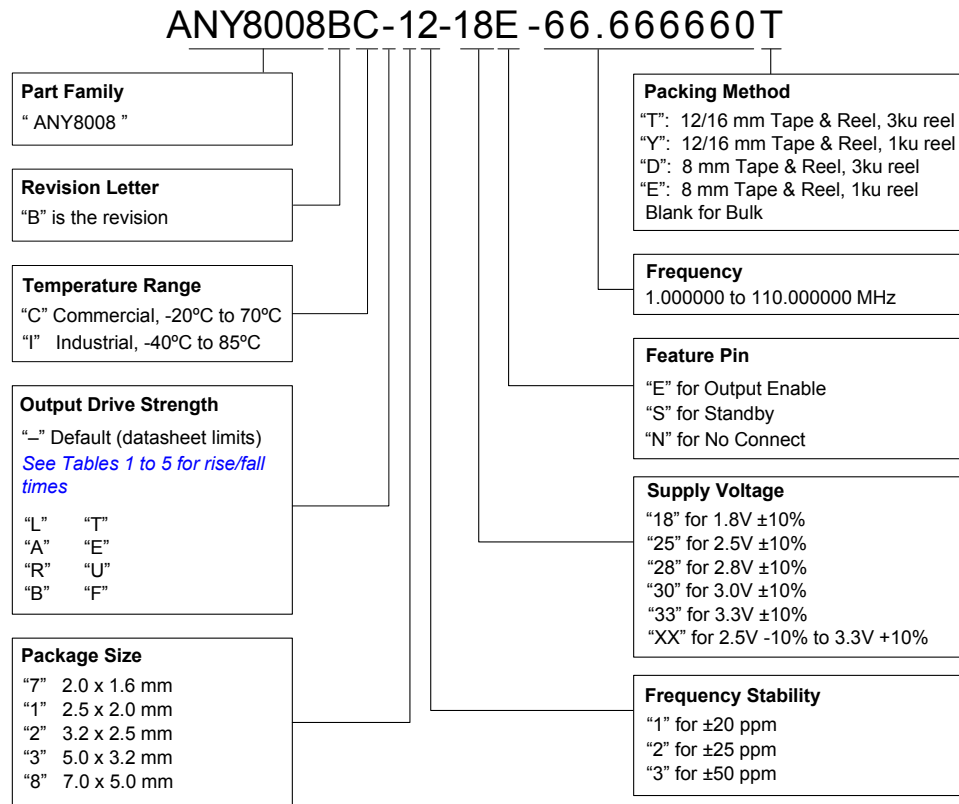
Package Size – Dimensions (Unit: mm) <sup>[10]</sup>	Recommended Land Pattern (Unit: mm) <sup>[11]</sup>
<p><b>7.0 x 5.0 x 0.90 mm</b></p>	

#### Notes:

10. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
11. A capacitor of value 0.1  $\mu$ F or higher between Vdd and GND is required.

### Ordering Information

The Part No. Guide is for reference only. To customize and build an exact part number, use the Anyclk [Part Number Generator](#).



**Table 13. Ordering Codes for Supported Tape & Reel Packing Method**

Device Size (mm x mm)	16 mm T&R (3ku)	16 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	8 mm T&R (3ku)	8 mm T&R (1ku)
2.0 x 1.6	–	–	–	–	D	E
2.5 x 2.0	–	–	–	–	D	E
3.2 x 2.5	–	–	–	–	D	E
5.0 x 3.2	–	–	T	Y	–	–
7.0 x 5.0	T	Y	–	–	–	–

**Table 14. Additional Information**

Document	Description	Inquiry
<b>Time Machine II</b>	MEMS oscillator programmer	<a href="mailto:luo@anyclk.com">Mail to luo@anyclk.com</a>
<b>Field Programmable Oscillators</b>	Devices that can be programmable in the field by Time Machine II	<a href="mailto:luo@anyclk.com">Mail to luo@anyclk.com</a>
<b>Manufacturing Notes</b>	Tape & Reel dimension, reflow profile and other manufacturing related info	<a href="mailto:luo@anyclk.com">Mail to luo@anyclk.com</a>
<b>Qualification Reports</b>	RoHS report, reliability reports, composition reports	<a href="mailto:luo@anyclk.com">Mail to luo@anyclk.com</a>
<b>Performance Reports</b>	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	<a href="mailto:luo@anyclk.com">Mail to luo@anyclk.com</a>
<b>Termination Techniques</b>	Termination design recommendations	<a href="mailto:luo@anyclk.com">Mail to luo@anyclk.com</a>
<b>Layout Techniques</b>	Layout recommendations	<a href="mailto:luo@anyclk.com">Mail to luo@anyclk.com</a>

## Revision History

**Table 15. Datasheet Version and Change Log**

Version	Release Date	Change Summary
1.0	6/10/14	First Production Release
1.01	5/07/15	<ul style="list-style-type: none"> <li>Revised the Electrical Characteristics, Timing Diagrams and Performance Plots</li> <li>Revised 2016 package diagram</li> </ul>
1.02	6/18/15	<ul style="list-style-type: none"> <li>Added 16 mm T&amp;R information to Table 13</li> <li>Revised 12 mm T&amp;R information to Table 13</li> </ul>

## Supplemental Information

The Supplemental Information section is not part of the datasheet and is for informational purposes only.

## Silicon MEMS Outperforms Quartz



## Best Reliability

Silicon is inherently more reliable than quartz. Unlike quartz suppliers, Anyclk has in-house MEMS and analog CMOS expertise, which allows Anyclk to develop the most reliable products. Figure 1 shows a comparison with quartz technology.

### Why is Anyclk Best in Class:

- Anyclk's MEMS resonators are vacuum sealed using an advanced EpiSeal™ process, which eliminates foreign particles and improves long term aging and reliability
- World-class MEMS and CMOS design expertise

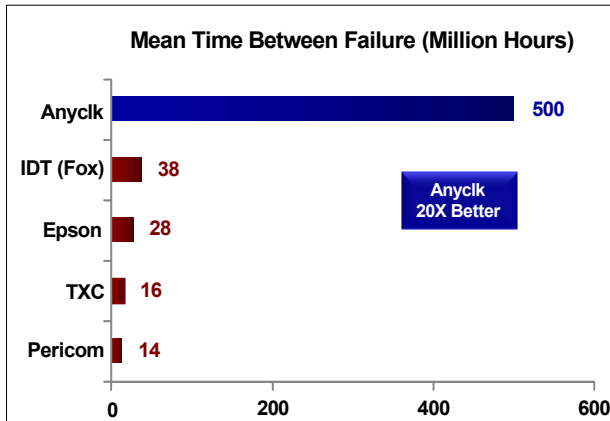


Figure 1. Reliability Comparison<sup>[1]</sup>

## Best Aging

Unlike quartz, MEMS oscillators have excellent long term aging performance which is why every new Anyclk product specifies 10-year aging. A comparison is shown in Figure 2.

### Why is Anyclk Best in Class:

- Anyclk's MEMS resonators are vacuum sealed using an advanced EpiSeal process, which eliminates foreign particles and improves long term aging and reliability
- Inherently better immunity of electrostatically driven MEMS resonator

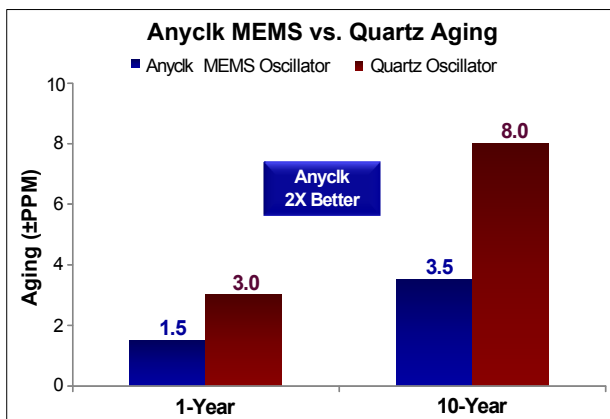


Figure 2. Aging Comparison<sup>[2]</sup>

## Best Electro Magnetic Susceptibility (EMS)

Anyclk's oscillators in plastic packages are up to 54 times more immune to external electromagnetic fields than quartz oscillators as shown in Figure 3.

### Why is Anyclk Best in Class:

- Internal differential architecture for best common mode noise rejection
- Electrostatically driven MEMS resonator is more immune to EMS

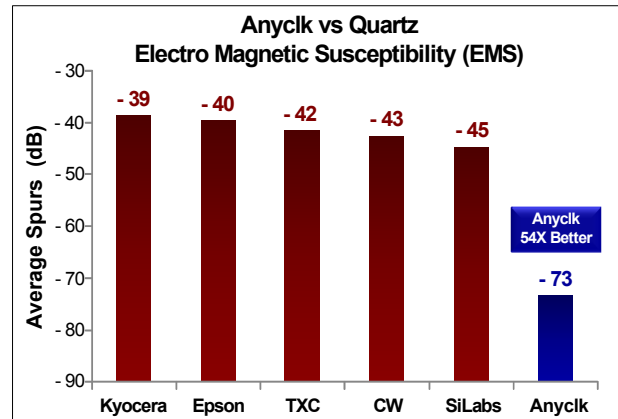


Figure 3. Electro Magnetic Susceptibility (EMS)<sup>[3]</sup>

## Best Power Supply Noise Rejection

Anyclk's MEMS oscillators are more resilient against noise on the power supply. A comparison is shown in Figure 4.

### Why is Anyclk Best in Class:

- On-chip regulators and internal differential architecture for common mode noise rejection
- Best analog CMOS design expertise

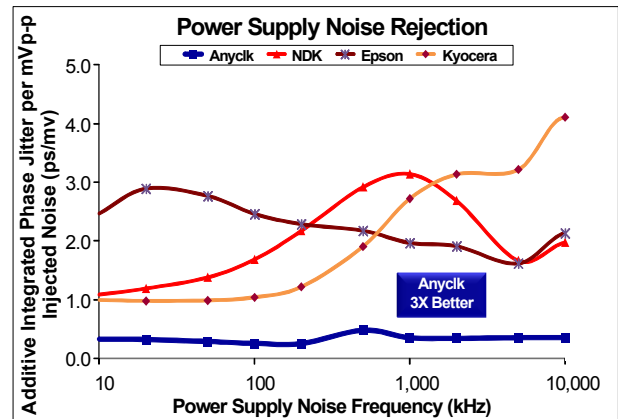


Figure 4. Power Supply Noise Rejection<sup>[4]</sup>

## Best Vibration Robustness

High-vibration environments are all around us. All electronics, from handheld devices to enterprise servers and storage systems are subject to vibration. Figure 5 shows a comparison of vibration robustness.

### Why is Anyclk Best in Class:

- The moving mass of Anyclk's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

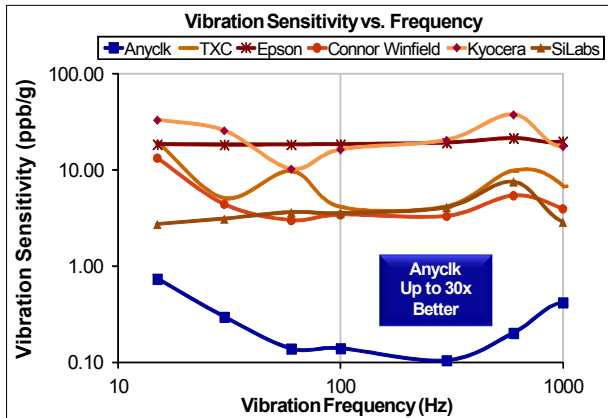


Figure 5. Vibration Robustness<sup>[5]</sup>

## Best Shock Robustness

Anyclk's oscillators can withstand at least 50,000 g shock. They all maintain their electrical performance in operation during shock events. A comparison with quartz devices is shown in Figure 6.

### Why is Anyclk Best in Class:

- The moving mass of Anyclk's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

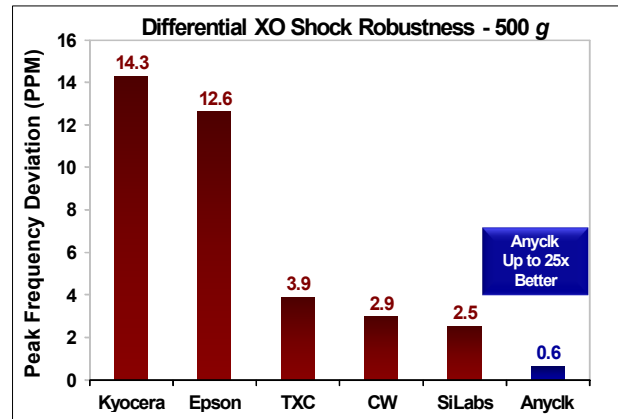


Figure 6. Shock Robustness<sup>[6]</sup>

### Notes:

1. Data Source: Reliability documents of named companies.
2. Data source: Anyclk and quartz oscillator devices datasheets.
3. Test conditions for Electro Magnetic Susceptibility (EMS):
  - According to IEC EN61000-4.3 (Electromagnetic compatibility standard)
  - Field strength: 3V/m
  - Radiated signal modulation: AM 1 kHz at 80% depth
  - Carrier frequency scan: 80 MHz – 1 GHz in 1% steps
  - Antenna polarization: Vertical
  - DUT position: Center aligned to antenna

**Devices used in this test:**

Anyclk, ANY9120AC-1D2-33E156.250000 - MEMS based - 156.25 MHz  
 Epson, EG-2102CA 156.2500M-PHPAL3 - SAW based - 156.25 MHz  
 TXC, BB-156.250MBE-T - 3rd Overtone quartz based - 156.25 MHz  
 Kyocera, KC7050T156.250P30E00 - SAW based - 156.25 MHz  
 Connor Winfield (CW), P123-156.25M - 3rd overtone quartz based - 156.25 MHz  
 SiLabs, Si590AB-BDG - 3rd overtone quartz based - 156.25 MHz
4. 50 mV pk-pk Sinusoidal voltage.
 

**Devices used in this test:**

Anyclk, ANY8208AI-33-33E-25.000000, MEMS based - 25 MHz  
 NDK, NZ2523SB-25.6M - quartz based - 25.6 MHz  
 Kyocera, KC2016B25MOC1GE00 - quartz based - 25 MHz  
 Epson, SG-310SCF-25M0-MB3 - quartz based - 25 MHz
5. **Devices used in this test:** same as EMS test stated in Note 3.
6. Test conditions for shock test:
  - MIL-STD-883F Method 2002
  - Condition A: half sine wave shock pulse, 500-g, 1ms
  - Continuous frequency measurement in 100 μs gate time for 10 seconds

**Devices used in this test:** same as EMS test stated in Note 3
7. Additional data, including setup and detailed results, is available upon request to qualified customers. Please contact [luo@anyclk.com](mailto:luo@anyclk.com)

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