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Vishay Siliconix

SiSS27DN

HALOGEN

FREE



PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A)	Q _g (TYP.)			
	0.0056 at V _{GS} = -10 V	-50 ^e				
-30	0.0070 at V_{GS} = -6 V	-50 ^e	45 nC			
	0.0090 at V_{GS} = -4.5 V	-50 ^e				

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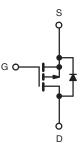


FEATURES

- TrenchFET[®] Power MOSFET
- Low thermal resistance PowerPAK[®] package with small size and low 0.75 mm profile
- 100 % R_q and UIS tested
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Notebook computers and mobile computing
 - Adaptor switch
 - Load switch
 - DC/DC converter
 - Power management



Ordering Information:

SiSS27DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

MOSFET

PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V _{DS}	-30		
Gate-Source Voltage		V _{GS}	± 20		
	T _C = 25 °C		-50 ^e		
Continuous Drain Current (T. 150 °C)	T _C = 70 °C		-50 ^e		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	-23 ^{a,b}		
	T _A = 70 °C		-18.5 ^{a,b}	•	
Pulsed Drain Current (t = 100 µs)		I _{DM}	-200	Α	
Continuous Source-Drain Diode Current	T _C = 25 °C		-47.5		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	-4 ^{a,b}		
Avalanche Current		I _{AS}	-25		
Single-Pulse Avalanche Energy L = 0.1 mH		E _{AS}	31	mJ	
	T _C = 25 °C		57		
Maximum Davies Dissis stics	T _C = 70 °C		36	14/	
Maximum Power Dissipation	T _A = 25 °C	P _D	4.8 ^{a,b}		
	T _A = 70 °C		3 a,b		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-50 to 150		
Soldering Recommendations (Peak Temperature) ^{c,d}			260		

Notes

a. Surface mounted on 1" x 1" FR4 board.

b. t = 10 s.

- c. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

e. Package limited.

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Vishay Siliconix

THERMAL RESISTANCE RATIN	GS				
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient a,b	t ≤ 10 s	R _{thJA}	21	26	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.7	2.2	0/10

Notes

a. Surface mounted on 1" x 1" FR4 board.

b. Maximum under steady state conditions is 63 °C/W.

SPECIFICATIONS ($T_J = 25 \text{ °C}$, PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static	OTHEOL				III/J/	UNIT	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	-30	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$		-	-22	_		
		I _D = -250 μA	-	5.7		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			÷	-	V	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-1	-	-2.2	-	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	-1	μA	
		$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$	-	-	-10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 V, V_{GS} = -10 V$	-20	-	-	A	
		$V_{GS} = -10 \text{ V}, \text{ I}_{D} = -15 \text{ A}$	-	0.0046	0.0056	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = -6 V, I_D = -10 A$	-	0.0058	0.0070		
					0.0090		
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$		-	S				
					-	pF	
	C _{oss}	V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz	-		-		
Reverse Transfer Capacitance	C _{rss}		-		-		
Total Gate Charge	Qg	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -20 \text{ A}$	-	-	140	nC	
.			-	-	70		
Gate-Source Charge	Q _{gs}	U		15	-		
Gate-Drain Charge	Q _{gd}		-	16	-		
Gate Resistance	Rg	f = 1 MHz	0.6	3	6	Ω	
Turn-On Delay Time	t _{d(on)}		-	60	120		
Rise Time	t _r	$V_{DD} = -15 \text{ V}, \text{ R}_{L} = 1.5 \Omega$	-	45	90		
Turn-Off DelayTime	t _{d(off)}	$\text{I}_\text{D}\cong$ -10 A, V_GEN = -4.5 V, R_g = 1 Ω	1	50	100		
Fall Time	t _f		1	20	40	- ns	
Turn-On Delay Time	t _{d(on)}		-	16	30		
Rise Time	t _r	$V_{DD} = -15 \text{ V}, \text{ R}_{L} = 1.5 \Omega$	-	5	10		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong -10$ Å, $V_{GEN} = -10$ V, $R_g = 1 \Omega$		65	130		
Fall Time	t _f		-	10	20	1	
Drain-Source Body Diode Characterist	tics	·					
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	-50 ^c	٨	
Pulse Diode Forward Current ^d	I _{SM}		-	-	-200	A	
Body Diode Voltage	V _{SD}	I _F = -10 A	-	-0.8	-1.2	V	
Body Diode Reverse Recovery Time	t _{rr}		-	30	60	ns	
Body Diode Reverse Recovery Charge	Q _{rr}		-	21	40	nC	
Reverse Recovery Fall Time	ta	I _F = -10 A, dl/dt = 100 A/μs, T _J = 25 °C	-	16	-	1	
Reverse Recovery Rise Time	t _b	1	-	14	-	ns	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

c. Package limited.

d. t = 100 µs.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

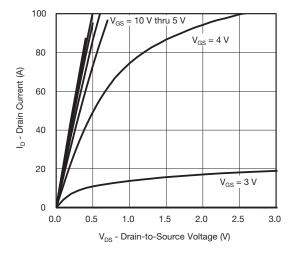
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SiSS27DN

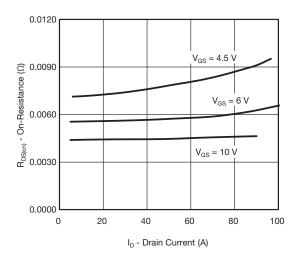


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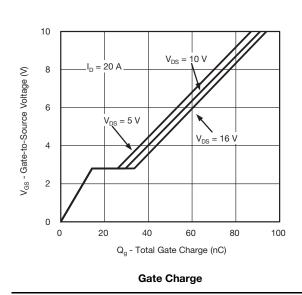
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

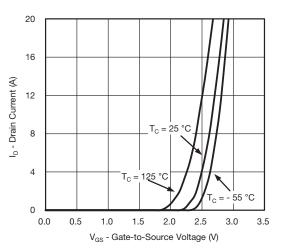


Output Characteristics

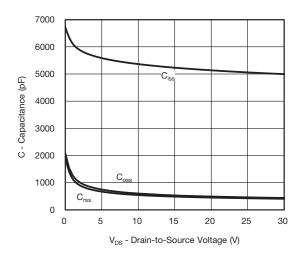


On-Resistance vs. Drain Current and Gate Voltage

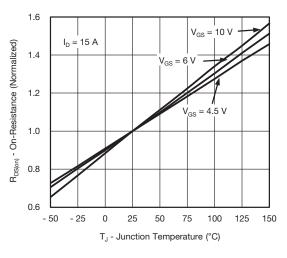




Transfer Characteristics







On-Resistance vs. Junction Temperature

S13-1161-Rev. A, 13-May-13

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Document Number: 62847

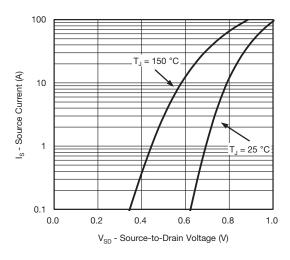
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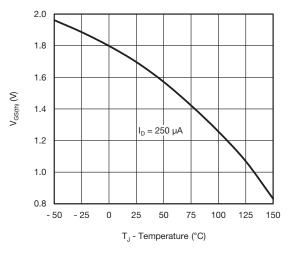


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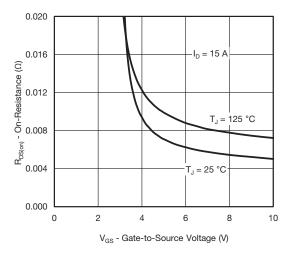
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



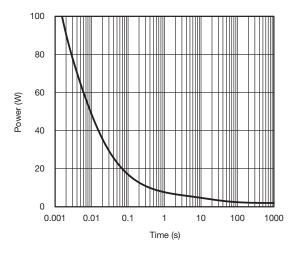
Source-Drain Diode Forward Voltage



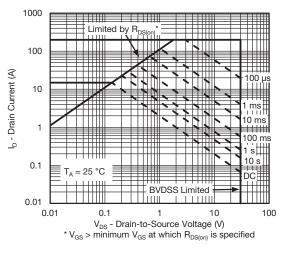




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

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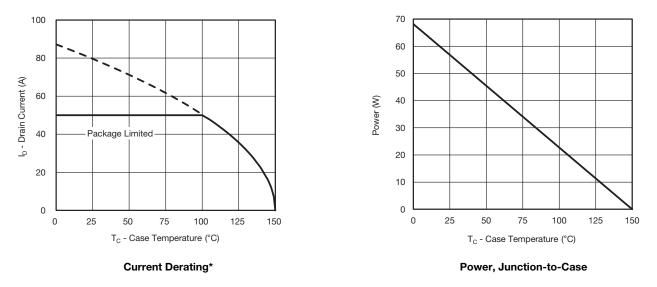
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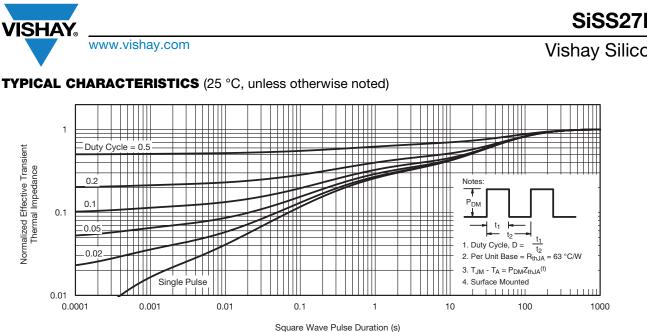
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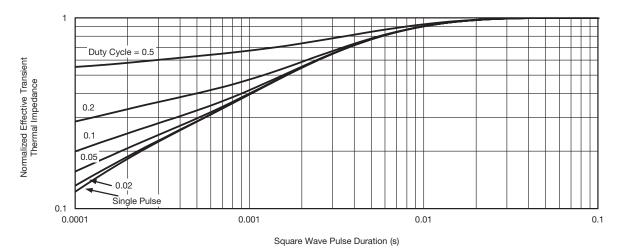
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



* The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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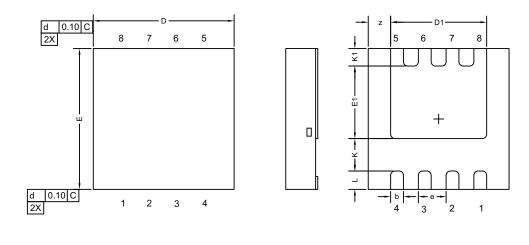
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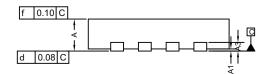
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Case Outline for PowerPAK[®] 1212-8S





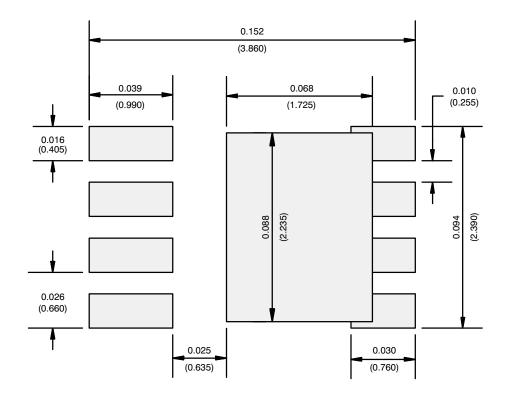
DIM.		MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
А	0.67	0.75	0.83	0.027	0.030	0.033		
A1	0	-	0.05	0	-	0.002		
A3		0.20 REF			0.008 REF			
b		0.30 BSC			0.012 BSC			
D		3.30 BSC			0.130 BSC			
D1	2.15	2.25	2.35	0.084	0.088	0.092		
E		3.30 BSC		0.130 BSC				
E1	1.60	1.70	1.80	0.063	0.067	0.071		
е		0.65 BSC		0.026 BSC				
К		0.76 TYP		0.030 TYP				
K1		0.41 TYP		0.016 TYP				
L		0.43 BSC		0.017 BSC				
Z		0.525 TYP		0.021 TYP				

Note

• Millimeters will govern.



RECOMMENDED MINIMUM PADS FOR PowerPAK[®] 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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