# 阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有"数据手册"字样。

# Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets".

# International **IQR** Rectifier
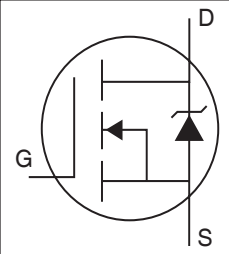
# IRFB3077PbF

HEXFET® Power MOSFET

## Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

## Benefits
- Worldwide Best $R_{DS(on)}$ in TO-220
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability

| | |
|---|---|
| $V_{DSS}$ | **75V** |
| $R_{DS(on)}$ **typ.** | **2.8m$\Omega$** |
| **max.** | **3.3m$\Omega$** |
| $I_D$ **(Silicon Limited)** | **210A** ① |
| $I_D$ **(Package Limited)** | **120A** |

TO-220AB
IRFB3077PbF
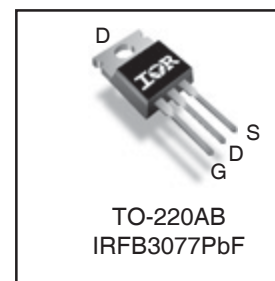
| G | D | S |
|---|---|---|
| Gate | Drain | Source |

## Absolute Maximum Ratings

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | 210① | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | 150① | |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Wire Bond Limited) | 120 | |
| $I_{DM}$ | Pulsed Drain Current ② | 850 | |
| $P_D$ @$T_C$ = 25°C | Maximum Power Dissipation | 370 | W |
| | Linear Derating Factor | 2.5 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| dV/dt | Peak Diode Recovery ④ | 2.5 | V/ns |
| $T_J$ | Operating Junction and | -55 to + 175 | °C |
| $T_{STG}$ | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds (1.6mm from case) | 300 | |
| | Mounting torque, 6-32 or M3 screw | 10lb·in (1.1N·m) | |

## Avalanche Characteristics

| | | | |
|---|---|---|---|
| $E_{AS \text{ (Thermally limited)}}$ | Single Pulse Avalanche Energy ③ | 200 | mJ |
| $I_{AR}$ | Avalanche Current ② | See Fig. 14, 15, 22a, 22b, | A |
| $E_{AR}$ | Repetitive Avalanche Energy ⑤ | | mJ |

## Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case ⑨ | —— | 0.402 | |
| $R_{\theta CS}$ | Case-to-Sink, Flat Greased Surface | 0.50 | —— | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient ⑧ ⑨ | —— | 62 | |
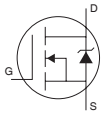
## Static @ $T_J$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 75 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | 0.091 | —— | V/°C | Reference to 25°C, $I_D$ = 5mA② |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | 2.8 | 3.3 | mΩ | $V_{GS}$ = 10V, $I_D$ = 75A ⑤ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | —— | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | —— | —— | 20 | µA | $V_{DS}$ = 75V, $V_{GS}$ = 0V |
|  |  | —— | —— | 250 |  | $V_{DS}$ = 75V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | —— | —— | 100 | nA | $V_{GS}$ = 20V |
|  | Gate-to-Source Reverse Leakage | —— | —— | -100 |  | $V_{GS}$ = -20V |
| $R_G$ | Gate Input Resistance | —— | 1.2 | —— | Ω | f = 1MHz, open drain |

## Dynamic @ $T_J$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| gfs | Forward Transconductance | 160 | —— | —— | S | $V_{DS}$ = 50V, $I_D$ = 75A |
| $Q_g$ | Total Gate Charge | —— | 160 | 220 | nC | $I_D$ = 75A |
| $Q_{gs}$ | Gate-to-Source Charge | —— | 37 | —— |  | $V_{DS}$ = 38V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | —— | 42 | —— |  | $V_{GS}$ = 10V ⑤ |
| $t_{d(on)}$ | Turn-On Delay Time | —— | 25 | —— | ns | $V_{DD}$ = 38V |
| $t_r$ | Rise Time | —— | 87 | —— |  | $I_D$ = 75A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | 69 | —— |  | $R_G$ = 2.1Ω |
| $t_f$ | Fall Time | —— | 95 | —— |  | $V_{GS}$ = 10V ⑤ |
| $C_{iss}$ | Input Capacitance | —— | 9400 | —— | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 820 | —— |  | $V_{DS}$ = 50V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 350 | —— |  | $f$ = 1.0MHz |
| $C_{oss}$ eff. (ER) | Effective Output Capacitance (Energy Related)⑦ | —— | 1090 | —— |  | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 60V ⑧, See Fig.11 |
| $C_{oss}$ eff. (TR) | Effective Output Capacitance (Time Related)⑥ | —— | 1260 | —— |  | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 60V ⑥, See Fig. 5 |

## Diode Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | —— | —— | 210① | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ②⑦ | —— | —— | 850 |  |  |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | 1.3 | V | $T_J$ = 25°C, $I_S$ = 75A, $V_{GS}$ = 0V ⑤ |
| $t_{rr}$ | Reverse Recovery Time | —— | 42 | 63 | ns | $T_J$ = 25°C $\quad V_R$ = 64V, |
|  |  | —— | 50 | 75 |  | $T_J$ = 125°C $\quad I_F$ = 75A |
| $Q_{rr}$ | Reverse Recovery Charge | —— | 59 | 89 | nC | $T_J$ = 25°C $\quad$ di/dt = 100A/µs ⑤ |
|  |  | —— | 86 | 130 |  | $T_J$ = 125°C |
| $I_{RRM}$ | Reverse Recovery Current | —— | 2.5 | —— | A | $T_J$ = 25°C |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) |  |  |  |  |

**Notes:**

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 0.028mH
$R_G$ = 25Ω, $I_{AS}$ = 120A, $V_{GS}$ =10V. Part not recommended for use above this value.

④ $I_{SD}$ ≤ 75A, di/dt ≤ 400A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C.

⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑥ $C_{oss}$ eff. (TR) is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑦ $C_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑨ $R_\theta$ is measured at $T_J$ approximately 90°C
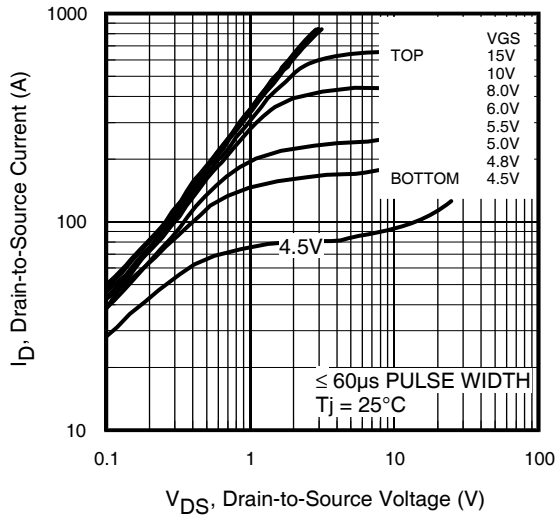
International **IGR** Rectifier



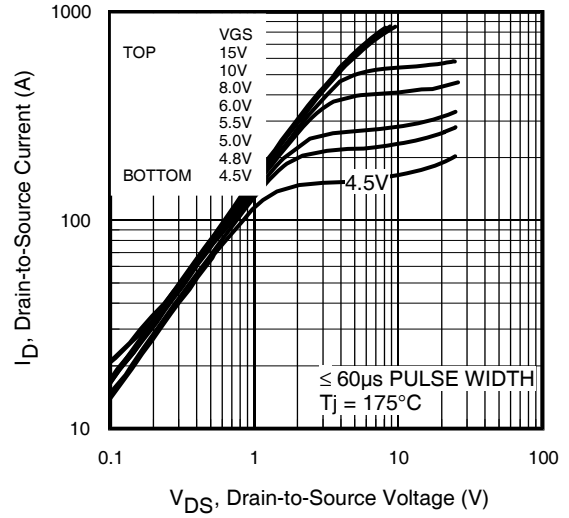**Fig 1.** Typical Output Characteristics



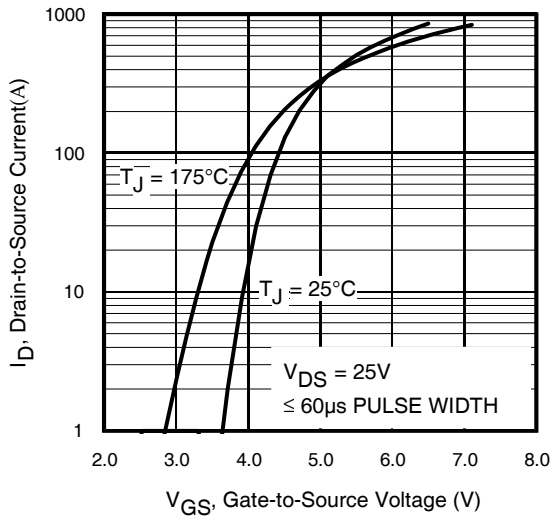**Fig 2.** Typical Output Characteristics


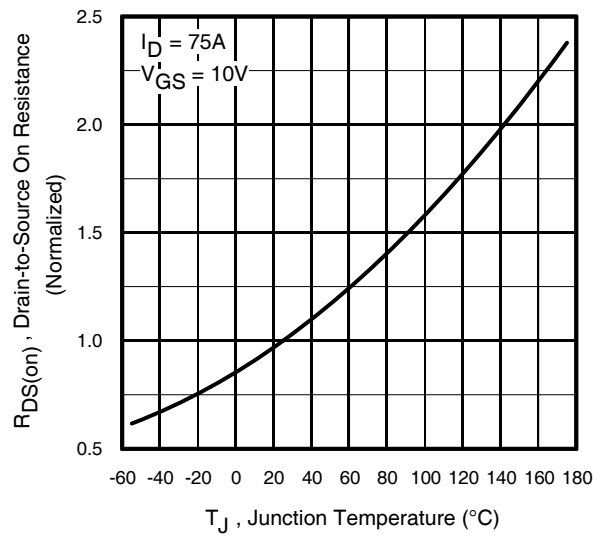
**Fig 3.** Typical Transfer Characteristics



**Fig 4.** Normalized On-Resistance vs. Temperature



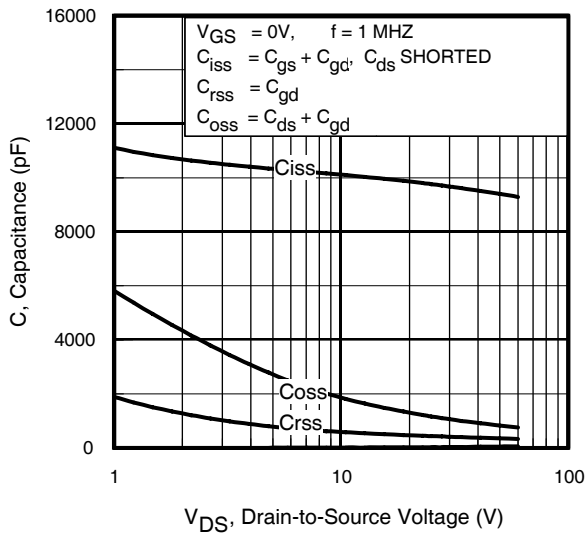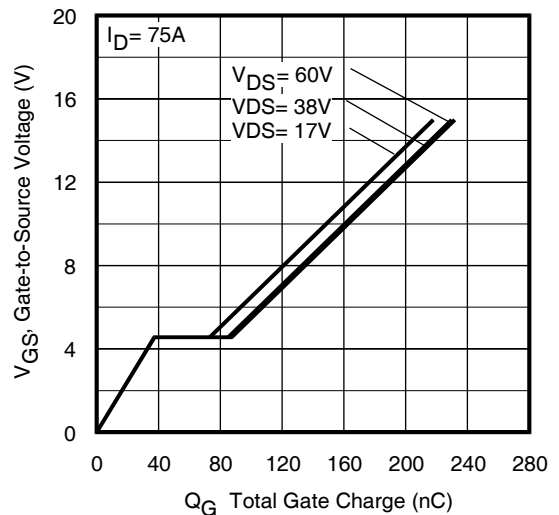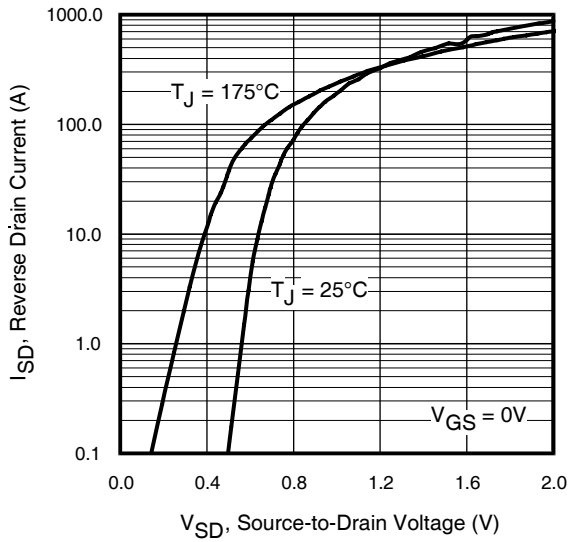**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage
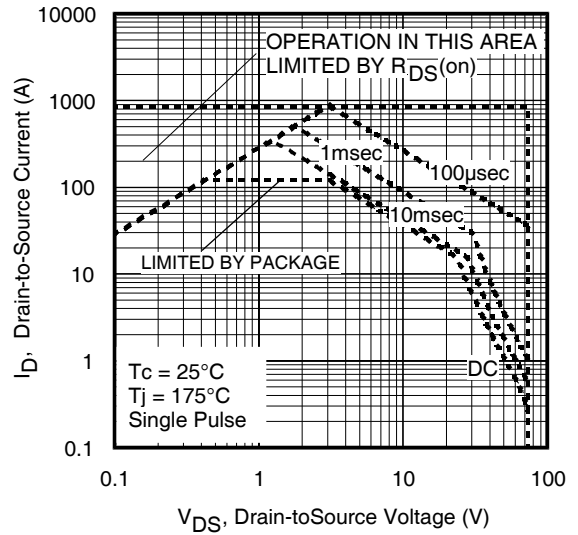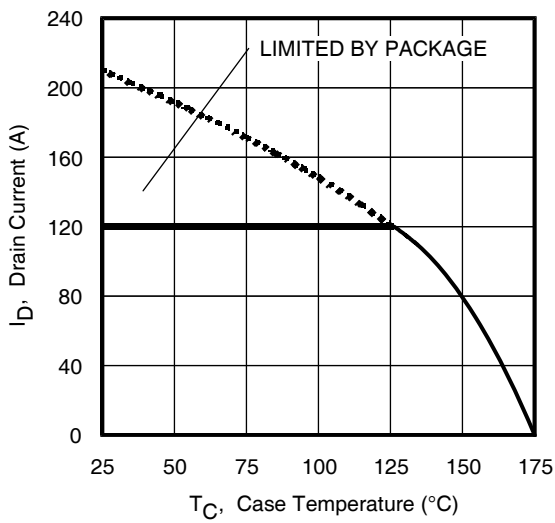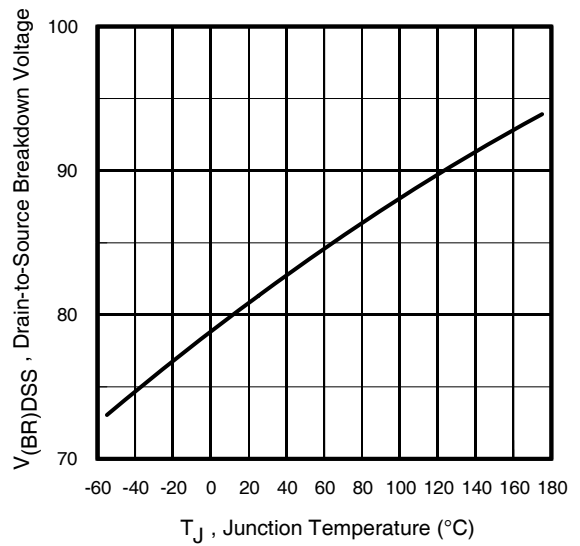


**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

**Fig 7.** Typical Source-Drain Diode
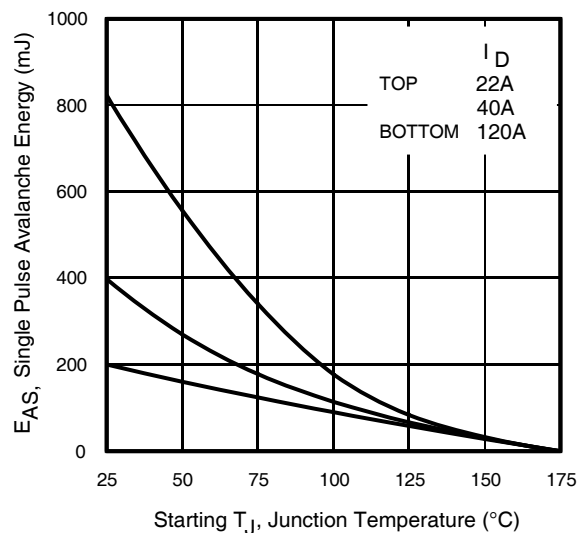Forward Voltage



**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current vs.
Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage
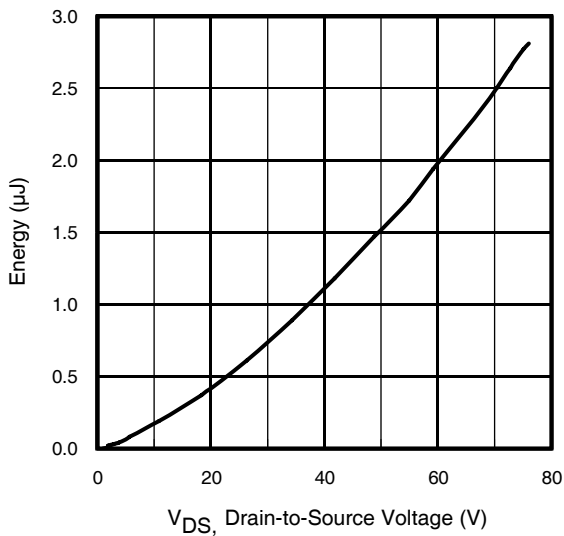


**Fig 11.** Typical $C_{OSS}$ Stored Energy



**Fig 12.** Maximum Avalanche Energy Vs. DrainCurrent
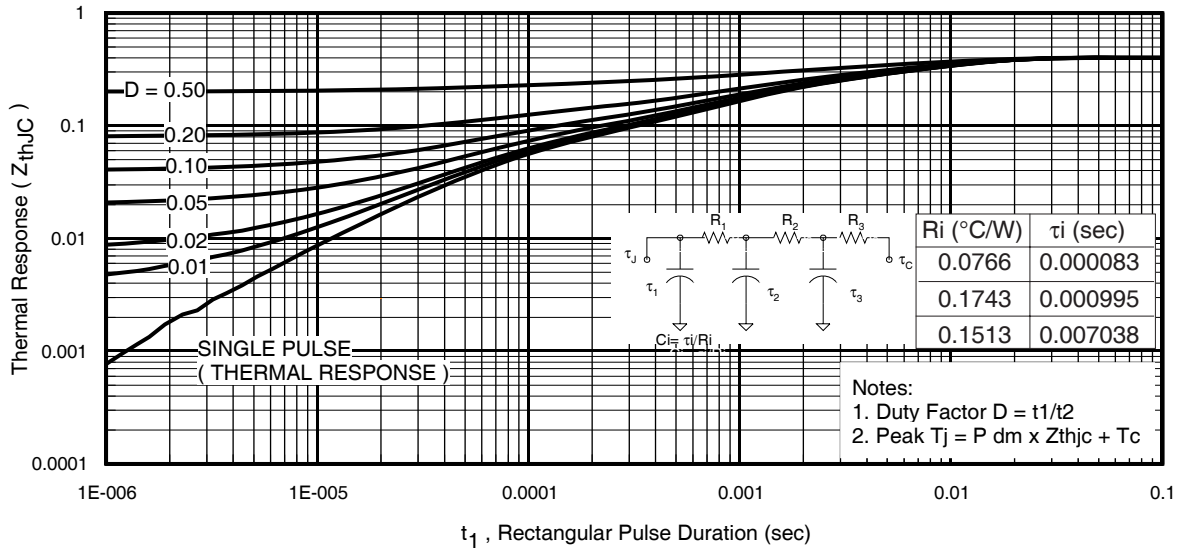
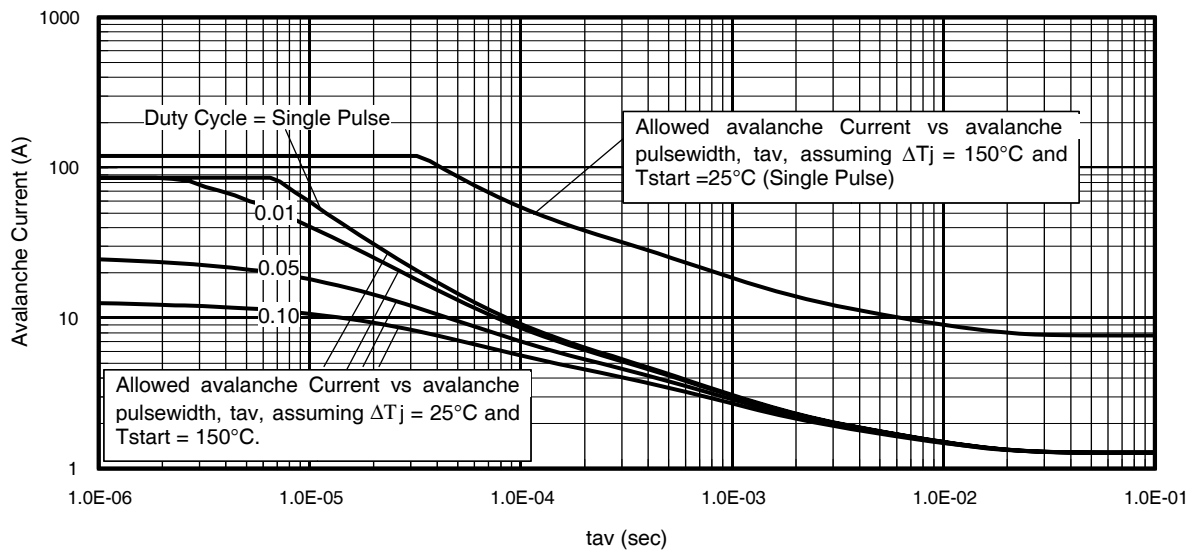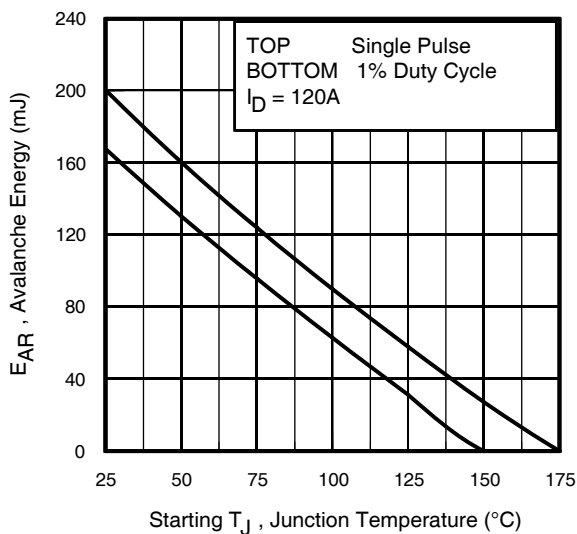**Fig 13.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Fig 14.** Typical Avalanche Current vs.Pulsewidth



**Fig 15.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 14, 15:**
**(For further info, see AN-1005 at www.irf.com)**
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as $T_{jmax}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 14, 15).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}$(D, $t_{av}$) = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T/\ Z_{thJC}$$
$$I_{av} = 2\Delta T/\ [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$
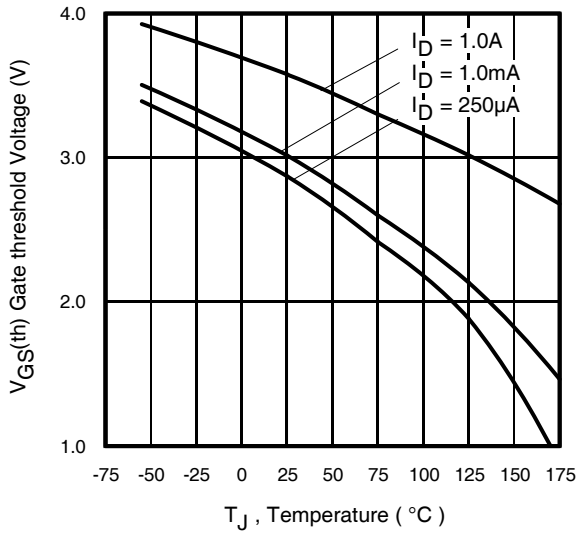
International **IØR** Rectifier



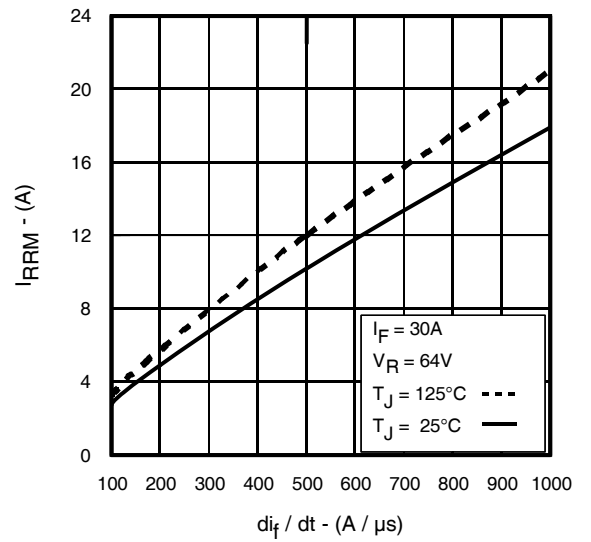**Fig 16.** Threshold Voltage Vs. Temperature



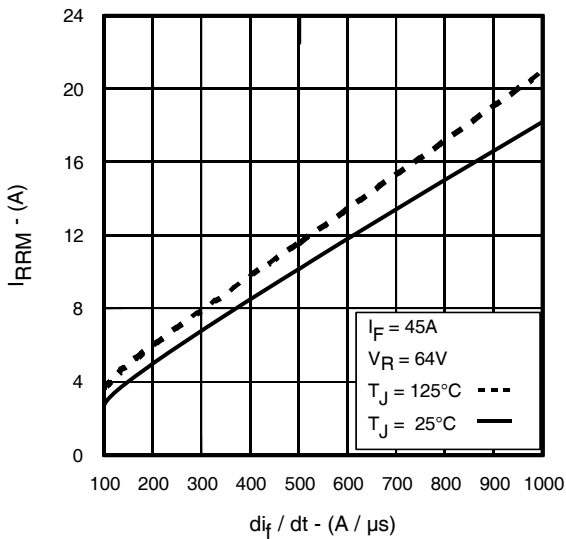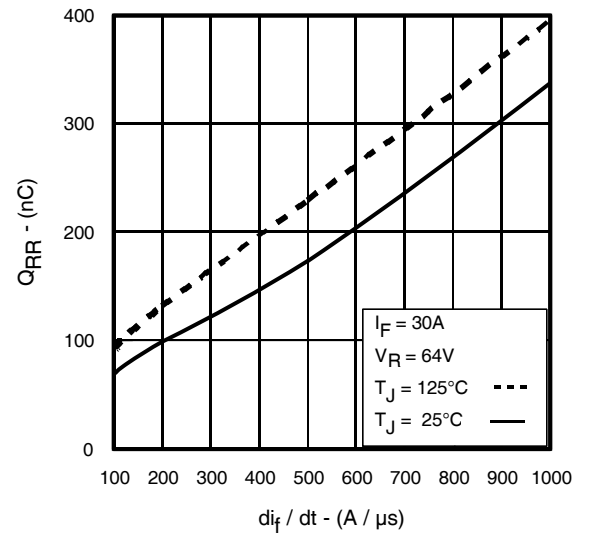**Fig. 17** - Typical Recovery Current vs. di$_f$/dt



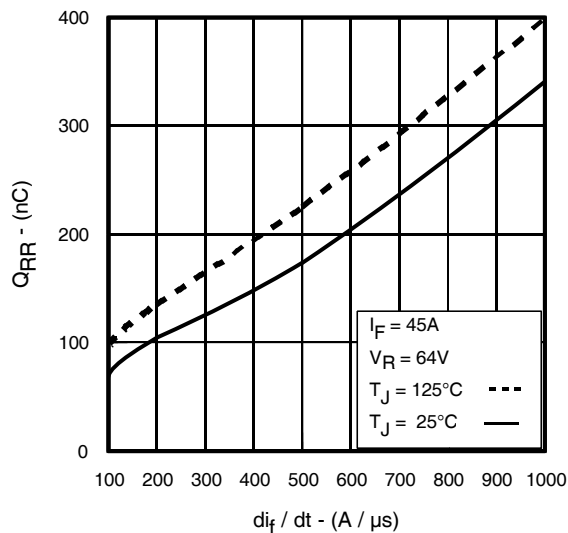**Fig. 18** - Typical Recovery Current vs. di$_f$/dt
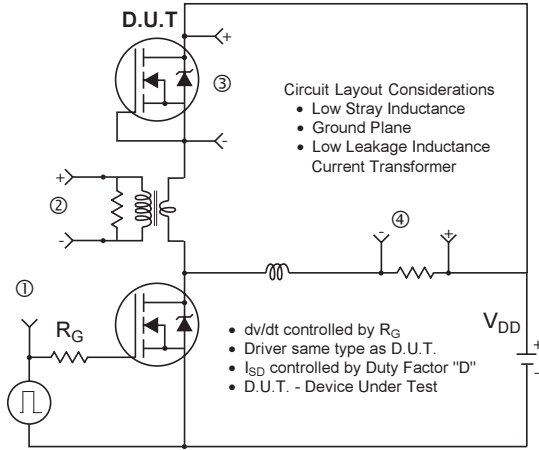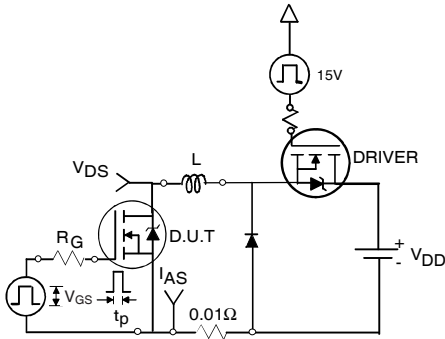


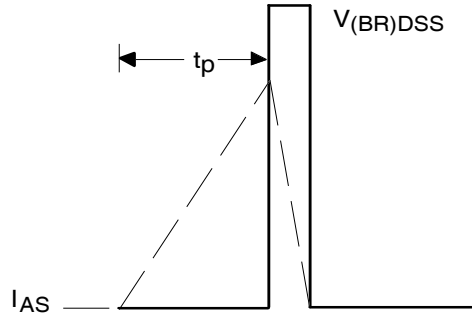**Fig. 19** - Typical Stored Charge vs. di$_f$/dt

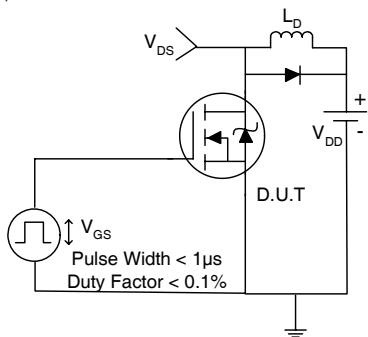

**Fig. 20** - Typical Stored Charge vs. di$_f$/dt
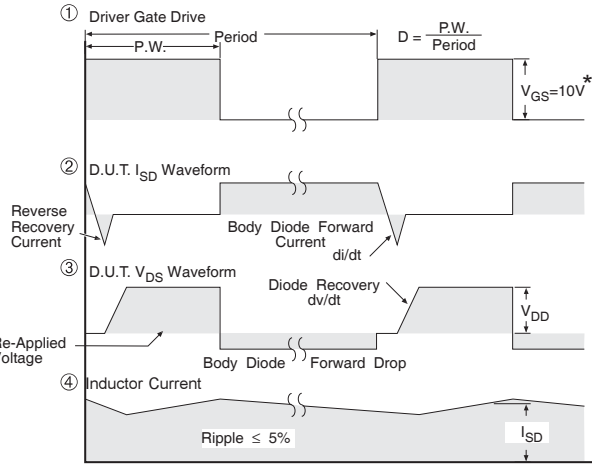
**Fig 21.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs
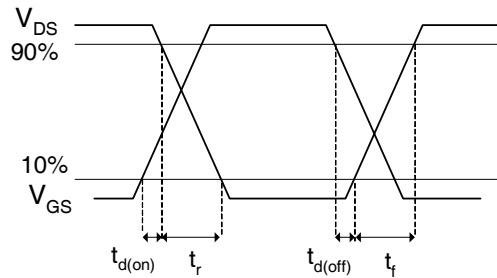


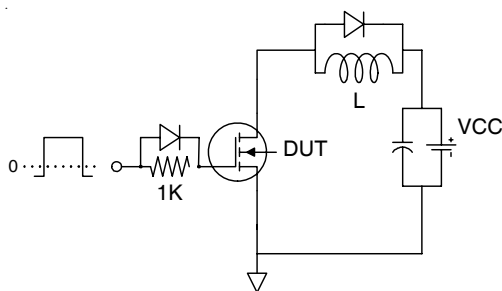**Fig 22a.** Unclamped Inductive Test Circuit
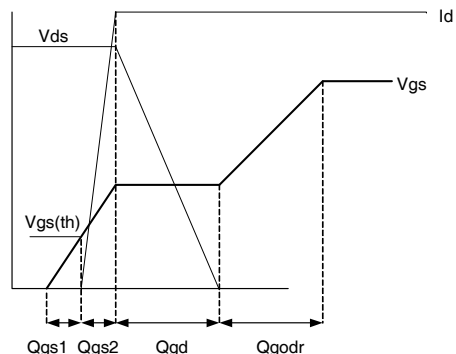


**Fig 22b.** Unclamped Inductive Waveforms



**Fig 23a.** Switching Time Test Circuit
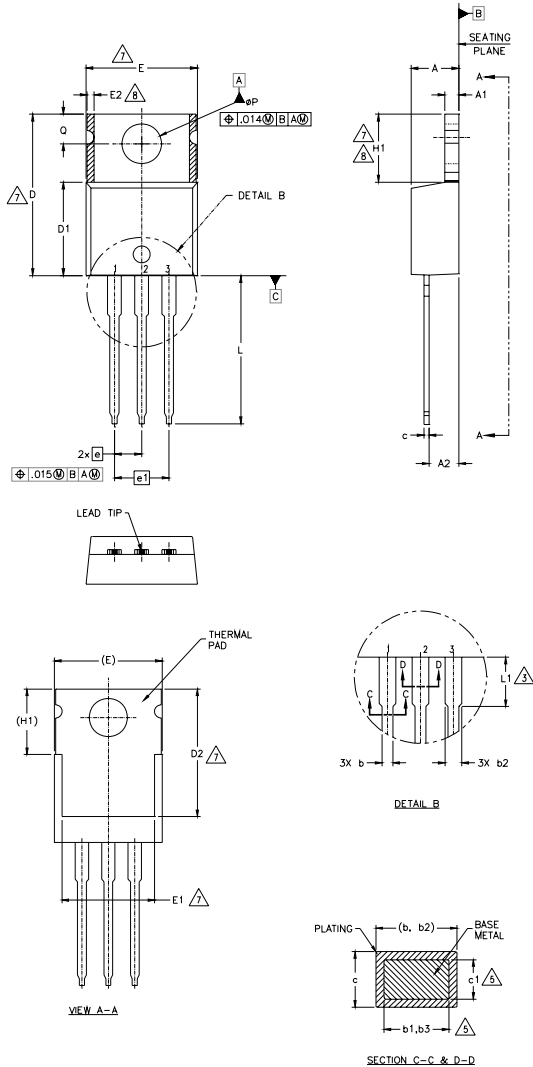


**Fig 23b.** Switching Time Waveforms



**Fig 24a.** Gate Charge Test Circuit



**Fig 24b.** Gate Charge Waveform

IRFB3077PbF

International **IQR** Rectifier

## TO-220AB Package Outline  (Dimensions are shown in millimeters (inches))



NOTES:
1.– DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M– 1994.
2.– DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.– DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.– DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.– CONTROLLING DIMENSION : INCHES.
7.– THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.– DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.– OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

| SYMBOL | DIMENSIONS | | | | NOTES |
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
|---|---|---|---|---|---|
| A | 3.56 | 4.83 | .140 | .190 | |
| A1 | 0.51 | 1.40 | .020 | .055 | |
| A2 | 2.03 | 2.92 | .080 | .115 | |
| b | 0.38 | 1.01 | .015 | .040 | |
| b1 | 0.38 | 0.97 | .015 | .038 | 5 |
| b2 | 1.14 | 1.78 | .045 | .070 | |
| b3 | 1.14 | 1.73 | .045 | .068 | 5 |
| c | 0.36 | 0.61 | .014 | .024 | |
| c1 | 0.36 | 0.56 | .014 | .022 | 5 |
| D | 14.22 | 16.51 | .560 | .650 | 4 |
| D1 | 8.38 | 9.02 | .330 | .355 | |
| D2 | 11.68 | 12.88 | .460 | .507 | 7 |
| E | 9.65 | 10.67 | .380 | .420 | 4,7 |
| E1 | 6.86 | 8.89 | .270 | .350 | 7 |
| E2 | – | 0.76 | – | .030 | 8 |
| e | 2.54 BSC | | .100 BSC | | |
| e1 | 5.08 BSC | | .200 BSC | | |
| H1 | 5.84 | 6.86 | .230 | .270 | 7,8 |
| L | 12.70 | 14.73 | .500 | .580 | |
| L1 | 3.56 | 4.06 | .140 | .160 | 3 |
| øP | 3.54 | 4.08 | .139 | .161 | |
| Q | 2.54 | 3.42 | .100 | .135 | |

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
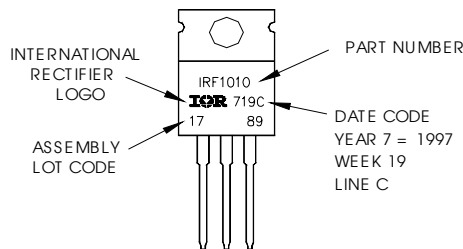3.– SOURCE

IGBTs, CoPACK
1.– GATE
2.– COLLECTOR
3.– EMITTER

DIODES
1.– ANODE
2.– CATHODE
3.– ANODE

## TO-220AB Part Marking Information

EXAMPLE:  THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

**Note:**  "P" in assembly line position indicates "Lead-Free"



INTERNATIONAL RECTIFIER LOGO

PART NUMBER

ASSEMBLY LOT CODE

DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C

TO-220AB packages are not recommended for Surface Mount Application.
**Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/**

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International **IQR** Rectifier