

## 阅读申明

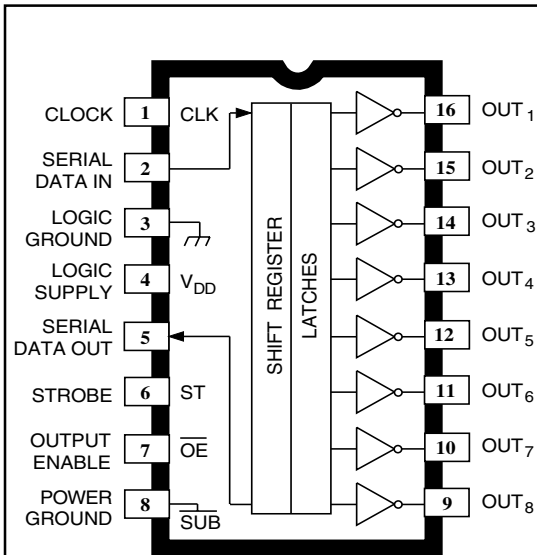
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# 5821 AND 5822

## BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS



Dwg. PP-026A

Note the DIP package and the SOIC package are electrically identical and share common terminal number assignments.

### ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage, $V_{OUT}$	
UCN5821A & UCN5821LW.....	50 V
UCN5822A & UCN5822LW.....	80 V
Logic Supply Voltage, $V_{DD}$ .....	15 V
Input Voltage Range,	
$V_{IN}$ .....	-0.3 V to $V_{DD} + 0.3$ V
Continuous Output Current,	
$I_{OUT}$ .....	500 mA
Package Power Dissipation, $P_D$	
Package Code 'A' .....	2.1 W
Package Code 'LW' .....	1.5 W
Operating Temperature Range,	
$T_A$ .....	-20°C to +85°C
Storage Temperature Range,	
$T_S$ .....	-55°C to +150°C

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

A merged combination of bipolar and MOS technology gives these devices an interface flexibility beyond the reach of standard logic buffers and power driver arrays. The UCN5821A, UCN5821LW, UCN5822A, and UCN5822LW each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sinking Darlington output drivers. The UCN5821A/LW and UCN5822A/LW are identical except for rated output voltage.

BiMOS II devices have much higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS and NMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

The UCN5821/22A are furnished in a standard 16-pin plastic DIP; the UCN5821/22LW are in a 16-lead wide-body SOIC for surface-mount applications. The UCN5821A is also available for operation from -40°C to +85°C. To order, change the prefix from 'UCN' to 'UCQ'.

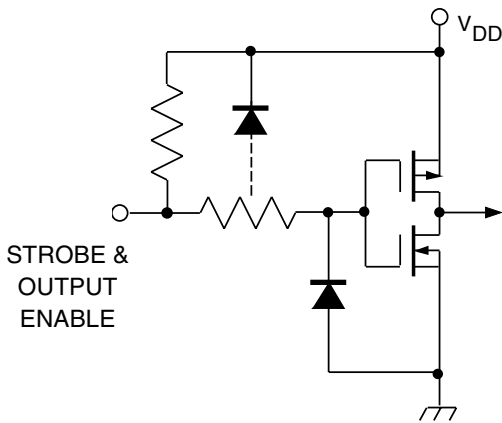
### FEATURES

- To 3.3 MHz Data Input Rate
- CMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Logic & Latches
- High-Voltage Current-Sink Outputs
- Automotive Capable

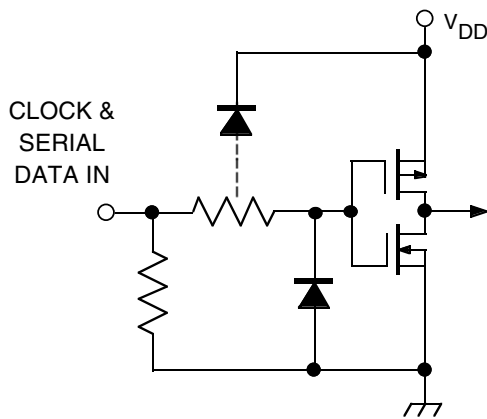
Always order by complete part number, e.g., **UCN5821A**.

# 5821 AND 5822 8-BIT SERIAL-INPUT, LATCHED DRIVERS

## TYPICAL INPUT CIRCUITS

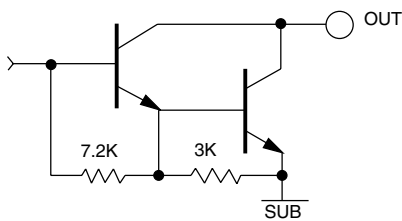


Dwg. EP-010-3



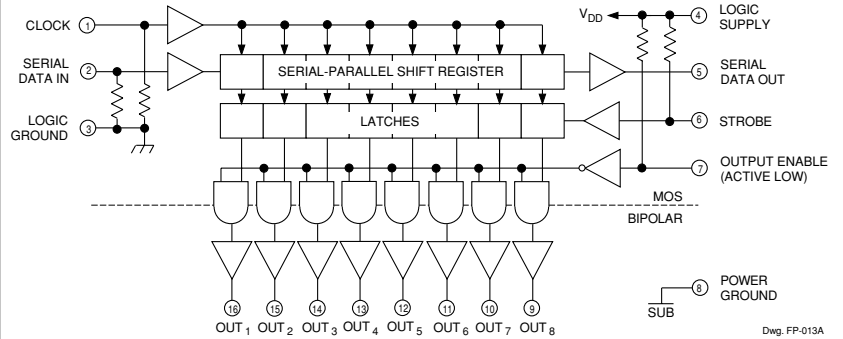
Dwg. EP-010-4A

## TYPICAL OUTPUT DRIVER



Dwg. No. A-14,314

## FUNCTIONAL BLOCK DIAGRAM



NOTE — There is an indeterminate resistance between logic ground and power ground. For proper operation, these terminals must be externally connected together.

Number of Outputs ON ( $I_{OUT} = 200\text{ mA}$ $V_{DD} = 12\text{ V}$ )	UCN5821A Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	90%	79%	72%	65%	57%
7	100%	90%	82%	74%	65%
6	100%	100%	96%	86%	76%
5	100%	100%	100%	100%	91%
4	100%	100%	100%	100%	100%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

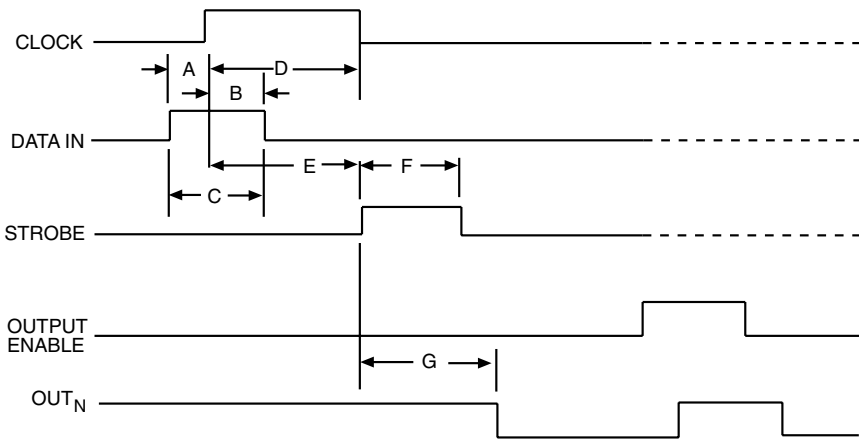
Number of Outputs ON ( $I_{OUT} = 200\text{ mA}$ $V_{DD} = 12\text{ V}$ )	UCN5821LW Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	67%	59%	54%	49%	43%
7	77%	68%	62%	56%	49%
6	90%	79%	72%	65%	57%
5	100%	95%	86%	78%	68%
4	100%	100%	100%	98%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

**5821 AND 5822**  
**8-BIT SERIAL-INPUT,**  
**LATCHED DRIVERS**

**ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ , (unless otherwise specified).**

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	$I_{CEX}$	UCN5821A/LW, $V_{OUT} = 50\text{ V}$	—	50	$\mu\text{A}$
		UCN5822A/LW, $V_{OUT} = 80\text{ V}$	—	50	$\mu\text{A}$
		UCN5821A/LW, $V_{OUT} = 50\text{ V}$ , $T_A = +70^\circ\text{C}$	—	100	$\mu\text{A}$
		UCN5822A/LW, $V_{OUT} = 80\text{ V}$ , $T_A = +70^\circ\text{C}$	—	100	$\mu\text{A}$
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\text{ mA}$	—	1.1	V
		$I_{OUT} = 200\text{ mA}$	—	1.3	V
		$I_{OUT} = 350\text{ mA}$ , $V_{DD} = 7.0\text{ V}$	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\text{ V}$	10.5	—	V
		$V_{DD} = 5.0\text{ V}$	3.5	—	V
Input Resistance	$r_{IN}$	$V_{DD} = 12\text{ V}$	50	—	$\text{k}\Omega$
		$V_{DD} = 5.0\text{ V}$	50	—	$\text{k}\Omega$
Supply Current	$I_{DD(ON)}$	One Driver ON, $V_{DD} = 12\text{ V}$	—	4.5	mA
		One Driver ON, $V_{DD} = 10\text{ V}$	—	3.9	mA
		One Driver ON, $V_{DD} = 5.0\text{ V}$	—	2.4	mA
	$I_{DD(OFF)}$	$V_{DD} = 5.0\text{ V}$ , All Drivers OFF, All Inputs = 0 V	—	1.6	mA
		$V_{DD} = 12\text{ V}$ , All Drivers OFF, All Inputs = 0 V	—	2.9	mA

# 5821 AND 5822 8-BIT SERIAL-INPUT, LATCHED DRIVERS



Dwg. No. A-12,627

## TIMING CONDITIONS

(V<sub>DD</sub> = 5.0 V, T<sub>A</sub> = +25°C, Logic Levels are V<sub>DD</sub> and Ground)

- A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**
- B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**
- C. Minimum Data Pulse Width ..... **150 ns**
- D. Minimum Clock Pulse Width ..... **150 ns**
- E. Minimum Time Between Clock Activation and Strobe ..... **30 ns**
- F. Minimum Strobe Pulse Width ..... **100 ns**
- G. Typical Time Between Strobe Activation and Output Transition ..... **1.0 μs**

Serial Data present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

## TRUTH TABLE

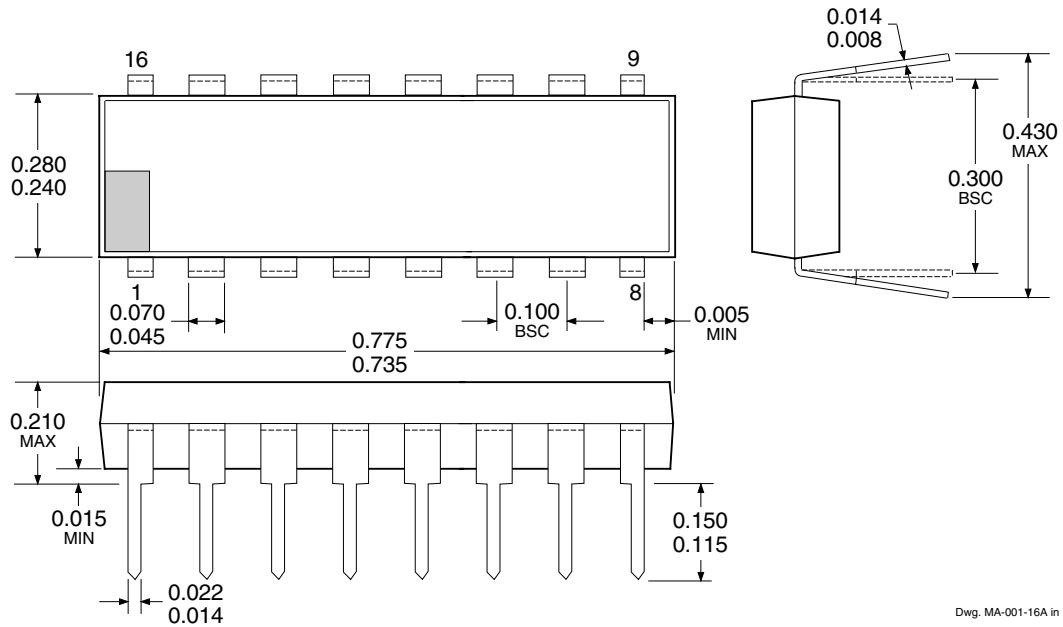
Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Enable	Output Contents						
		I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	.....	I <sub>8</sub>	R <sub>1</sub>			R <sub>2</sub>	R <sub>3</sub>	.....	R <sub>8</sub>	L <sub>1</sub>	L <sub>2</sub>		L <sub>3</sub>	.....	L <sub>8</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	.....
H	┌	H	R <sub>1</sub>	R <sub>2</sub>	.....	R <sub>7</sub>	R <sub>7</sub>																
L	┐	L	R <sub>1</sub>	R <sub>2</sub>	.....	R <sub>7</sub>	R <sub>7</sub>																
X	└	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	.....	R <sub>8</sub>	R <sub>8</sub>																
		X	X	X	.....	X	X	L		R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	.....	R <sub>8</sub>									
		P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	.....	P <sub>8</sub>	P <sub>8</sub>	H		P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	.....	P <sub>8</sub>	L								
					.....					X	X	X	.....	X	H								

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State



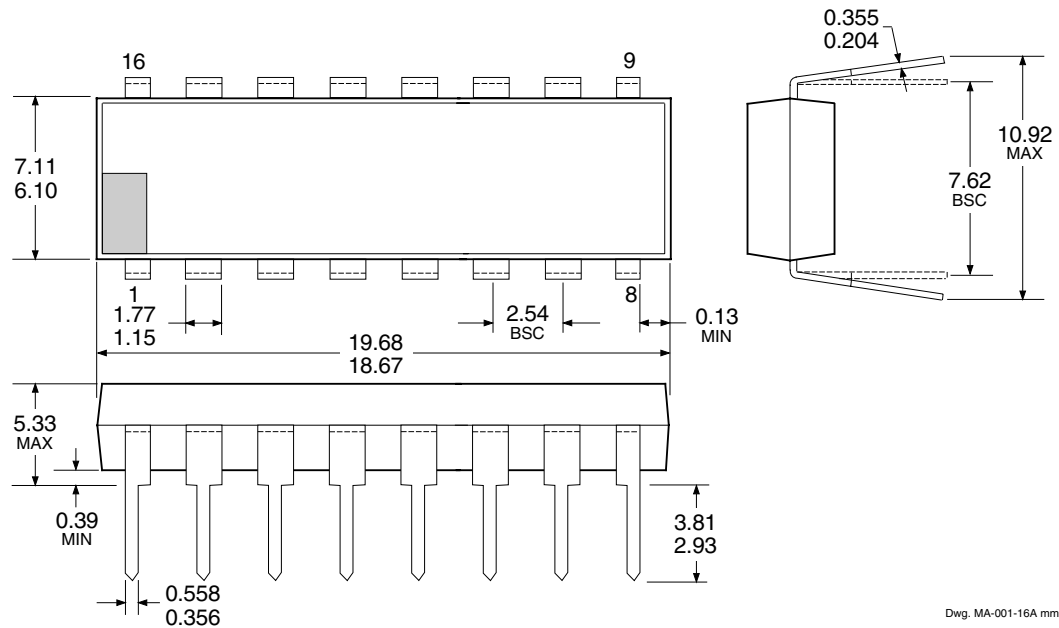
# 5821 AND 5822 8-BIT SERIAL-INPUT, LATCHED DRIVERS

## UCN5821A and UCN5822A Dimensions in Inches (controlling dimensions)



Dwg. MA-001-16A in

## Dimensions in Millimeters (for reference only)

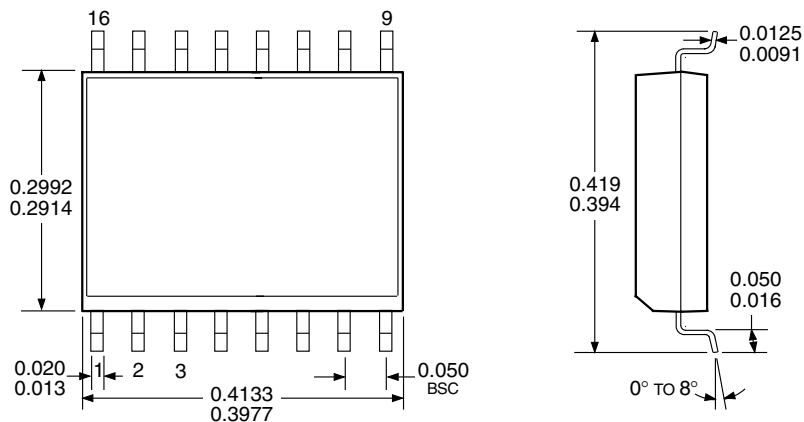


Dwg. MA-001-16A mm

- NOTES:
1. Lead thickness is measured at seating plane or below.
  2. Lead spacing tolerance is non-cumulative.
  3. Exact body and lead configuration at vendor's option within limits shown.

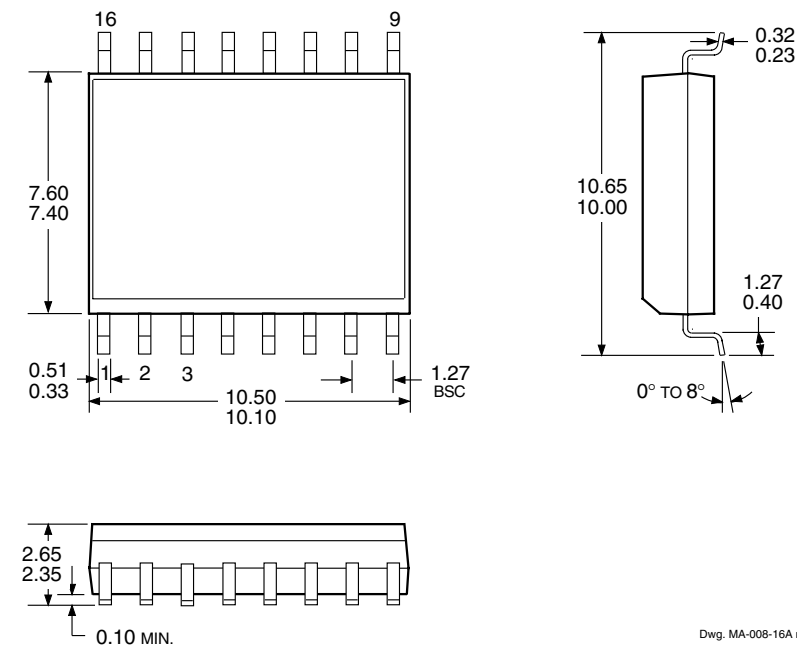
# 5821 AND 5822 8-BIT SERIAL-INPUT, LATCHED DRIVERS

## UCN5821LW and UCN5822LW Dimensions in Inches (for reference only)



Dwg. MA-008-16A in

## Dimensions in Millimeters (controlling dimensions)



Dwg. MA-008-16A mm

- NOTES: 1. Lead spacing tolerance is non-cumulative.  
2. Exact body and lead configuration at vendor's option within limits shown.

**5821 AND 5822  
8-BIT SERIAL-INPUT,  
LATCHED DRIVERS**

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**5821 AND 5822**  
**8-BIT SERIAL-INPUT,**  
**LATCHED DRIVERS**

**POWER**  
**INTERFACE DRIVERS**

Function	Output Ratings*		Part Number†
<b>SERIAL-INPUT LATCHED DRIVERS</b>			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	80 V	5822
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
8-Bit (constant-current LED driver)	75 mA	17 V	6275
8-Bit (DMOS drivers)	250 mA	50 V	6595
8-Bit (DMOS drivers)	350 mA	50 V‡	6A595
8-Bit (DMOS drivers)	100 mA	50 V	6B595
10-Bit (active pull-downs)	-25 mA	60 V	5810-F and 6809/10
12-Bit (active pull-downs)	-25 mA	60 V	5811 and 6811
16-Bit (constant-current LED driver)	75 mA	17 V	6276
20-Bit (active pull-downs)	-25 mA	60 V	5812-F and 6812
32-Bit (active pull-downs)	-25 mA	60 V	5818-F and 6818
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
<b>PARALLEL-INPUT LATCHED DRIVERS</b>			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
8-Bit (DMOS drivers)	100 mA	50 V	6B273
8-Bit (DMOS drivers)	250 mA	50 V	6273
<b>SPECIAL-PURPOSE DEVICES</b>			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 8-Bit Decoder/DMOS Driver	250 mA	50 V	6259
Addressable 8-Bit Decoder/DMOS Driver	350 mA	50 V‡	6A259
Addressable 8-Bit Decoder/DMOS Driver	100 mA	50 V	6B259
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

\* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

