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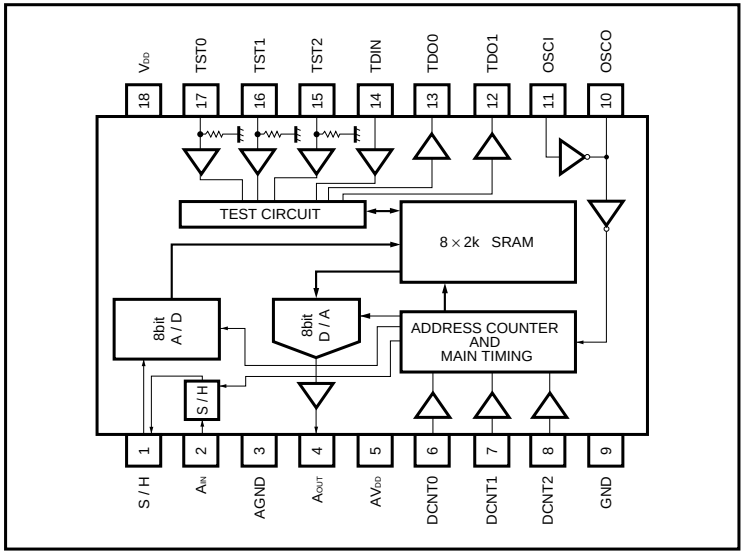
Audio digital delay (KARAOKE echo)
BU9252S / BU9252F

The BU9252S and BU9252F are digital delays specifically for Karaoke systems. Each has an internal sample hold circuit, an 8-bit A / D and D / A converter and 2kB SRAM, and allows for the selection of one of eight delay times just by attaching an inexpensive ceramic resonator.
A digital echo system can be formed by using either of these ICs together with the BA7725S or BA7725FS.

●Applications
Karaoke echo system
Electronic circuits that require signal delays

●Features
1) Internal digital delay circuit.
2) Internal 8-bit A / D converter. Sample rate. (14.22kHz when f_{OSC} = 455kHz).
3) Internal 2k bytes data SRAM.
4) Internal 8-bit D / A converter.
5) CMOS design for low power consumption.
6) Internal sample hold circuit.
7) Internal feedback resistors and capacitors for oscillator circuits.

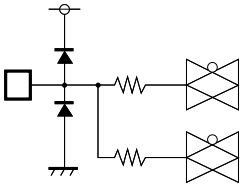
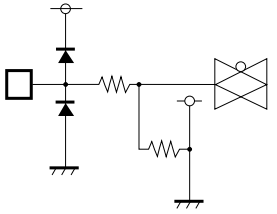
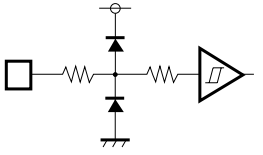
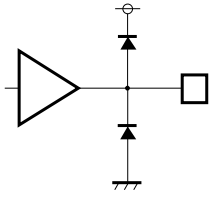
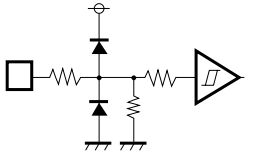
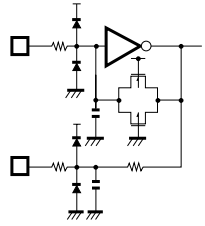
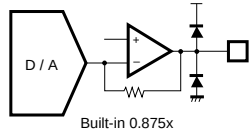
●Block diagram



●Pin descriptions

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	S / H	For attaching sample-and-hold capacitor	10	OSCO	Oscillator pin 2
2	A_{IN}	Analog input	11	OSCI	Oscillator pin 1
3	AGND	Analog circuit ground	12	TDO1	Test pin (output)
4	A_{OUT}	Analog output	13	TDO0	Test pin (output)
5	AV_{DD}	Analog circuit power supply	14	TDIN	Test pin (input)
6	DCNT0	Delay setting input	15	TST2	Test mode setting
7	DCNT1	Delay setting input	16	TST1	Test mode setting
8	DCNT2	Delay setting input	17	TST0	Test mode setting
9	GND	Digital circuit ground	18	V_{DD}	Digital circuit power supply

●Input / output circuits

Pin name	Pin No.	Internal equivalent circuit
S / H	1	
A_{IN}	2	
TDIN DCNT0 DCNT1 DCNT2	14 6 7 8	
TDO0 TDO1	13 12	
TST0 TST1 TST2	17 16 15	
OSCI OSCO	11 10	
A_{OUT}	4	 Built-in 0.875x amplifier as output buffer.

●Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Power supply voltage		V_{DD}	– 0.3 ~ + 7.0	V
Power dissipation	BU9252S	Pd	600*1	mW
	BU9252F		450*2	
Storage temperature		Tstg	– 55 ~ + 125	°C
Input voltage		V_{IN}	– 0.3 ~ V_{DD} + 0.3	V
Output voltage		V_{OUT}	– 0.3 ~ V_{DD} + 0.3	V

*1 IC only. Reduce by – 6mW / °C for each in Ta of 1°C over 25°C.

*2 IC only. Reduce by – 4.5mW / °C for each in Ta of 1°C over 25°C.

●Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	4.5 ~ 5.5	V
Analog power supply voltage	AV_{DD}	V_{DD}	V
Input "L" voltage	V_{IL}	0.0 ~ 0.2V_{DD}	V
Input "H" voltage	V_{IH}	0.8V_{DD} ~ V_{DD}	V
Analog input voltage	V_{AIN}	0 ~ AV_{DD}	V
Clock frequency	f_{OSC}	200 ~ 1000	kHz
Operating temperature	Topr	– 10 ~ + 70	°C

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = AV_{DD} = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply current	I_{DD}	—	3.5	12	mA	V_{AIN} = AV_{DD}, f_{OSC} = 455kHz
Analog output current	I_{AOUT}	1	4	—	mA	V_{AOUT} = 1V, V_{AIN} = 0V
		0.3	0.8	—	mA	V_{AOUT} = 0.5V_{DD}, V_{AIN} = V_{DD}
Analog input impedance	R_{AIN}	12	25	60	kΩ	*
A / D to D / A precision	RES	—	2	—	LSB	
OSCO output "L" voltage	V_{LOSC}	—	0.6	1.2	V	I_{OL} = 100μA
OSCO output "H" voltage	V_{HOSC}	3.8	4.4	—	V	I_{OH} = – 100μA
OSCI feedback loop current	I_{OSCI}	1	6	20	μA	V_{OSCI} = V_{DD}
Oscillation capacity	—	—	150	—	pF	

* The bias circuit is impedance.

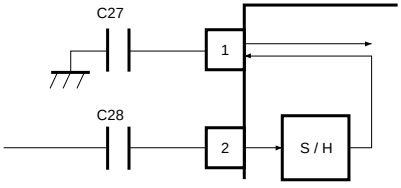
●Circuit operation

(1) External capacitor for signal input pin

Audio signals compressed by the BA7725S or BA7725FS have their DC component removed by an AC coupling capacitor and are then input to pin 2 of BU9252S or BU9252F. At this stage, level deviations occur because the input signal is capacitor-divided by this AC coupling capacitor C28 and by sampling hold capacitor C27 connected to pin 1.

To prevent this, make sure that C27 is much lower than C28.

(Note: The numbers of external components are the numbers used in the system application example.)



The sample-held analog signal is converted to digital by the serial 8-bit A / D converter and then temporarily stored in the internal SRAM (2k bytes).

(2) Relationship between oscillation frequency (CLK) and delay time

Sample rate F = fosc / 32 (fosc: oscillation frequency)

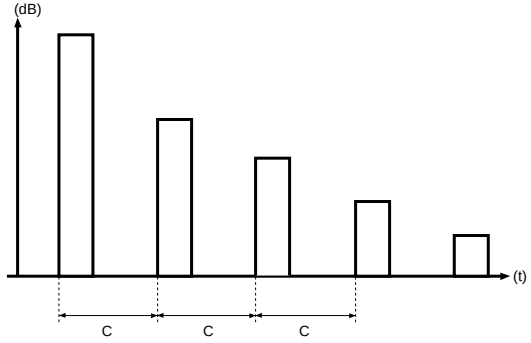
F = 14.22kHz at fosc = 455kHz

Sample period T = 1 / F

Delay time Dtime = T × number of counts

(3) Delay timer settings

The delay time (i.e., the length of time the signal is stored in the SRAM) can be set to any of eight settings between the maximum and minimum delay times by setting pins 6, 7 and 8 to the combination of logic signal inputs that results in the corresponding number of counts. The maximum and minimum delay times are determined by the oscillation frequency of the attached ceramic resonator.



C : Delay time (ms)

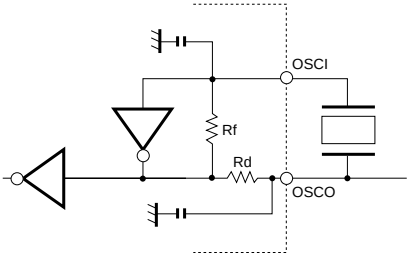
The delay time can be set to any of the eight settings shown below by setting the logic inputs of terminals DCNT0 through DCNT2.

Logic input			Count	Delay time (ms) (when fosc = 455kHz)
DCNT1	DCNT2	DCNT0	BU9252S / F	BU9252S / F
0	0	0	256	18.00
0	0	1	512	36.01
0	1	0	768	54.01
0	1	1	1024	72.02
1	0	0	1280	90.02
1	0	1	1536	108.03
1	1	0	1792	126.03
1	1	1	2048	144.04

Maximum and minimum delay times when using 300kHz, 375kHz and 455kHz ceramic oscillators

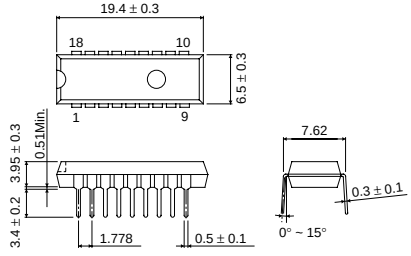
Delay time (ms)					
300kHz		375kHz		455kHz	
Max.	Min.	Max.	Min.	Max.	Min.
218.45	27.30	174.76	21.85	144.04	18.00

(4) Peripheral components of the ceramic oscillator
An oscillator circuit can be configured simply by attaching a 455kHz ceramic resonator.



●External dimensions (Units: mm)

BU9252S



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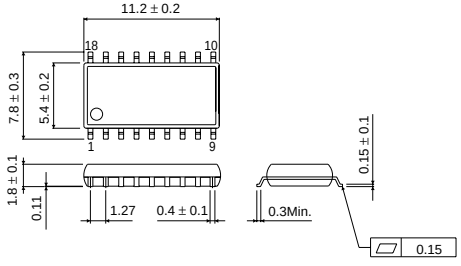
BU9252F



SOP18