SL28779

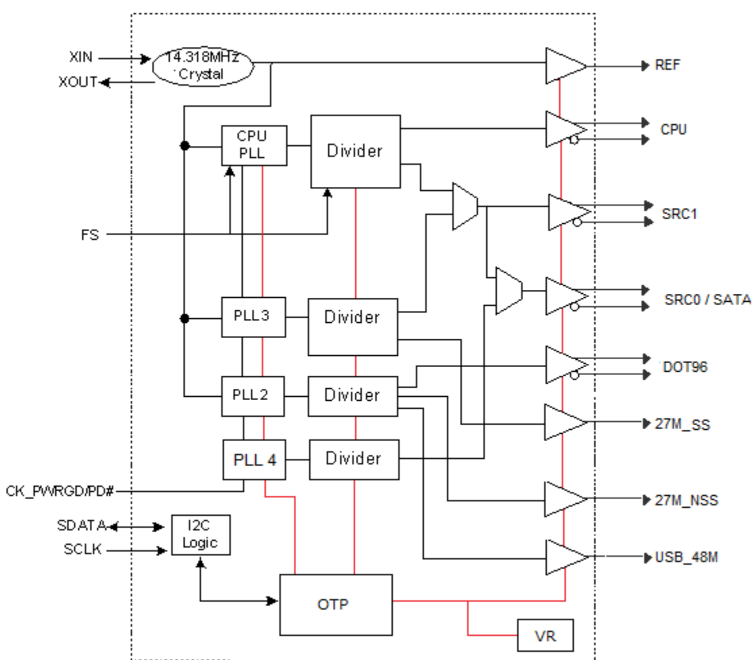
EProClock® Generator for Intel Calpella Chipset

Features

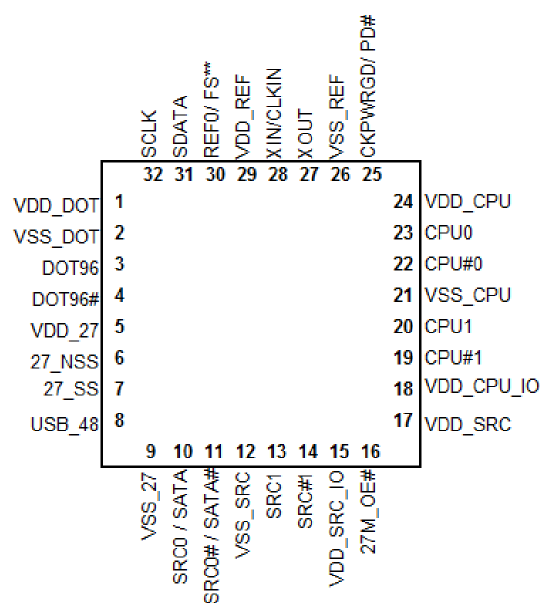
- Intel CK505 Clock Revision 1.0 Compliant
- Hybrid Video Support - Simultaneous DOT96, 27MHz_SS and 27MHz_NSS video clocks
- PCI-Express Gen 2 Compliant
- Low power push-pull type differential output buffers
- Integrated voltage regulator
- Integrated resistors on differential clocks
- Scalable low voltage VDD_IO (3.3V to 1.05V)
- Wireless friendly 3-bits slew rate control on single-ended clocks.
- Differential CPU clocks with selectable frequency
- 100MHz Differential SRC clocks
- 100MHz Differential SATA clocks
- 96MHz Differential DOT clock
- 27MHz Video clock
- 48MHz USB clock
- Buffered Reference Clock 14.318MHz
- 14.318MHz Crystal Input or Clock input
- EProClock® Programmable Technology
- I²C support with readback capabilities
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V Power supply
- 32-pin QFN package

CPU	SRC	SATA	DOT96	USB_48	REF	27M
x2	x1	x 1	x 1	x1	x1	x2

Block Diagram



Pin Configuration



** Internal 100K-ohm Pull-Down Resistor

400 West Cesar Chavez, Austin, TX 78701 1+(512) 416-8500 1+(512) 416-9669 www.silabs.com

32-QFN Pin Definitions

Pin No.	Name	Type	Description
1	VDD_DOT	PWR	3.3V Power supply for outputs and PLL
2	VSS_DOT	GND	Ground for outputs
3	DOT96	O, DIF	Fixed true 96MHz clock output
4	DOT96#	O, DIF	Fixed complement 96MHz clock output
5	VDD_27	PWR	3.3V Power supply for 27MHz PLL
6	27M_NSS	O,SE	Non-spread 27MHz video clock output
7	27M_SS	O, SE	Spread 27MHz video clock output
8	USB_48	O,SE	Non-spread 48MHz video clock output
9	VSS_27	GND	Ground for 27MHz PLL
10	SRC0 / SATA	O, DIF	100MHz True differential serial reference clock
11	SRC0# / SATA#	O, DIF	100MHz Complement differential serial reference clock
12	VSS_SRC	GND	Ground for PLL
13	SRC1	O, DIF	100MHz True differential serial reference clock
14	SRC1#	O, DIF	100MHz Complement differential serial reference clock
15	VDD_SRC_IO	PWR	Scalable 3.3V to 1.05V power supply for output buffer
16	27_OE#	I	3.3V tolerance input pin to enable and disable both 27_NSS and 27_SS
17	VDD_SRC	PWR	3.3V Power supply for PLL
18	VDD_CPU_IO	PWR	Scalable 3.3V to 1.05V power supply for output buffer
19	CPU1#	O, DIF	Complement differential CPU clock output
20	CPU1	O, DIF	True differential CPU clock output
21	VSS_CPU	GND	Ground for PLL
22	CPU0#	O, DIF	Complement differential CPU clock output
23	CPU0	O, DIF	True differential CPU clock output
24	VDD_CPU	PWR	3.3V Power supply for CPU PLL
25	CKPWRGD/PD#	I	3.3V LVTTL input. This pin is a level sensitive strobe used to latch the FS. After CKPWRGD (active HIGH) assertion, this pin becomes a real-time input for asserting power down (active LOW)
26	VSS_REF	GND	Ground for outputs
27	XOUT	O, SE	14.318MHz Crystal output, *Float XOUT if using only CLKIN (Clock input)*
28	XIN/CLKIN	I	14.318MHz Crystal input or 3.3V, 14.318MHz Clock Input
29	VDD_REF	PWR	3.3V Power supply for outputs and also maintains SMBUS registers during power-down
30	REF/FS**	PD, I/O	3.3V tolerant input for Graphic clock selection/fixed 14.318MHz clock output. (*Internal 100K-ohm pull-down resistor on FS pin*) *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications*
31	SDATA	I/O	SMBus compatible SDATA
32	SCLK	I	SMBus compatible SCLOCK

PC EProClock® Programmable Technology

PC EProClock® is the world's first non-volatile programmable PC clock. The PC EProClock® technology allows board designer to promptly achieve optimum compliance and clock signal integrity; historically, attainable typically through device and/or board redesigns.

PC EProClock® technology can be configured through SMBus or hard coded.

Features:

- > 4000 bits of configurations
- Can be configured through SMBus or hard coded
- Custom frequency sets
- Differential skew control on true or compliment or both
- Differential duty cycle control on true or compliment or both
- Differential amplitude control
- Differential and single-ended slew rate control
- Program Internal or External series resistor on single-ended clocks
- Program different spread profiles
- Program different spread modulation rate

Frequency Select Pin (FS)

FS	CPU	Power On	SRC	SATA	DOT96	USB_48	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	48MHz	27MHz	14.318MHz
1	100MHz							

Frequency Select Pin FS

Apply the appropriate logic levels to FS inputs before CKPWRGD assertion to achieve host clock frequency selection. When the clock chip sampled HIGH on CKPWRGD and indicates that VTT voltage is stable then FS input values are sampled. This process employs a one-shot functionality and once the CKPWRGD sampled a valid HIGH, all other FS, and CKPWRGD transitions are ignored except in test mode.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits

Table 2. Block Read and Block Write Protocol (continued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	HW	FS	CPU Frequency Select Bit, set by HW 0 = 133MHz, 1= 100MHz
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	0	iAMT_EN	iAMT Enable 0 = Legacy Mode, 1 = iAMT Enabled
3	0	RESERVED	RESERVED
2	0	SRC_Main_SEL	Select source for SRC clock 0 = SRC_MAIN = PLL1, *PLL3_CFG Table applies* 1 = SRC_MAIN = PLL3, *PLL3_CFG Table does not apply*
1	0	SATA_SEL	Select source of SATA clock 0 = SATA = SRC_MAIN, 1= SATA = PLL4
0	1	PD_Restore	Save configuration when PD# is asserted 0 = Config. cleared, 1 = Config. saved

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	0	PLL1_SS_DC	Select for down or center SS 0 = Down spread, 1 = Center spread
5	0	PLL3_SS_DC	Select for down or center SS 0 = Down spread, 1 = Center spread
4	0	PLL3_CFB3	CFB Bit [4:1] only applies when SRC_Main_SEL = 0 (Byte 0, bit 2 =0) See Table 4 on page 9 for Configuration.
3	0	PLL3_CFB2	
2	1	PLL3_CFB1	
1	0	PLL3_CFB0	
0	1	RESERVED	RESERVED

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	REF_OE	Output enable for REF 0 = Output Disabled, 1 = Output Enabled
6	1	USB_48_OE	Output enable for USB_48 0 = Output Disabled, 1 = Output Enabled
5	1	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED

Byte 3: Control Register 3

5	1	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	SATA_OE	Output enable for SATA 0 = Output Disabled, 1 = Output Enabled
5	1	SRC_OE	Output enable for SRC 0 = Output Disabled, 1 = Output Enabled
4	1	DOT96_OE	Output enable for DOT96 0 = Output Disabled, 1 = Output Enabled
3	1	CPU1_OE	Output enable for CPU1 0 = Output Disabled, 1 = Output Enabled
2	1	CPU0_OE	Output enable for CPU0 0 = Output Disabled, 1 = Output Enabled
1	1	PLL1_SS_EN	Enable PLL1s spread modulation, 0 = Spread Disabled, 1 = Spread Enabled
0	1	PLL3_SS_EN	Enable PLL3s spread modulation 0 = Spread Disabled, 1 = Spread Enabled

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	REF Bit1	REF slew rate control *(see Byte 13 for Slew Rate Bit 0 and Bit 2)* 0 = High, 1 = Low
4	0	RESERVED	RESERVED
3	0	27MHz Bit 1	27MHz slew rate control *(see Byte 13 for Slew Rate Bit 0 and Bit 2)* 0 = High, 1 = Low
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED

Byte 6: Control Register 6

0	0	RESERVED	RESERVED

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Rev Code Bit 3	Revision Code Bit 3
6	0	Rev Code Bit 2	Revision Code Bit 2
5	1	Rev Code Bit 1	Revision Code Bit 1
4	0	Rev Code Bit 0	Revision Code Bit 0
3	1	Vendor ID bit 3	Vendor ID Bit 3
2	0	Vendor ID bit 2	Vendor ID Bit 2
1	0	Vendor ID bit 1	Vendor ID Bit 1
0	0	Vendor ID bit 0	Vendor ID Bit 0

Byte 8: Control Register 8

Bit	@Pup	Name	Description
7	1	Device_ID3	RESERVED
6	0	Device_ID2	RESERVED
5	0	Device_ID1	RESERVED
4	0	Device_ID0	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	1	27M_non-SS_OE	Output enable for 27M_non-SS 0 = Output Disabled, 1 = Output Enabled
0	1	27M_SS_OE	Output enable for 27M_SS 0 = Output Disabled, 1 = Output Enabled

Byte 9: Control Register 9

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	0	TEST _MODE_SEL	Test mode select either REF/N or tri-state 0 = All outputs tri-state, 1 = All output REF/N
3	0	TEST_MODE_ENTRY	Allows entry into test mode 0 = Normal Operation, 1 = Enter test mode(s)
2	1	I2C_VOUT<2>	Amplitude configurations differential clocks I2C_VOUT[2:0] 000 = 0.30V 001 = 0.40V 010 = 0.50V 011 = 0.60V 100 = 0.70V 101 = 0.80V (default) 110 = 0.90V 111 = 1.00V
1	0	I2C_VOUT<1>	
0	1	I2C_VOUT<0>	

Byte 10: Control Register 10

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 11: Control Register 11

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	1	CPU1_iAMT_EN	CPU1 iAMT Clock Enabled 0 = Disabled, 1 = Enabled
1	1	PCI-e_GEN2	PCI-e_Gen2 Compliant 0 = non Gen2, 1= Gen2 Compliant
0	1	RESERVED	RESERVED

Byte 12: Byte Count

Bit	@Pup	Name	Description
7	0	BC7	Byte count register for block read operation. The default value for Byte count is 15. In order to read beyond Byte 15, the user should change the byte count limit.to or beyond the byte that is desired to be read.
6	0	BC6	
5	0	BC5	
4	0	BC4	
3	1	BC3	
2	1	BC2	
1	1	BC1	
0	1	BC0	

Byte 13: Control Register 13

Bit	@Pup	Name	Description

<table>
<tr><td>7</td><td>1</td><td>REF_Bit2</td><td rowspan="6">Drive Strength Control - Bit[2:0], Note: See Byte 6 Bit 5 for REF Slew Rate Bit 1 and Byte 6 Bit 3 for 27MHz Slew Rate Bit 1
Normal mode default ‘101’
Wireless Friendly Mode default to ‘111’
<table>
<tr><th>Mode</th><th>Bit2</th><th>Bit1</th><th>Bit0</th><th>Buffer Strength</th></tr>
<tr><td></td><td>0</td><td>0</td><td>0</td><td>Strong</td></tr>
<tr><td></td><td>0</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>0</td><td>1</td><td>0</td><td></td></tr>
<tr><td></td><td>0</td><td>1</td><td>1</td><td></td></tr>
<tr><td></td><td>1</td><td>0</td><td>0</td><td></td></tr>
<tr><td>Default</td><td>1</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>1</td><td>1</td><td>0</td><td></td></tr>
<tr><td>Wireless Friendly</td><td>1</td><td>1</td><td>1</td><td>Weak</td></tr>
</table>
</td></tr>
<tr><td>6</td><td>1</td><td>REF_Bit0</td></tr>
<tr><td>5</td><td>1</td><td>27MHz_NSS_Bit2</td></tr>
<tr><td>4</td><td>1</td><td>27MHz_NSS_Bit0</td></tr>
<tr><td>3</td><td>1</td><td>27MHz_SS_Bit2</td></tr>
<tr><td>2</td><td>1</td><td>27MHz_SS_Bit0</td></tr>
<tr><td>1</td><td>0</td><td>RESERVED</td><td>RESERVED</td></tr>
<tr><td>0</td><td>0</td><td>Wireless Friendly mode</td><td>Wireless Friendly Mode
0 = Disabled, Default all single-ended clocks slew rate config bits to ‘101’
1 = Enabled, Default all single-ended clocks slew rate config bits to ‘111’</td></tr>
</table>

Byte 14: Control Register 14

<table>
<tr><th>Bit</th><th>@Pup</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>1</td><td>USB_48_Bit2</td><td rowspan="3">Drive Strength Control - Bit[2:0] , Note: REF Bit 1is located in Byte 6 Bit 5 and 27MHz Bit 1 is located in Byte 6 Bit 3
Normal mode default ‘101’
Wireless Friendly Mode default to ‘111’
<table>
<tr><th>Mode</th><th>Bit2</th><th>Bit1</th><th>Bit0</th><th>Buffer Strength</th></tr>
<tr><td></td><td>0</td><td>0</td><td>0</td><td>Strong</td></tr>
<tr><td></td><td>0</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>0</td><td>1</td><td>0</td><td></td></tr>
<tr><td></td><td>0</td><td>1</td><td>1</td><td></td></tr>
<tr><td></td><td>1</td><td>0</td><td>0</td><td></td></tr>
<tr><td>Default</td><td>1</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>1</td><td>1</td><td>0</td><td></td></tr>
<tr><td>Wireless Friendly</td><td>1</td><td>1</td><td>1</td><td>Weak</td></tr>
</table>
</td></tr>
<tr><td>6</td><td>0</td><td>USB_48_Bit1</td></tr>
<tr><td>5</td><td>1</td><td>USB_48_Bit0</td></tr>
<tr><td>4</td><td>0</td><td>OTP_4</td><td rowspan="5">OTP_ID
Identification for programmed device</td></tr>
<tr><td>3</td><td>0</td><td>OTP_3</td></tr>
<tr><td>2</td><td>0</td><td>OTP_2</td></tr>
<tr><td>1</td><td>0</td><td>OTP_1</td></tr>
<tr><td>0</td><td>0</td><td>OTP_0</td></tr>
</table>

Table 4. Pin 6 and 7 Configuration Table

B1b4	B1b3	B1b2	B1b1	Pin7	Pin 8	Spread (%)
0	0	0	0	N/A	N/A	N/A
0	0	0	1	N/A	N/A	N/A
0	0	1	0	27M_NSS	27M_SS	-0.5%
0	0	1	1	27M_NSS	27M_SS	-1%
0	1	0	0	27M_NSS	27M_SS	-1.5%
0	1	0	1	27M_NSS	27M_SS	-2%
0	1	1	0	27M_NSS	27M_SS	-0.75V
0	1	1	1	27M_NSS	27M_SS	-1.25%

B1b4	B1b3	B1b2	B1b1	Pin7	Pin 8	Spread (%)
1	0	0	0	27M_NSS	27M_SS	-1.75%
1	0	0	1	27M_NSS	27M_SS	+/-0.5%
1	0	1	0	27M_NSS	27M_SS	+/-0.75%
1	0	1	1	N/A	N/A	N/A
1	1	0	0	N/A	N/A	N/A
1	1	0	1	N/A	N/A	N/A
1	1	1	0	N/A	N/A	N/A
1	1	1	1	N/A	N/A	N/A

Table 5. Output Driver Status during 27_OE#

	27M_OE# Asserted	27M_OE# Deasserted	SMBus OE Disabled
27M_SS & 27M_NSS	Stoppable	Running	Driven low
Other single-ended clocks	Running	Running	
Differential Clocks	Running	Running	Driven low
	Running	Running	
	Running	Running	

Table 6. Output Driver Status

	All Single-ended Clocks		All Differential Clocks	
	w/o Strap	w/ Strap	Clock	Clock#
PD# = 0 (Power down)	Low	Hi-z	Low	Low

Table 7. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

The SL28779 requires a Parallel Resonance Crystal. Substituting a series resonance crystal causes the SL28779 to operate at the wrong frequency and violates the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. It is important that the trim capacitors are in series with the crystal. It is not true that load capacitors are in parallel with the crystal and are approximately equal to the load capacitance of the crystal.

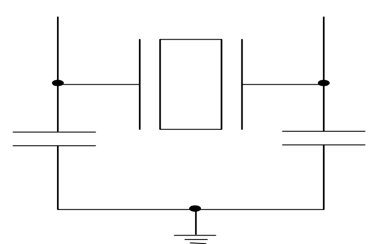


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. Again, the capacitance on each side is in series with the crystal. The total capacitance on both side is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.

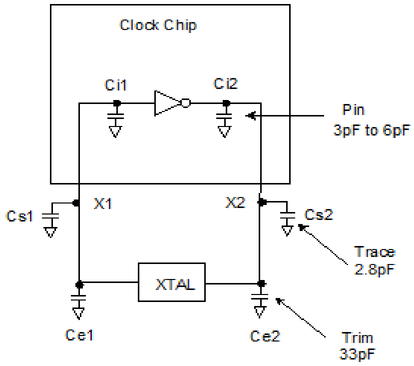


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL .... Crystal load capacitance

CLe ....Actual loading seen by crystal using standard value trim capacitors

Ce ....External trim capacitors

Cs .... Stray capacitance (terraced)

Ci .... Internal capacitance (lead frame, bond wires, etc.)

PD# (Power down) Clarification

The CKPWRGD/PD# pin is a dual-function pin. During initial power up, the pin functions as CKPWRGD. Once CKPWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, clocks are driven to a LOW value and held before turning off the VCOs and the crystal oscillator.

PD# (Power down) Assertion

When PD# is sampled LOW by two consecutive rising edges of CPU clocks, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must held LOW. When PD# mode is desired as the initial power on state, PD# must be asserted LOW in less than 10 μs after asserting CKPWRGD.

PD# Deassertion

The power up latency is less than 1.8 ms. This is the time from the deassertion of the PD# pin or the ramping of the power supply until the time that stable clocks are generated from the clock chip. All differential outputs stopped in a three-state condition, resulting from are driven high in less than 300 μs of PD# deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are enabled within a few clock cycles of each clock. *Figure 4* is an example showing the relationship of clocks coming up.

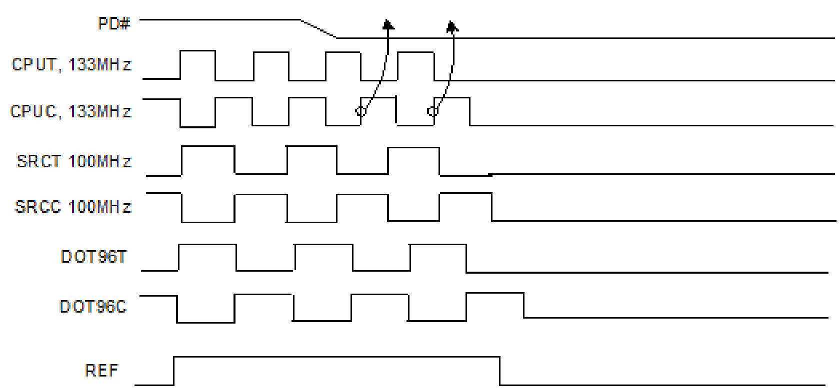


Figure 3. Power Down Assertion Timing Waveform

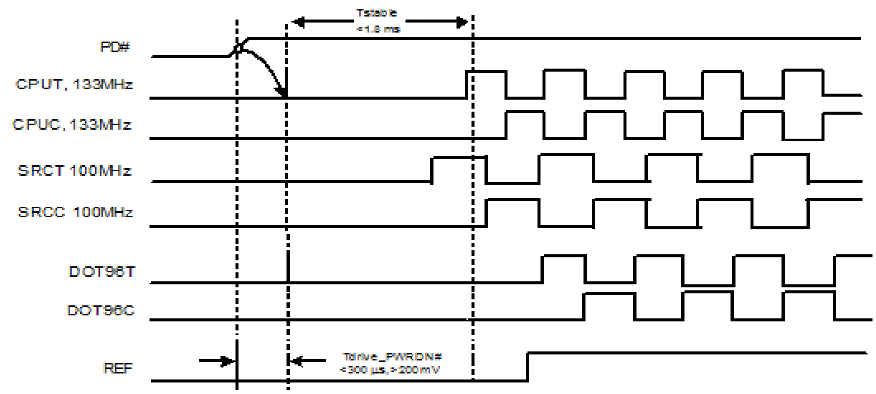


Figure 4. Power Down Deassertion Timing Waveform

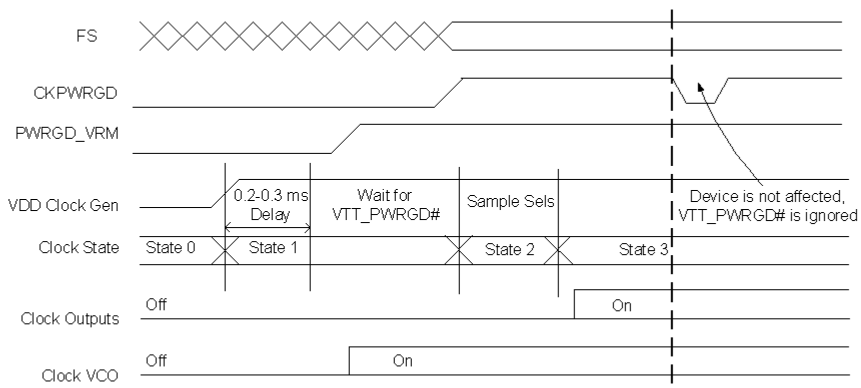


Figure 5. CKPWRGD Timing Diagram

27M_OE# Assertion

The 27M_OE# signal is an active LOW input used for stopping and starting both 27MHz spread and 27MHz non-spread output clocks while the rest of the clock generator continues to function. When the 27M_OE# pin is asserted, both 27MHz spread and 27MHz non-spread outputs are stopped after they are sampled by two falling edges of the internal 27MHz clock. The final states of the stopped 27MHz spread and 27MHz non-spread signals are LOW.

27M_OE# Deassertion

The deassertion of the 27M_OE# signal causes both stopped 27MHz spread and 27MHz non-spread outputs to resume normal operation in a synchronous manner. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two 27MHz clock cycles.

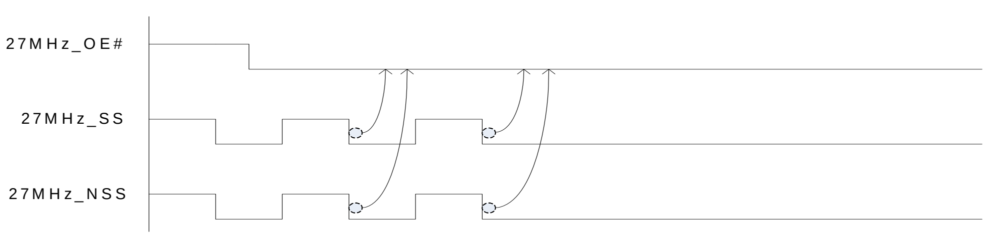


Figure 6. 27M_OE# Assertion Waveform

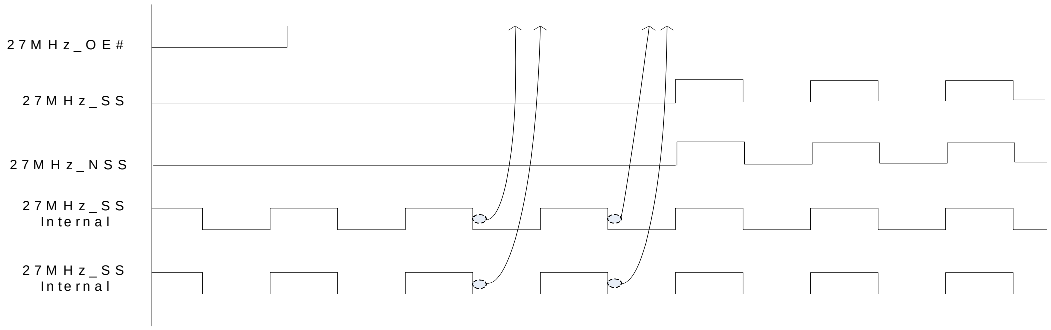


Figure 7. 27M_OE# Deassertion Waveform

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
$V_{DD\_3.3V}$	Main Supply Voltage	Functional	–	4.6	V
V_{DD_IO}	IO Supply Voltage	Functional		4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	4.6	V_{DC}
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	0	85	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Functional	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC (JESD 51)	2000	–	V
UL-94	Flammability Rating	JEDEC (JESD 22 - A114)	V–0		
MSL	Moisture Sensitivity Level	UL (Class)	1		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD core	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{IH}	3.3V Input High Voltage (SE)		2.0	V_{DD} + 0.3	V
V_{IL}	3.3V Input Low Voltage (SE)		V_{SS} – 0.3	0.8	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IH_FS}	FS Input High Voltage		0.7	VDD+0.3	V
V_{IL_FS}	FS Input Low Voltage		V_{SS} – 0.3	0.35	V
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	–	5	µA
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	–	µA
V_{OH}	3.3V Output High Voltage (SE)	I_{OH} = –1 mA	2.4	–	V
V_{OL}	3.3V Output Low Voltage (SE)	I_{OL} = 1 mA	–	0.4	V
$V_{DD\ IO}$	Low Voltage IO Supply Voltage		1	3.465	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		1.5	5	pF
C_{OUT}	Output Pin Capacitance			6	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V
$IDD_{\_PD}$	Power Down Current		–	1	mA
$I_{DD\_3.3V}$	Dynamic Supply Current	All outputs enabled. SE clocks with 8” traces. Differential clocks with 7” traces. Loading per CK505 spec.	–	65	mA
$I_{DD\_VDD\_IO}$	Dynamic Supply Current	All outputs enabled. SE clocks with 8” traces. Differential clocks with 7” traces. Loading per CK505 spec.	–	25	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device operates reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R/T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-μs duration	–	500	ps
L_{ACC}	Long-term Accuracy	Measured at VDD/2 differential	–	250	ppm
Clock Input					
T_{DC}	CLKIN Duty Cycle	Measured at VDD/2	47	53	%
T_R/T_F	CLKIN Rise and Fall Times	Measured between $0.2V_{DD}$ and $0.8V_{DD}$	0.5	4.0	V/ns
T_{CCJ}	CLKIN Cycle to Cycle Jitter	Measured at VDD/2	–	250	ps
T_{LTJ}	CLKIN Long Term Jitter	Measured at VDD/2	–	350	ps
V_{IL}	Input Low Voltage	XIN / CLKIN pin	–	0.8	V
V_{IH}	Input High Voltage	XIN / CLKIN pin	2	VDD+0.3	V
I_{IL}	Input LowCurrent	XIN / CLKIN pin, 0 < VIN <0.8	–	20	uA
I_{IH}	Input HighCurrent	XIN / CLKIN pin, VIN = VDD	–	35	uA
CPU at 0.7V					
T_{DC}	CPUT and CPUC Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz CPUT and CPUC Period	Measured at 0V differential at 0.1s	9.99900	10.00100	ns
T_{PERIOD}	133 MHz CPUT and CPUC Period	Measured at 0V differential at 0.1s	7.49925	7.50075	ns
$T_{PERIODSS}$	100 MHz CPUT and CPUC Period, SSC	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
$T_{PERIODSS}$	133 MHz CPUT and CPUC Period, SSC	Measured at 0V differential at 0.1s	7.51804	7.51955	ns
$T_{PERIODAbs}$	100 MHz CPUT and CPUC Absolute period	Measured at 0V differential at 1 clock	9.91400	10.0860	ns
$T_{PERIODAbs}$	133 MHz CPUT and CPUC Absolute period	Measured at 0V differential at 1 clock	7.41425	7.58575	ns
$T_{PERIODSSAbs}$	100 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential at1 clock	9.914063	10.1362	ns
$T_{PERIODSSAbs}$	133 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential at1 clock	7.41430	7.62340	ns
T_{CCJ}	CPU Cycle to Cycle Jitter	Measured at 0V differential	–	85	ps
Skew	CPU0 to CPU1 skew	Measured at 0V differential	–	100	ps
L_{ACC}	Long-term Accuracy	Measured at 0V differential	–	100	ppm
T_R / T_F	CPU Rising/Falling Slew rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
SRC at 0.7V					
T_{DC}	SRC Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz SRC Period	Measured at 0V differential at 0.1s	9.99900	10.0010	ns
$T_{PERIODSS}$	100 MHz SRC Period, SSC	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
$T_{PERIODAbs}$	100 MHz SRC Absolute Period	Measured at 0V differential at 1 clock	9.87400	10.1260	ns
$T_{PERIODSSAbs}$	100 MHz SRC Absolute Period, SSC	Measured at 0V differential at 1 clock	9.87406	10.1762	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
$T_{SKEW(window)}$	Any SRC Clock Skew from the earliest bank to the latest bank	Measured at 0V differential	–	3.0	ns
T_{CCJ}	SRC Cycle to Cycle Jitter	Measured at 0V differential	–	125	ps
L_{ACC}	SRC Long Term Accuracy	Measured at 0V differential	–	100	ppm
T_R / T_F	SRC Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
DOT96 at 0.7V					
T_{DC}	DOT96 Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	DOT96 Period	Measured at 0V differential at 0.1s	10.4156	10.4177	ns
$T_{PERIODAbs}$	DOT96 Absolute Period	Measured at 0V differential at 0.1s	10.1656	10.6677	ns
T_{CCJ}	DOT96 Cycle to Cycle Jitter	Measured at 0V differential at 1 clock	–	250	ps
L_{ACC}	DOT96 Long Term Accuracy	Measured at 0V differential at 1 clock	–	100	ppm
T_R / T_F	DOT96 Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
USB_48 at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.83125	20.83542	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T_{HIGH}	48_M High time	Measurement at 2V	8.216563	11.15198	ns
T_{LOW}	48_M Low time	Measurement at 0.8V	7.816563	10.95198	ns
T_R / T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	2.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	350	ps
L_{ACC}	48M Long Term Accuracy	Measurement at 1.5V	–	100	ppm
27M_NSS/27_SS at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread 27M Period	Measurement at 1.5V	37.03594	37.03813	ns
	Spread Enabled 27M Period	Measurement at 1.5V	37.12986	37.13172	ns
T_R / T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	300	ps
L_{ACC}	27_M Long Term Accuracy	Measured at crossing point V_{OX}	–	50	ppm
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	Measurement at 1.5V	69.82033	69.86224	ns
$T_{PERIODAbs}$	REF Absolute Period	Measurement at 1.5V	68.83429	70.84826	ns
T_{HIGH}	REF High time	Measurement at 2V	29.97543	38.46654	ns
T_{LOW}	REF Low time	Measurement at 0.8V	29.57543	38.26654	ns
T_R / T_F	REF Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	REF Clock to REF Clock	Measurement at 1.5V	–	500	ps

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
L_{ACC}	Long Term Accuracy	Measurement at 1.5V	–	100	ppm
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns

Test and Measurement Set-up

For USB_48 and REF clocks

The following diagram shows the test load configurations for the single-ended USB_48 and REF output signals.

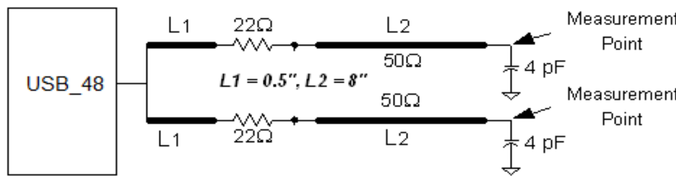


Figure 8. Single-ended USB_48 Clock Double Load Configuration

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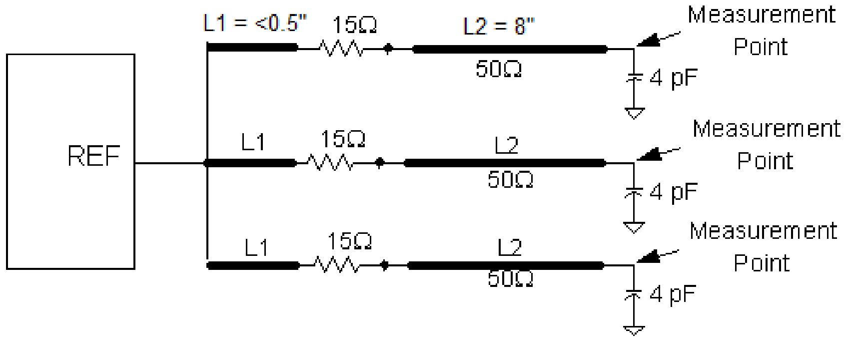


Figure 9. Single-ended REF Triple Load Configuration

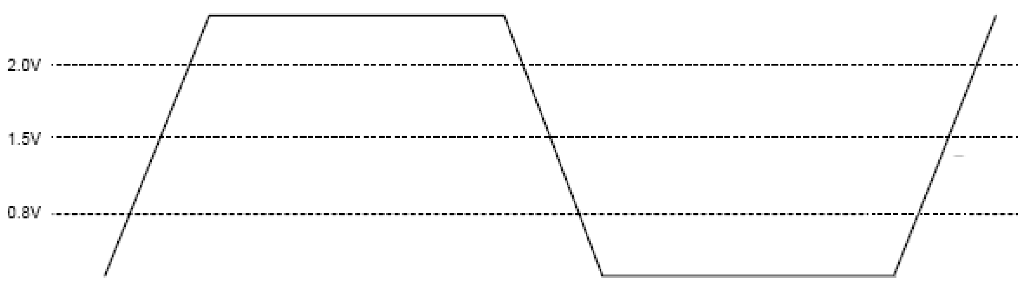


Figure 10. Single-ended Output Signals (for AC Parameters Measurement)

For Differential Clock Signals

This diagram shows the test load configuration for the differential clock signals

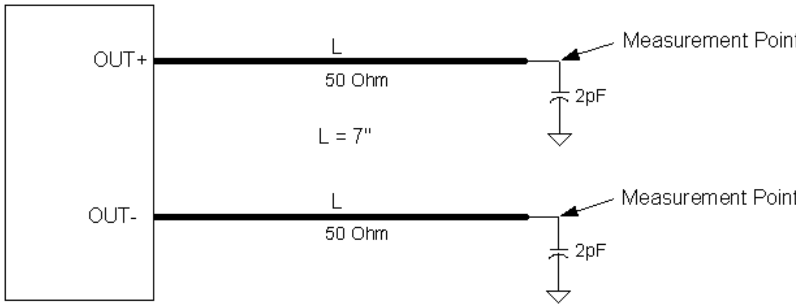


Figure 11. 0.7V Differential Load Configuration

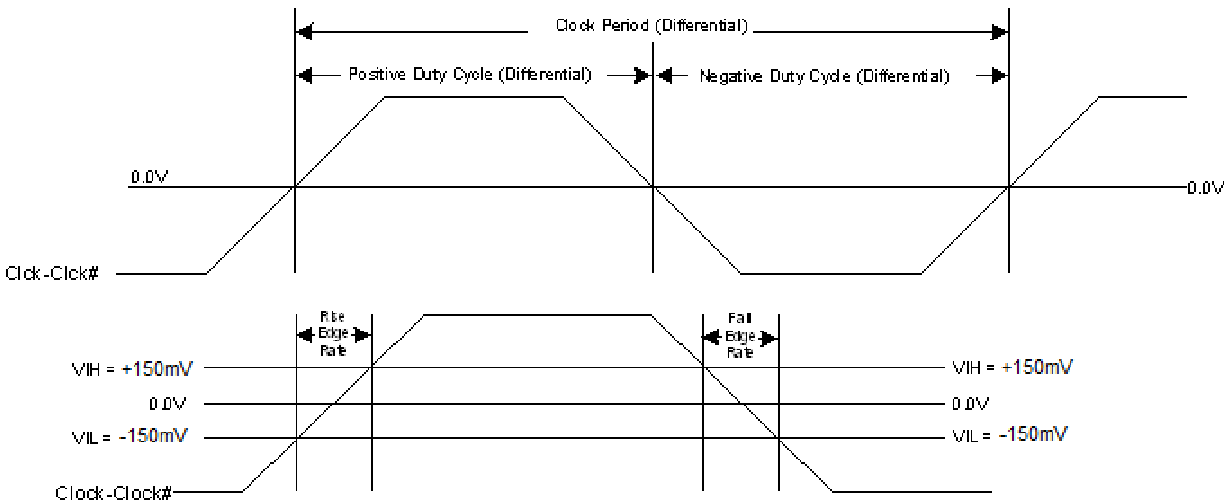


Figure 12. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

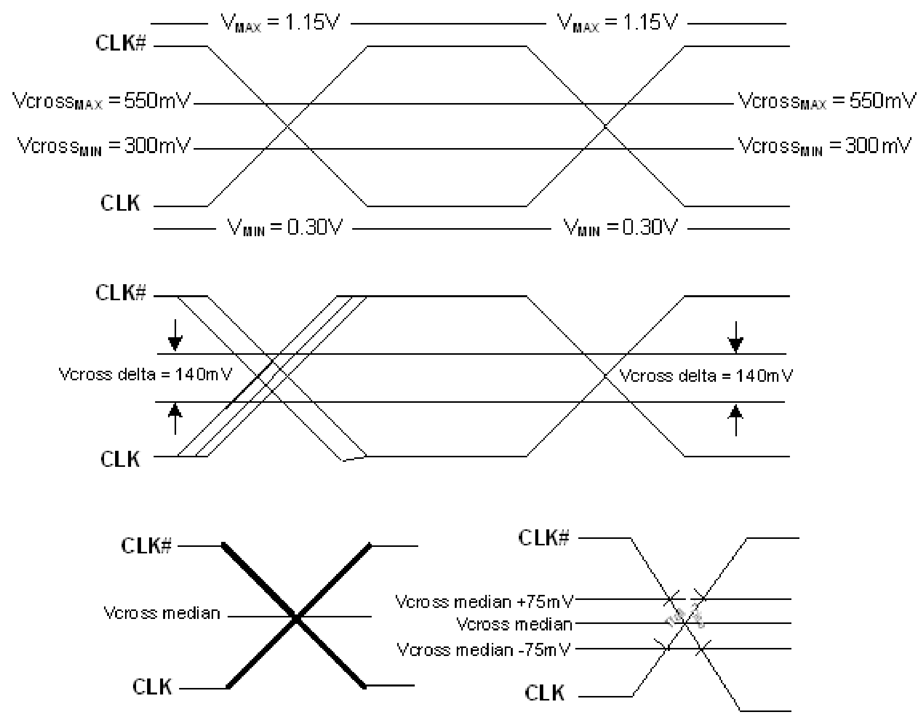
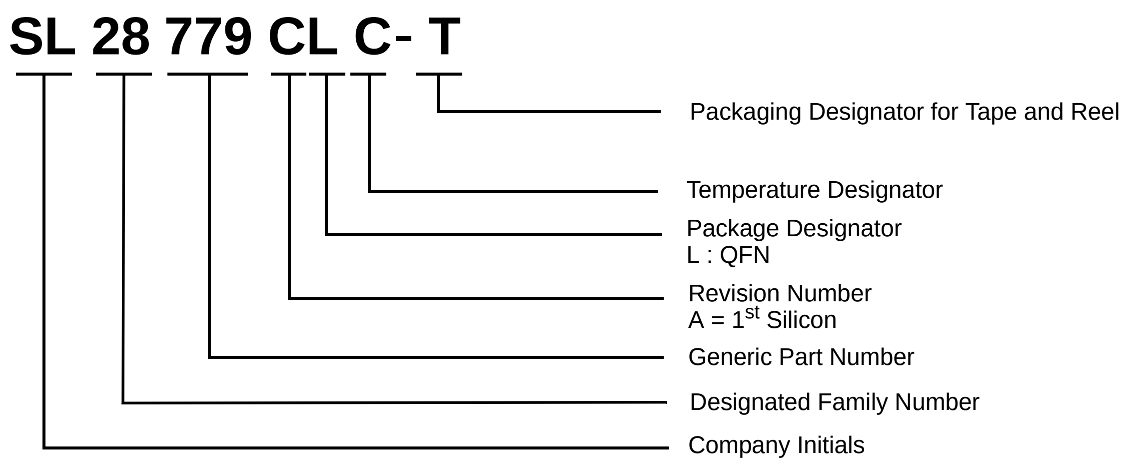


Figure 13. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

Ordering Information

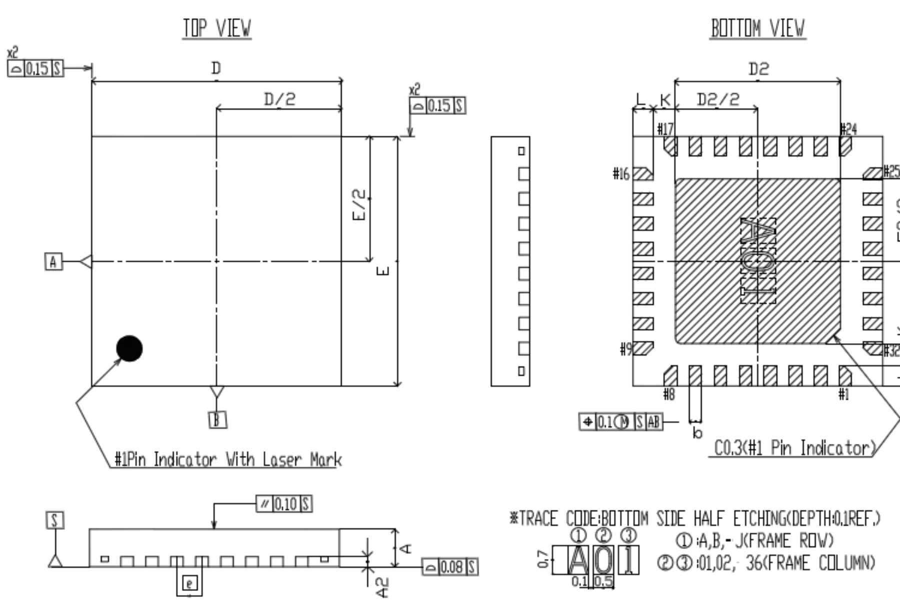
Part Number	Package Type	Product Flow
Lead-free		
SL28779CLC	32-pin QFN	Commercial, 0° to 85°C
SL28779CLCT	32-pin QFN–Tape and Reel	Commercial, 0° to 85°C



This device is Pb free and RoHS compliant.

Package Diagrams

32-Lead QFN 5x 5mm (Saw Version)



SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A2	0.20 REF.		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.15	3.30	3.45
E	4.90	5.00	5.10
E2	3.15	3.30	3.45
e	0.50 BSC.		
k	0.41	—	—
L	0.30	0.40	0.50

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
2. DIMENSIONAL TOLERANCE UNLESS OTHERWISE SPECIFIED +/- 0.10.
3. THE SURFACE OF THE PACKAGE SHALL BE RZ 4-8uM
4. PROTRUSIONS AT THE PKG. OUTLINE SHALL NOT EXCEED 0.10.

Document History Page

Document Title: SL28779 PC EProClock® Generator for Intel Calpella Chipset DOC#: SP-AP-0066 (Rev. AA)				
REV.	**ECR#**	**Issue Date**	**Orig. of Change**	**Description of Change**
1.0		10/9/08	JMA	Initial Release
1.1		10/23/08	JMA	1. Changed operating temperature to 0-85C 2. Re-aligned ordering part number description
1.2		1/27/09	JMA	1. Updated Rev. ID 2. Uddated definition of Byte 6 bit 5 and 3 3. Updated Byte 13 and single-ended slew rate table 4. Udated Byte 14 5. Updated Feature description 6. Added less than symbol in power consumption value 7. Updated ordering part number 8. Changed package information 9. Changed Wireless Friendly Mode to 111
1.3		3/16/09	JMA	1. Added PC EProClock® Programmed Technology in Feature section 2. Updated Block Diagram 3. Updated 27MHz slew rate measurement window 4. Updated power consumption
1.4		5/18/09	JMA	1. Updated Package information removed punch version with saw version 2. Updated TPeriod at 100MHz for CPU clocks 3. Updated Revision ID 4. Added Power down Spec 5. Added PC EProClock® Technology description 6. Added CPU Skew 7. Added 27M_OE# information 8. Removed CPU_STP# information
1.5		6/3/09	JMA	1. Update Revision ID 2. Removed 3-bit differential slew rate 3. Removed 0.1s from CPU duty cycle spec 4. Changed SATA PLL2 to PLL4 5. Updated IDD measurement condition
AA	1458	01/05/10	JMA	1. Added Note in package diagram 2. Updated text content 3. Added information on trace length in Figure 8 4. Removed CPU Driven Figures 5. Updated VDD_IO spec to 4.6Vmaximum value 6. Edited CK_PWRGD to CKPWRGD 7. Removed Preliminary word 8. Updated MIL-Std to JEDEC standard 9. Updated revision to be ISO compliant 10. Added CLKIN feature