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Multifunction Timer

Description

The monolithic integrated bipolar circuit U2102B is a MOSFET or IGBT control circuit which allows the realization of an extremely wide range of timer and

dimmer functions. The integrated current monitoring function additionally permits the power switch to be reliably protected without an additional fuse.

Features

- Integrated reverse phase control
- Two- or three-wire applications
- Mode selection:
 - Zero-voltage switch with static output
 - Two-stage reverse phase control with switch-off
 - Two-stage reverse phase control
- Current monitoring:
 - High-speed short-circuit monitoring with output
 - High-current monitoring with integrating buffer
- Integrated chip temperature monitoring

- Adjustable and retriggerable tracking time
- External window adjustment for sensor input
- Enable input for triggering

Applications

- Motion detectors
- Time-delay relays
- Dimmers
- Reverse phase controls
- Timers

Block Diagram

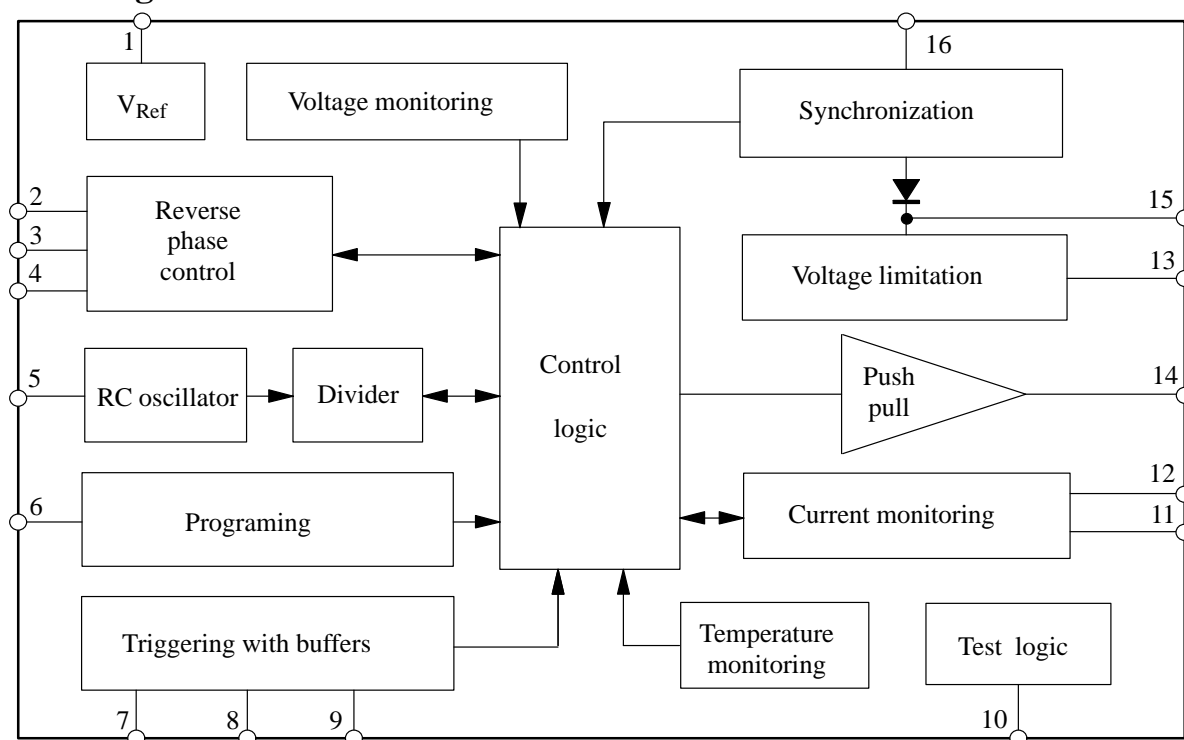
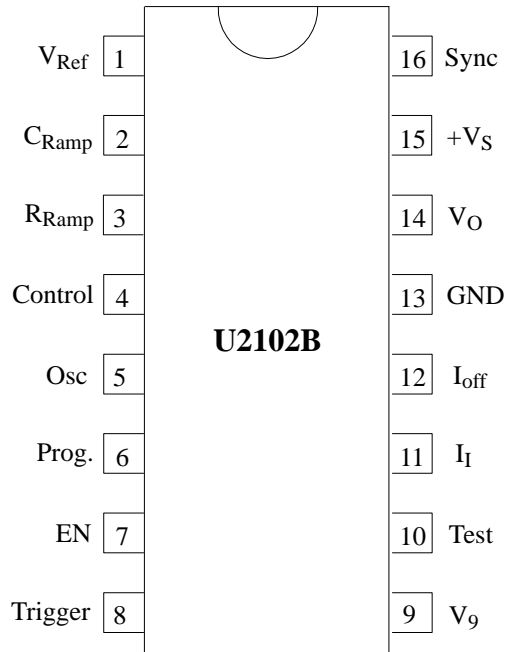


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U2102B-x	DIP16	Tube
U2102B-xFP	SO16	Tube
U2102B-xFPG3	SO16	Taped and reeled

Pin Description



Pin	Symbol	Function
1	V _{Ref}	Reference voltage 5 V
2	C _{Ramp}	Ramp, capacitance
3	R _{Ramp}	Current setting for ramp
4	Control	Control voltage
5	Osc	RC oscillator
6	Prog.	Tri-state programming
7	EN	Enable input
8	Trigger	Trigger input (window)
9	V ₉	Window adjustment
10	Test	Test output
11	I _I	Input current monitoring
12	I _{off}	Fast output current monitoring
13	GND	Ground
14	V _O	Output voltage
15	+V _S	Supply voltage
16	Sync	Synchronization input

Figure 2. Pinning

Power Supply, Synchronization Pins 15 and 16

The voltage limitation circuit contained in the U2102B enables simple power supply via a dropping resistor R_1 . In the case of dc loads, practically all the supply current flows into Pin 16 (the pull down resistor at Pin 16 is necessary in order to guarantee reliable synchronization) and is supplied via an internal diode to Pin 15, where the resultant supply voltage is limited and smoothed by C_1 . As a result, the rectified and divided line voltage appears at

Pin 16, where the amplitude is limited. The power supply for the circuit can be realized in all modes for dc loads as shown in figure 3. The voltage at Pin 16 is used to synchronize the circuit with the mains and generate the system clock required for the buffers. The circuit detects a “zero crossing” when the voltage at Pin 16 falls below an internal threshold of approximately 8 V.

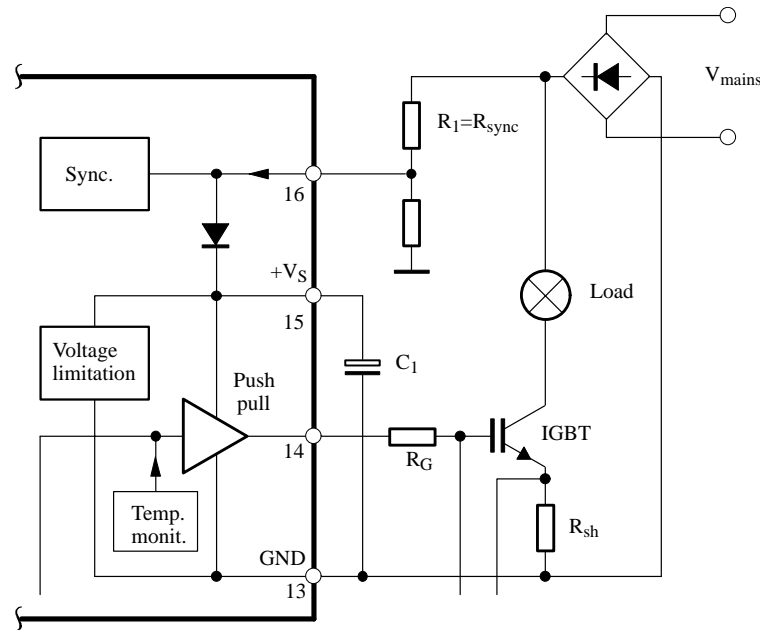


Figure 4. Power supply for dc loads (R_1 is identical with R_{sync})

R_1 is calculated here as follows:

$$R_{1max} = 0.85 \times \frac{V_{Nmin} - V_S}{I_{tot}} \quad (1)$$

where:

$$V_{Nmin} = V_{mains} - 15\%$$

$$V_S = \text{Supply voltage}$$

$$I_{tot} = I_{Smax} + I_x$$

$$I_{Smax} = \text{Max. current consumption of the IC}$$

$$I_x = \text{Current consumption of the external components}$$

In the case of ac loads, it is necessary to make a distinction for power supply purposes between the individual operating modes. In reverse phase control mode, figure 4, Pin 15 must be additionally supplied with power via a dropping resistor, since no current flows in Pin 16 when the power switch is switched on. Here, the dropping

resistor, R_1 , is connected before the rectifier bridge and therefore has only one mains half-wave. R_1 is then calculated as follows:

$$R_{1\max} = 0.85 \times \frac{V_{N\min} - V_S}{2 \times I_{\text{tot}}}$$

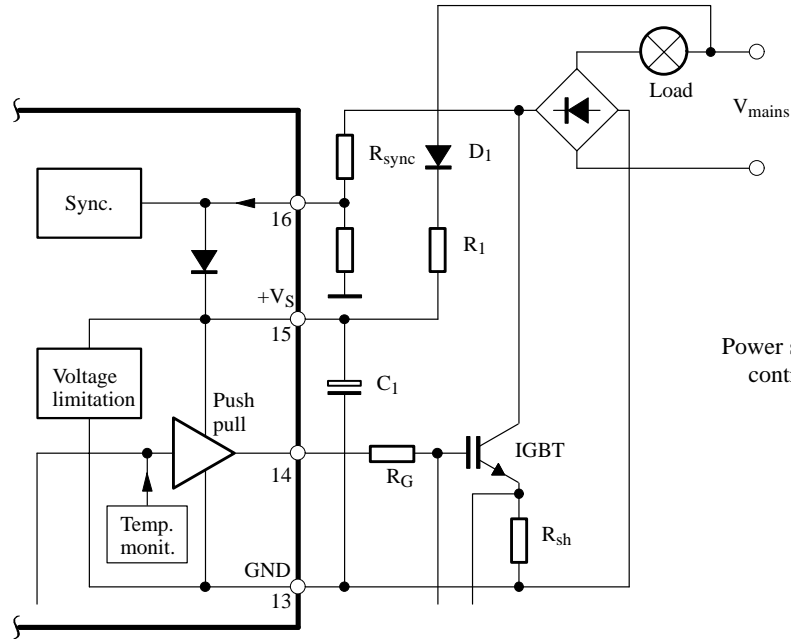


Figure 5.
Power supply in reverse phase control mode for ac loads

In two-wire systems, the additional power supply at Pin 15 is not possible (see figure 4, by omitting R_1 and Diode D_1). In this case, the resistor R_{sync} is identical with R_1 and should be as low as the power dissipation allows it. A sufficiently large residual phase angle must remain in this case in order to guarantee the device supply.

The power supply is simplified if the device is operated as a static zero-voltage switch for ac loads (see figure 5). All delay times are twice as long here, since synchronization of the module is tapped before the rectifier bridge.

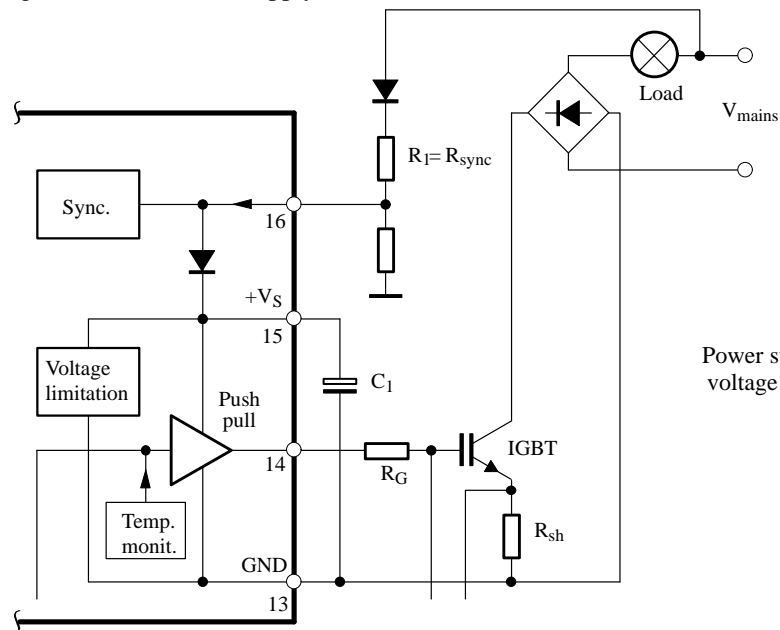


Figure 6.
Power supply as static zero voltage switch for ac loads

Voltage Monitoring

While the operating voltage is being built up or reduced, uncontrolled conditions or output pulses of insufficient amplitude are being suppressed by the internal monitoring circuit. All latches in the circuit, the divider and the control logic are reset. When the supply voltage is applied, the enable threshold (clamp voltage) of approximately 16 V must be reached so that the circuit is enabled. The circuit is reset at approximately 11 V if the supply voltage breaks down. A further threshold is activated in reverse phase control mode. If the supply voltage breaks down here after enabling of the circuit, the output stage is switched off at approximately 12.5 V, while the other parts of the circuit are not affected. The output stage can then be switched on again only in the following half-wave. As a result, the residual phase angle remains just large enough, (e.g., in two-wire systems), so that the circuit can still be properly supplied with power. In all operating modes, a single operating cycle is started after the supply voltage is applied, independently of the trigger inputs, in order to immediately demonstrate the overall function.

Chip Temperature Monitoring

The circuit possesses an integrated chip temperature monitoring circuit which disables the output stage when a temperature of approximately 140°C is reached. The circuit is enabled again only after cooling down and additionally switched “off and on” of the operating voltage.

Reverse Phase Control, Pins 2, 3, 4

In the case of normal phase controls, e.g., with a triac, the load current is switched ON only at a certain phase angle after the zero crossing of the mains voltage. In the following zero crossing of the current, the triac gets extinguished (switched-off) automatically. Reverse phase control differs from this in that the load current is always switched-on by a semiconductor switch (e.g., IGBT) at the zero crossing of the mains voltage and then switched back off again after a certain phase angle α . This has the advantage that the load current always rises with the mains voltage in a defined manner and thus keeps the required interference suppression to a minimum.

The charging current for the capacitor C_3 at Pin 2 is set with the resistor R_3 at Pin 3. When the synchronization circuit recognizes a zero crossing, an increased charging current $I_2 \approx 4 \times I_3$ is enabled which then charges C_3 up to ≈ 0.45 V. The output stage is switched-on at this value and the charging current for C_3 is reduced to $I_2 = I_3$. Since the actual zero crossing of the supply voltage occurs later than recognized by the circuit, the load current starts to flow quite close to the exact zero crossing of the supply voltage. While the output stage is switched-on C_3 is charged until the control voltage, set externally at Pin 4, is reached. When this condition is reached, the output stage is switched off and C_3 is charged again with the increased current ($I_2 = 4 \times I_3$) to $V_2 \approx 5.5$ V. The charging current is switched off at this point and C_3 is discharged internally. The whole process then starts again when the circuit recognizes another zero crossing (see figure 6).

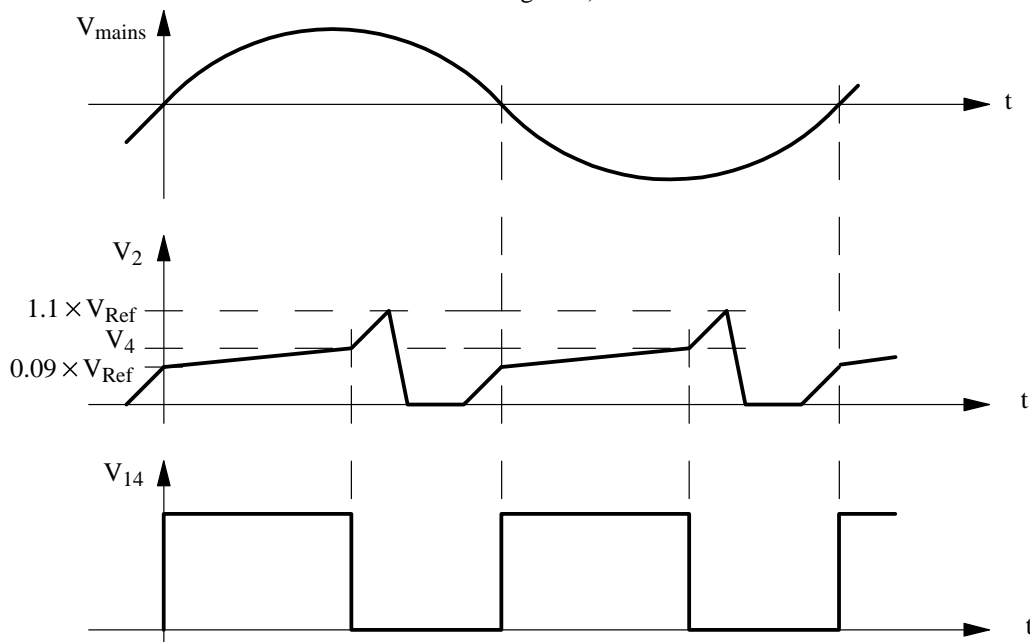


Figure 7. Signal characteristics of reverse phase control

Programming, Pin 6

Three operating modes can be programmed with the tristate input Pin 6:

- Zero-voltage switch (ZVS) with static output ($V_6 = V_1 = V_{Ref}$):

The reverse phase control is inactive here. The output stage is statically switched-on after triggering by the timer and switched-off again after the running down of the time (at the zero crossing of the supply voltage in each case). This operating mode is not possible in two-wire systems.

- Two-stage reverse phase control with switch-off ($V_6 = V_{15} = V_S$):

The maximum current flow angle, α_{max} , is set when the timer has enabled the output stage. Switchover to the phase angle α , which can be set arbitrarily at Pin 4, takes place after expiry of 3/4 of the tracking time set at Pin 5. The output stage switches off after expiry of the whole tracking time.

- Two-stage reverse phase control ($V_6 = V_{13} = GND$):

The output stage switches to the maximum current flow angle, α_{max} , (adjustable) if the trigger condition for both inputs (Pins 7, 8) is satisfied. Switchover to the current flow angle, α , set at Pin 4 takes place after expiry of 3/4 of the tracking time set at Pin 5. The whole process is repeated from the beginning again if renewed triggering takes place at Pin 8. The lamp is switched-off in the following half-wave of the mains voltage if the trigger condition at Pin 7 disappears. In this mode, the output stage is switched-on even if only Pin 7 is in the ON state. The current flow angle is then determined by V_4 (e.g., house no. illumination, twilight switch).

Trigger Inputs, Pins 7 and 8

The trigger condition of the timer is determined by the two inputs Pins 7 and 8. A Light Dependent Resistor (LDR) can be connected to Pin 7, for example, and an IR sensor to Pin 8. Both inputs must be in the ON state to initiate triggering, since they are equal and AND-gated. In the operating mode “2-stage reverse phase control”, the output stage can additionally be switched-on and switched-off by Pin 7 alone and independently of the timer.

The enable input Pin 7 is implemented as a comparator with hysteresis. The enable threshold is approximately 2.5 V. The blocking threshold is switched by the control logic in order to avoid faults as a result of load switching.

This threshold is approximately 2 V in switched-off condition and also during the second current flow angle, α , in two-stage reverse phase control mode. Otherwise, the blocking-or switch-off threshold is 0.5 V.

The input Pin 8 is designed as a window discriminator, its window is set at Pin 9. The minimum window of approximately 250 mV is set with $V_9 = V_{13}$, and the maximum window of approximately 1.25 V with $V_9 = V_1$. The window discriminator is in the OFF state when the voltage at Pin 8 lies within the window set at Pin 9.

If a resistor divider with an NTC resistor is connected to Pin 9, for example, it is possible to compensate for the temperature dependence of the IR sensor, i.e. the range is made independent of temperature.

Noise suppression for $t_{ON} = 40$ ms guarantees that there is no peak noise signals at the inputs which could trigger the circuit. Equally, renewed triggering is prevented for $t_{OFF} = 640$ ms after load switch-off in order to avoid any self interference.

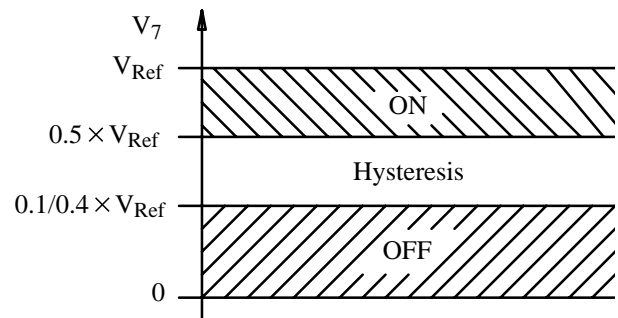


Figure 8. Trigger condition Pin 7

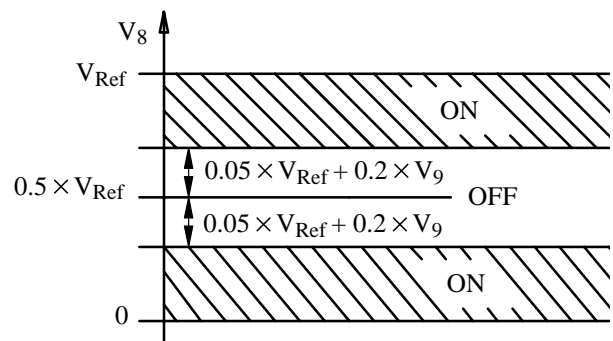


Figure 9. Trigger condition Pin 8

RC Oscillator, Pin 5

An internal RC oscillator with following divider stage 1:2¹¹ permits a very long and reproducible tracking time.

The RC values for a certain tracking time, t_t , are calculated as follows:

$$R_2 \text{ (k}\Omega\text{)} = \frac{t_t(\text{s}) \cdot 10^3}{1.4 \times 2048 \cdot C_2 \text{ (\mu F)}}$$

$$C_2 \text{ (\mu F)} = \frac{t_t(\text{s}) \cdot 10^3}{1.4 \times 2048 \cdot R_2 \text{ (k}\Omega\text{)}}$$

In reverse phase control mode, switchover from maximum current flow angle to the value set at Pin 4 takes place after expiry of 3/4 of the total tracking time t_t .

Current Monitoring, Pins 11 and 12

The current monitoring circuit integrated in the U2102B represents a double electronic fuse. The circuit measures the current flowing through the power switch by way of the voltage drop across the shunt resistor R_{sh} . This voltage is supplied to Pin 11. If this voltage exceeds a value of 500 mV because of a high load current (e.g., short-circuit), the switch-off latch is set and the switching output Pin 11 closes immediately. Pin 11 can be connected to the gate via a resistor or network, depending on load conditions, thus allowing the switch-off behavior to be adapted to the respective requirements. The short-circuit current is reduced to a problem-free value by this procedure.

There is a second threshold at 100 mV. The output stage is disabled if the voltage at Pin 11 exceeds this value and if it reaches this value for 120 ms in every half-wave without exceeding the switch-off threshold of 500 mV. Since high voltage peaks would be caused by switching off due to the line and leakage inductances, the output stage is not switched-off immediately but is simply not enabled in the next half-wave. The circuit is designed so that it also switches off in the case of changing over-currents which do not occur in every half-wave. But in this case the switch-off time is larger.

Absolute Maximum Ratings

Reference point Pin 13, unless otherwise specified

Parameters	Symbol	Value	Unit
Power supply Current $t < 10 \mu\text{s}$	Pin 15 I_S i_s	20 60	mA mA
Synchronization Input current $t \leq 10 \mu\text{s}$	Pin 16 I_I i_i	20 60	mA mA
Reference voltage source Output current	Pin 1 $-I_{Ref}$	10	mA
Push-pull output stage Output current $t \leq 2 \text{ms}$	Pin 14 $\pm I_O$ Pin 14 $\pm i_o$	10 60	mA mA
Input currents	Pin 2 $-I_I$ Pin 2 I_I Pin 3 $-I_I$ Pin 10 $\pm I_I$ Pin 12 I_I	1 8 0.2 1 20	mA mA mA mA mA
Input voltages	Pins 4, 5, 7, 8, 9 and 11 V_I Pins 6 and 12 V_I	0 to V_1 0 to V_{15}	V V
Storage temperature range	T_{stg}	- 40 to + 125	°C
Junction temperature	T_j	+ 125	°C
Ambient temperature	T_{amb}	- 10 to + 100	°C

Thermal Resistance

Parameters		Symbol	Value	Unit
Junction ambient	DIP 16	R_{thJA}	120	K/W
	SO 16 on PC board	R_{thJA}	180	K/W
	SO 16 on ceramic	R_{thJA}	100	K/W

Electrical Characteristics

$V_S = 15.0$ V, $f_{mains} = 50$ Hz, $T_{amb} = 25^\circ\text{C}$, reference point Pin 13, unless otherwise specified

Parameters	Test Conditions / Pin		Symbol	Min.	Typ.	Max.	Unit
Supply voltage limitation	$I_S = 2$ mA	Pin 15	V_S	15		17	V
	$I_S = 5$ mA		V_S	15.2		17.2	V
Current consumption	$V_S = 15$ V	Pin 15	I_S			2	mA
Voltage monitoring Pin 15							
Switch-on threshold			V_{SON}	14.8		16.5	V
Switch-off threshold			V_{SOFF}	10.4	11	11.6	V
Undervoltage threshold			V_{15}	11.7	12.5	13.3	V
Reference voltage	$-I_1 = 0$ to 5 mA	Pin 1	V_{Ref}	4.75	5	5.25	V
Synchronization							
Voltage limitation	$I_{16} = 2$ mA	Pin 16-15	V_{limit}		0.8		V
Input current	$V_{16} = 0$ V	Pin 16	$-I_1$		100		μA
Zero crossing switch-on threshold		Pin 16	V_{TON}	7.3	7.7	8.1	V
Zero crossing switch-off threshold		Pin 16	V_{TOFF}	7.9	8.3	8.7	V
Reverse phase control Pin 3							
Ramp current setting			$-I_1$			50	μA
Input current			V_3	4.7	5	5.3	V
Input voltage	$I_3 = -10$ μA						
Ramp	$I_3 = -10$ μA	Pin 2					
Charging current 1			$-I_{ch1}$	9	10	11	μA
Charging current 2			$-I_{ch2}$	37	40	43	μA
Discharge impedance			R_{dis}		1		k Ω
Switch-on threshold, output stage			V_{TON}	410	450	490	mV
Discharge threshold voltage		Pin 2-1	V_{dis}		600		mV
Control voltage Pin 4							
Input voltage			V_1	0		V_{Ref}	V
Input current	$V_{13} \leq V_4 \leq V_1$		$\pm I_1$			500	nA
Programming, tri state input Pin 6							
Input current	$V_{13} \leq V_6 \leq V_{15}$		$\pm I_1$			1	μA
Operating mode: Static zero-voltage switch			V_1	1		$V_{Ref}+0.3$	
2-stage reverse phase control with switch-off			V_1	$V_{Ref}+1$		V_S	V
2-stage reverse phase control			V_1	0		0.3	V
RC oscillator Pin 5							
Input current	$V_{13} \leq V_5 < 3.6$ V		$\pm I_1$			500	nA
Upper threshold			V_{TU}	3.6	4	4.4	V
Lower threshold			V_{TL}	0.9	1	1.1	V
Discharge impedance			R_{dis}		1		k Ω

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit	
Window discriminator							
Input current	$0\text{ V} \leq V_8 \leq V_1$ Pin 8	$\pm I_i$			500	nA	
Upper threshold	Pins 8 and 9	V_{TU}	$0.55 \cdot V_{Ref} + (0.2 \cdot V_9)$			V	
Lower threshold		V_{TL}	$0.45 \cdot V_{Ref} - (0.2 \cdot V_9)$			V	
Input current window adjustment	$0\text{ V} \leq V_9 \leq V_1$ Pin 9	$\pm I_i$			500	nA	
Minimum window:	$V_9 = V_{13}$ Pin 8	V_{TL1} V_{TU1}	2.05	2.75	2.45	V	
Lower threshold			2.55	3.75	2.95	V	
Upper threshold	$V_9 = V_1$ Pin 8	V_{TL2} V_{TU2}	1.1	1.25	1.4	V	
Lower threshold			3.4	3.75	4.1	V	
Upper threshold							
Enable Schmitt trigger Pin 7							
Input current	$0\text{ V} \leq V_7 \leq V_1$	$\pm I_i$			500	nA	
Enable threshold		V_T	2.3	2.5	2.7	V	
Blocking threshold:		V_T	1.8	2	2.2	V	
Output stage OFF			V_T	0.45	0.5	0.55	V
Output stage ON, except in the case of two-stage reverse phase control in second stage (α)							
Threshold for test mode		V_T	85	100	115	mV	
Current monitoring Pin 11							
Input current	$0\text{ V} \leq V_{11} \leq V_1$	$\pm I_i$			500	nA	
Switch-off threshold 1		V_{T1}	80	100	120	mV	
Switch-off threshold 2		V_{T2}	450	500	550	mV	
Switching output Pin 12							
Leakage current	$V_{11} < 450\text{ mV}, V_{12} \leq V_{15}$	I_{lkg}			1	μA	
Saturation voltage	$V_{11} > 550\text{ mV}$ $I_{12} = 0.5\text{ mA}$ $I_{12} = 10\text{ mA}$	V_{Sat} V_{Sat}			1.0	V	
					1.2	V	
Push-pull output stage							
Upper saturation voltage, ON state	$I_{14} = -10\text{ mA}$ Pins 14 and 15	$-V_{Sat}$			2.4	V	
Lower saturation voltage, OFF state	$I_{14} = 10\text{ mA}$ Pin 14	V_{SatL}			1.2	V	
Output current	ON state	$-I_O$	50			mA	
	OFF state	I_O	50			mA	

Applications

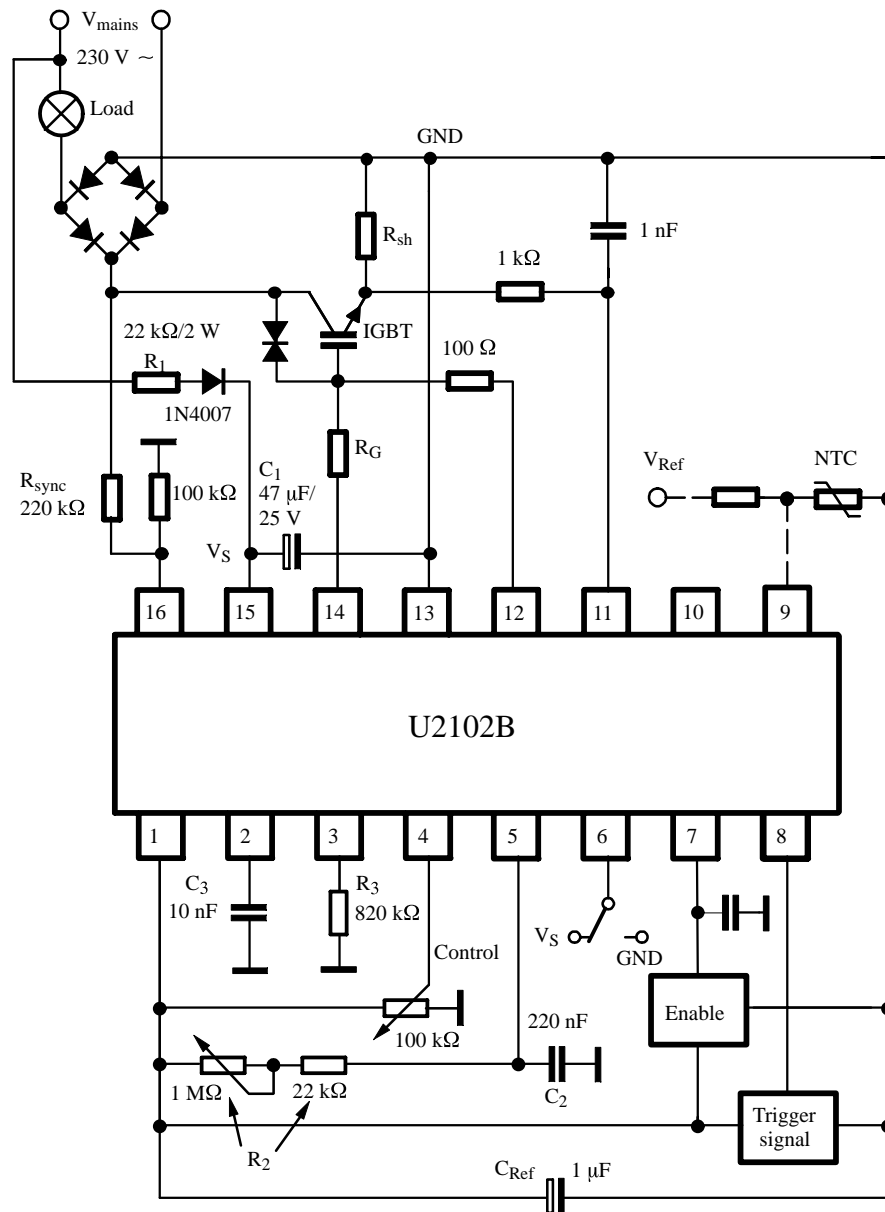


Figure 10. House number or staircase illumination for ac loads
 House number illumination: $V_6 = V_{13}$
 Staircase illumination: $V_6 = V_{15}$

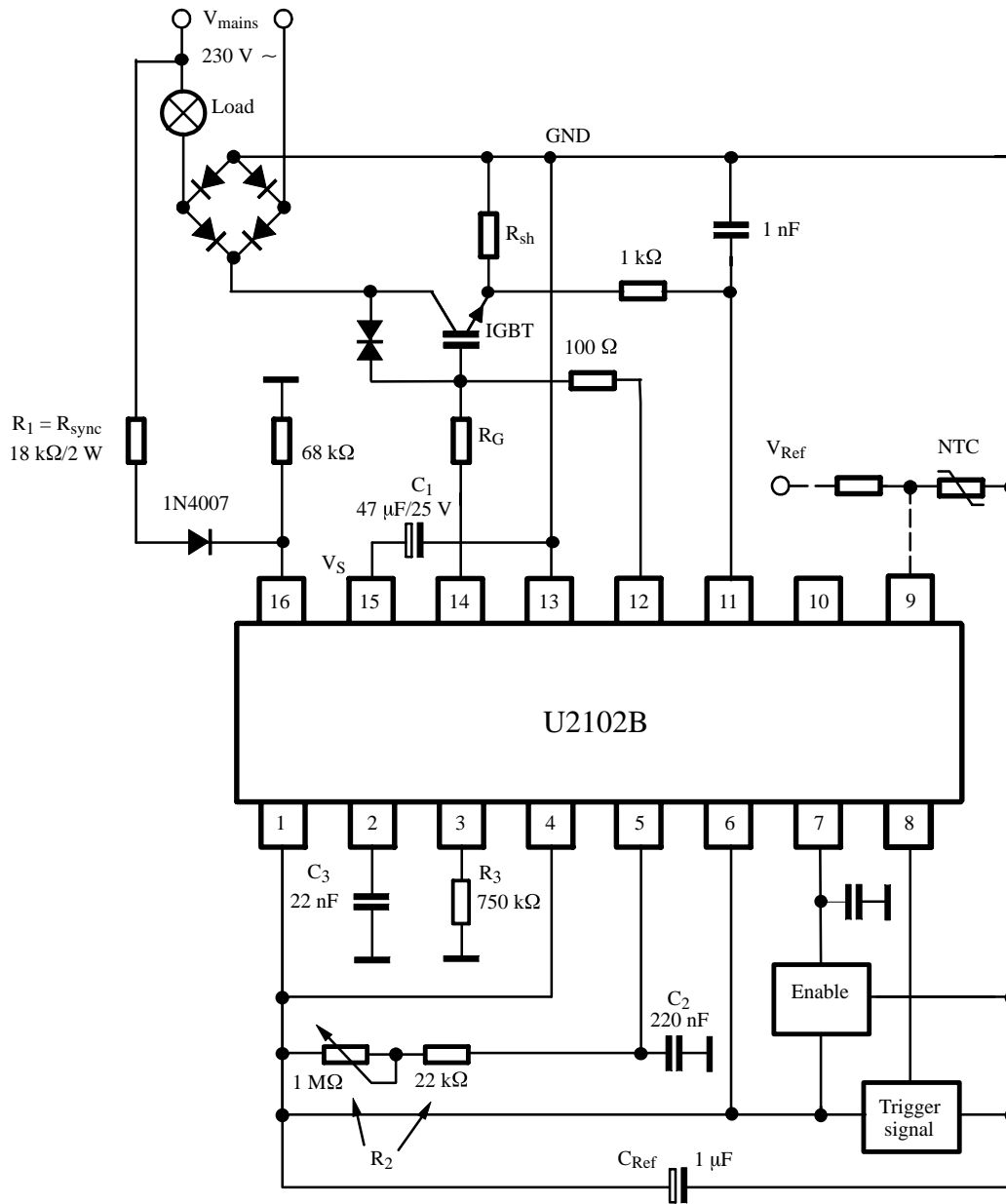


Figure 11. Zero voltage switch mode for ac loads

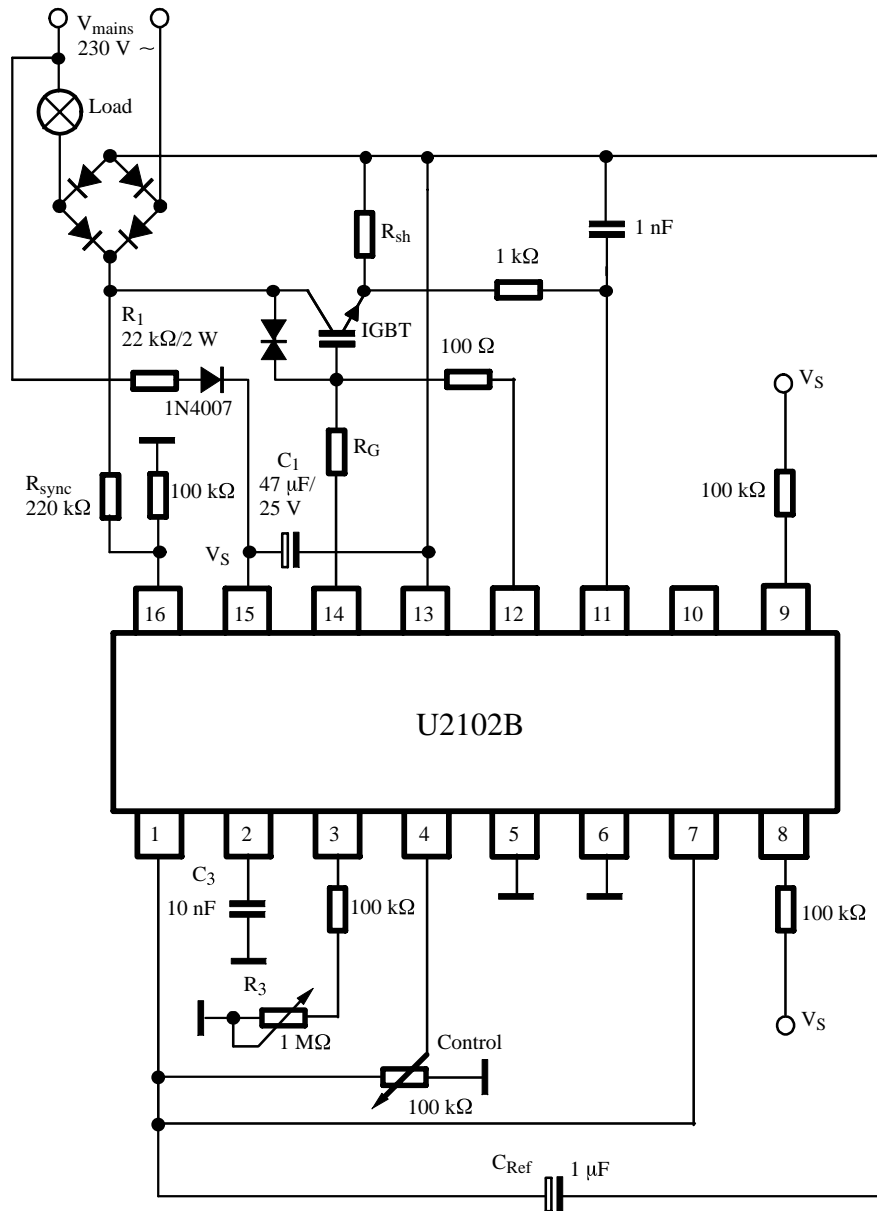
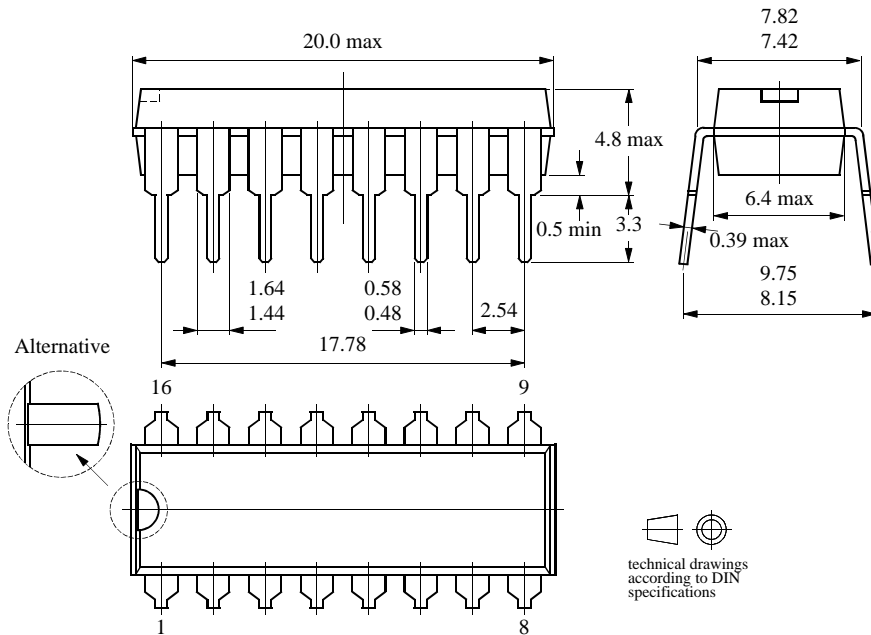


Figure 12. Reverse phase control for ac loads

Package Information

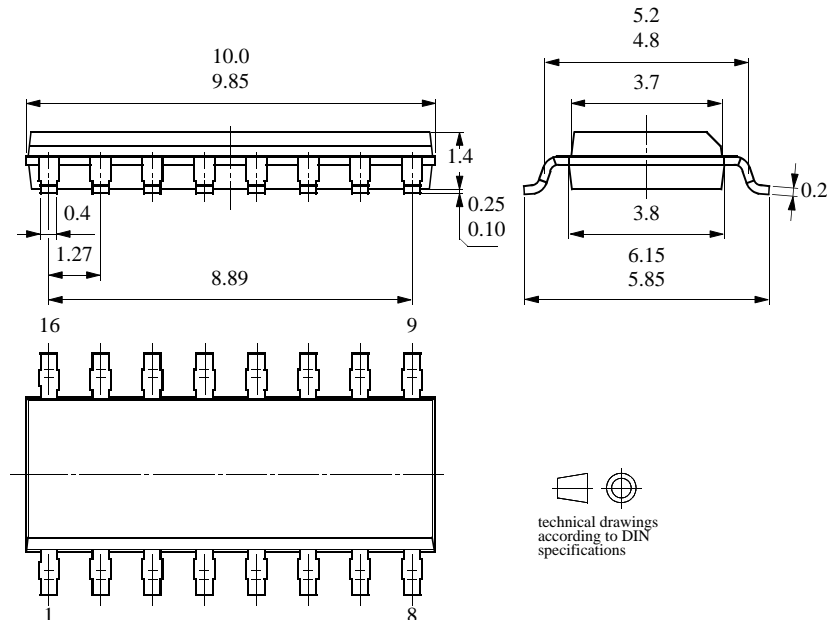
Package DIP16

Dimensions in mm



Package SO16

Dimensions in mm



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