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# Winbond Clock Generator
# W83195WG-416
# W83195CG-416
# For ATI K8 Chipset

Date: Feb/27/2006 Revision: 0.6

## W83195WG-416/W83195CG-416 Data Sheet Revision History

| | Pages | Dates | Version | Web Version | Main Contents |
|---|---|---|---|---|---|
| **1** | n.a. | 01/20/2006 | 0.5 | n.a. | All of the versions before 0.50 are for internal use. |
| **2** | 13 | 02/27/2006 | 0.6 | n.a. | Add HTT66 asynchronous mode. |
| **3** | | | | | |
| **4** | | | | | |
| **5** | | | | | |
| **6** | | | | | |
| **7** | | | | | |
| **8** | | | | | |
| **9** | | | | | |
| **10** | | | | | |



### LIFE SUPPORT APPLICATIONS

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# TABLE OF CONTENT

# W83195WG-416/W83195CG-416

STEPLESS FOR ATI K8 CLOCK GENERATOR

## 1. GENERAL DESCRIPTION

The W83195WG-416/W83195CG-416 is a Clock Synthesizer for ATI K8 serial chipsets. W83195WG-416/ W83195CG-416 provides all clocks required for the high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, PCI, and SRC clocks setting, all clocks are externally selectable with smooth transitions.

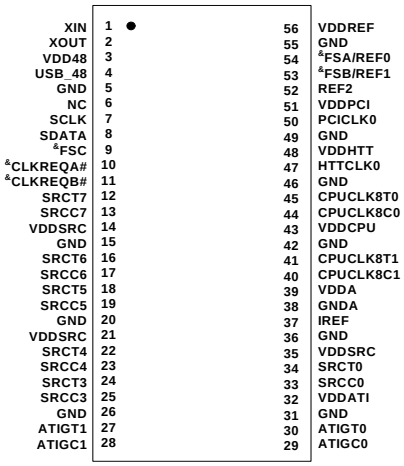
The W83195WG-416/W83195CG-416 provides $I^2C$ serial bus interface to program the registers to enable or disable each clock outputs and provides programmable S.S.T. scale to reduce EMI.

The W83195WG-416/W83195CG-416 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply.

## 2. PRODUCT FEATURES

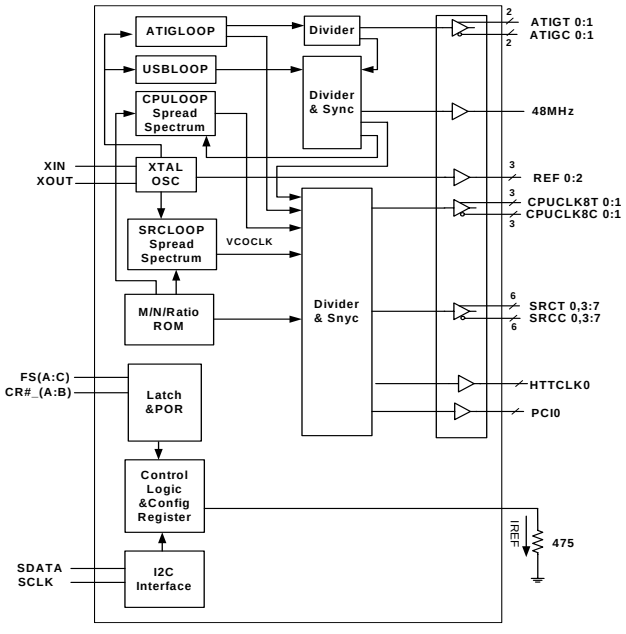
- 2 pair push-pull Differential clock outputs for CPU.
- 6 pair current-mode Differential clock outputs for SRC.
- 2 pair current-mode Differential clock outputs for ATIG programmable.
- 1 PCI clock output.
- 1 48 MHz clock output for USB.
- 3 14.318MHz REF clock outputs.
- 1 HTT 66MHz clock output.
- Smooth frequency switch with selections from 100 to 400MHz.
- Step-less frequency programming.
- $I^2C$ 2-wire serial interface and support byte read/write and block read/write.
- Programmable S.S.T. scale to reduce EMI in M/N mode.
- Programmable registers to enable/disable each output and select modes.
- Programmable clock outputs slew rate control and skew control.
- 56 pin TSSOP/SSOP package.

## 3. PIN CONFIGURATION




#: Active low
*: Internal pull up resistor 120K to VDD
&: Internal Pull-down resistor 120K to GND

## 4. BLOCK DIAGRAM



## 5. PIN DESCRIPTION

| PIN | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | XIN | IN | Crystal output at 14.318MHz nominally with internal loading capacitors (18pF). |
| 2 | XOUT | OUT | Crystal input with internal loading capacitors (18pF) and feedback resistors. |
| 3 | VDD48 | PWR | Power supply for USB_48 |
| 4 | USB_48 | OUT | 3.3V USB 48Mhz clock output. |
| 5 | GND | PWR | Ground pin |
| 6 | VTT_PG#/PD | IN | Notifies CK410 to sample latched input or power down mode |
| 7 | SCLK | IN | Serial clock of $I^2C$ 2-wire control interface. |
| 8 | SDATA | I/O | Serial data of $I^2C$ 2-wire control interface. |
| 9 | &FSC | IN | FSC CPU frequency select |
| 10 | &CLKREQA# | IN | Dynamic output control<br>0 = active, 1 = inactive |
| 11 | &CLKREQB# | IN | Dynamic output control<br>0 = active, 1 = inactive |
| 12 | SRCT7 | OUT | 0.7V current mode differential clock output for SRC |
| 13 | SRCC7 | OUT | 0.7V current mode differential clock output for SRC |
| 14 | VDDSRC | PWR | Power supply for SRC |
| 15 | GND | PWR | Ground pin |
| 16 | SRCT6 | OUT | 0.7V current mode differential clock output for SRC |
| 17 | SRCC6 | OUT | 0.7V current mode differential clock output for SRC |
| 18 | SRCT5 | OUT | 0.7V current mode differential clock output for SRC |
| 19 | SRCC5 | OUT | 0.7V current mode differential clock output for SRC |
| 20 | GND | PWR | Ground pin |
| 21 | VDDSRC | PWR | Power supply for SRC |
| 22 | SRCT4 | OUT | 0.7V current mode differential clock output for SRC |
| 23 | SRCC4 | OUT | 0.7V current mode differential clock output for SRC |
| 24 | SRCT3 | OUT | 0.7V current mode differential clock output for SRC |
| 25 | SRCC3 | OUT | 0.7V current mode differential clock output for SRC |
| 26 | GND | PWR | Ground pin |
| 27 | ATIGT1 | OUT | 0.7V current mode differential clock output for ATIG |
| 28 | ATIGC1 | OUT | 0.7V current mode differential clock output for ATIG |

| | | | |
|---|---|---|---|
| 29 | ATIGC0 | OUT | 0.7V current mode differential clock output for ATIG |
| 30 | ATIGT0 | OUT | 0.7V current mode differential clock output for ATIG |
| 31 | GND | PWR | Ground pin |
| 32 | VDDATIG | PWR | Power supply for ATIG |
| 33 | SRCC0 | OUT | 0.7V current mode differential clock output for SRC |
| 34 | SRCT0 | OUT | 0.7V current mode differential clock output for SRC |
| 35 | VDDSRC | PWR | Power supply for SRC |
| 36 | GND | PWR | Ground pin |
| 37 | IREF | OUT | Deciding the reference current for the differential pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current; 475 ohm is the standard value. |
| 38 | GNDA | PWR | Ground pin for PLL core. |
| 39 | VDDA | PWR | 3.3V power supply for PLL core. |
| 40 | CPUCLK8C1 | OUT | 3.3V Push Pull differential clock output for AMD K8 |
| 41 | CPUCLK8T1 | OUT | 3.3V Push Pull differential clock output for AMD K8 |
| 42 | GND | PWR | Ground pin |
| 43 | VDDCPU | PWR | Power supply for CPU |
| 44 | CPUCLK8C0 | OUT | 3.3V Push Pull differential clock output for AMD K8 |
| 45 | CPUCLK8T0 | OUT | 3.3V Push Pull differential clock output for AMD K8 |
| 46 | GND | PWR | Ground pin |
| 47 | HTTCLK0 | OUT | 3.3V HTT clock output. |
| 48 | VDDHTT | PWR | Power supply for HTTCLK |
| 49 | GND | PWR | Ground pin |
| 50 | PCICLK0 | OUT | 3.3V PCI clock output. |
| 51 | VDDPCI | PWR | Power supply for PCI |
| 52 | REF2 | OUT | 3.3V REF 14.318Mhz clock output. |
| 53 | &FSB/REF1 | I/O | FSB CPU frequency select/3.3V REF 14.318Mhz clock output. |
| 54 | &FSA/REF0 | I/O | FSA CPU frequency select/3.3V REF 14.318Mhz clock output. |
| 55 | GND | PWR | Ground pin |
| 56 | VDDREF | PWR | Power supply for REF |

## 6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [2:0] value or software programming at SSEL [4:0] (Register 0 bit 7 ~ 3). If FS [2:0] no any external circuit to modify power on status the Gray shading is Hardware default frequency.

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | CPU (MHZ) | SRC (MHZ) | PCI (MHZ) |
|---|---|---|---|---|---|---|---|
| FS4 | FS3 | FS2 | FS1 | FS0 | | | |
| 0 | 0 | 0 | 0 | 0 | 266.68 | 100.00 | 33.33 |
| 0 | 0 | 0 | 0 | 1 | 133.34 | 100.00 | 33.33 |
| 0 | 0 | 0 | 1 | 0 | 200.01 | 100.00 | 33.33 |
| 0 | 0 | 0 | 1 | 1 | 166.59 | 111.06 | 33.32 |
| 0 | 0 | 1 | 0 | 0 | 333.17 | 111.06 | 33.32 |
| 0 | 0 | 1 | 0 | 1 | 100.00 | 100.00 | 33.33 |
| 0 | 0 | 1 | 1 | 0 | 400.01 | 100.00 | 33.33 |
| 0 | 0 | 1 | 1 | 1 | 200.06 | 100.03 | 33.34 |
| 0 | 1 | 0 | 0 | 0 | 266.68 | 100.00 | 33.33 |
| 0 | 1 | 0 | 0 | 1 | 133.34 | 100.00 | 33.33 |
| 0 | 1 | 0 | 1 | 0 | 200.01 | 100.00 | 33.33 |
| 0 | 1 | 0 | 1 | 1 | 166.59 | 111.06 | 33.32 |
| 0 | 1 | 1 | 0 | 0 | 333.17 | 111.06 | 33.32 |
| 0 | 1 | 1 | 0 | 1 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 1 | 1 | 0 | 400.01 | 100.00 | 33.33 |
| 0 | 1 | 1 | 1 | 1 | 200.06 | 100.03 | 33.34 |
| 1 | 0 | 0 | 0 | 0 | 100.00 | 100.00 | 33.33 |
| 1 | 0 | 0 | 0 | 1 | 133.34 | 100.00 | 33.33 |
| 1 | 0 | 0 | 1 | 0 | 200.01 | 100.00 | 33.33 |
| 1 | 0 | 0 | 1 | 1 | 166.59 | 111.06 | 33.32 |
| 1 | 0 | 1 | 0 | 0 | 199.90 | 99.95 | 33.32 |
| 1 | 0 | 1 | 0 | 1 | 266.68 | 100.00 | 33.33 |
| 1 | 0 | 1 | 1 | 0 | 400.01 | 100.00 | 33.33 |
| 1 | 0 | 1 | 1 | 1 | 333.30 | 111.10 | 33.33 |
| 1 | 1 | 0 | 0 | 0 | 100.00 | 100.00 | 33.33 |
| 1 | 1 | 0 | 0 | 1 | 133.34 | 100.00 | 33.33 |
| 1 | 1 | 0 | 1 | 0 | 200.01 | 100.00 | 33.33 |
| 1 | 1 | 0 | 1 | 1 | 166.59 | 111.06 | 33.32 |
| 1 | 1 | 1 | 0 | 0 | 199.90 | 99.95 | 33.32 |
| 1 | 1 | 1 | 0 | 1 | 266.68 | 100.00 | 33.33 |
| 1 | 1 | 1 | 1 | 0 | 400.01 | 100.00 | 33.33 |
| 1 | 1 | 1 | 1 | 1 | 333.30 | 111.10 | 33.33 |

## 7. I²C CONTROL AND STATUS REGISTERS

**(The register No. is increased by 1 if use byte data read/write protocol)**

### 7.1 Register 0: ( Default : 00h )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | AFFECTED PIN / FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | SSEL<4> | 0 | Software frequency table selection through I²C | R/W |
| 6 | SSEL<3> | 0 | | |
| 5 | SSEL<2> | 0 | | |
| 4 | SSEL<1> | 0 | | |
| 3 | SSEL<0> | 0 | | |
| 2 | EN_SSEL | 0 | Enable software table selection FS[4:0].<br>0 = Hardware table setting (Jump mode).<br>1 = Software table setting through Bit7~3 .<br>(Jumpless mode) | R/W |
| 1 | SPSPEN | 0 | Enable spread spectrum mode under clock output.<br>0 = Spread Spectrum mode disable<br>1 = Spread Spectrum mode enable | R/W |
| 0 | EN_SAFE_FREQ | 0 | After watchdog timeout<br>0 = Reload the hardware FS [4:0] latched pins setting.<br>1 = Reload the desirable frequency table selection defined at Reg-5 Bit 4~0. | R/W |

### 7.2 Register 1: ( Default : XXh)

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | Reserved | 1 | Reserved | R/W |
| 6 | CPUEN<1> | 1 | CPUCLKT1/C1 output control<br>1: Enable<br>0: Disable | R/W |
| 5 | CPUEN<0> | 1 | CPUCLKT0/C0 output control<br>1: Enable<br>0: Disable | R/W |
| 4 | Reserved | X | Reserved | R |
| 3 | Reserved | X | Reserved | R |
| 2 | FS2_BACK | X | Power on latched value of FS2 pin. Default : **0** | R |
| 1 | FS1_BACK | X | Power on latched value of FS1 pin. Default : **0** | R |
| 0 | FS0_BACK | X | Power on latched value of FS0 pin. Default : **0** | R |

### 7.3 Register 2: ( Default : 03h )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | CLREQA7#_Ctr | 0 | SRCCLK7 is controlled by the CLREQA# pin<br>1: Controllable<br>0: Uncontrollable | R/W |
| 6 | CLREQA6#_Ctr | 0 | SRCCLK6 is controlled by the CLREQA# pin<br>1: Controllable<br>0: Uncontrollable | R/W |
| 5 | CLREQA5#_Ctr | 0 | SRCCLK5 is controlled by the CLREQA# pin<br>1: Controllable<br>0: Uncontrollable | R/W |
| 4 | CLREQA4#_Ctr | 0 | SRCCLK4 is controlled by the CLREQA# pin<br>1: Controllable<br>0: Uncontrollable | R/W |
| 3 | CLREQA3#_Ctr | 0 | SRCCLK3 is controlled by the CLREQA# pin<br>1: Controllable<br>0: Uncontrollable | R/W |
| 2 | CLREQA0#_Ctr | 0 | SRCCLK0 is controlled by the CLREQA# pin<br>1: Controllable<br>0: Uncontrollable | R/W |
| 1 | Reserved | 1 | Reserved | R/W |
| 0 | Reserved | 1 | Reserved | R/W |

### 7.4 Register 3: ( Default : 03h )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | CLREQB7#_Ctr | 0 | SRCCLK7 is controlled by the CLREQB# pin<br>1: Controllable<br>0: Uncontrollable | R/W |
| 6 | CLREQB6#_Ctr | 0 | SRCCLK6 is controlled by the CLREQB# pin<br>1: Controllable<br>0: Uncontrollable | R/W |
| 5 | CLREQB5#_Ctr | 0 | SRCCLK5 is controlled by the CLREQB# pin<br>1: Controllable<br>0: Uncontrollable | R/W |
| 4 | CLREQB4#_Ctr | 0 | SRCCLK4 is controlled by the CLREQB# pin<br>1: Controllable<br>0: Uncontrollable | R/W |
| 3 | CLREQB3#_Ctr | 0 | SRCCLK3 is controlled by the CLREQB# pin<br>1: Controllable<br>0: Uncontrollable | R/W |

| | | | | |
|---|---|---|---|---|
| 2 | CLREQB0#_Ctr | 0 | SRCCLK0 is controlled by the CLREQB# pin<br>1: Controllable<br>0: Uncontrollable | R/W |
| 1 | PCIEN | 1 | PCI0 output control<br>1: Enable<br>0: Disable | R/W |
| 0 | HTTEN | 1 | HTT66 output control<br>1: Enable<br>0: Disable | R/W |

### 7.5 Register 4: ( Default : FEh)

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | Reserved | 1 | Reserved | R/W |
| 6 | Reserved | 1 | Reserved | R/W |
| 5 | Reserved | 1 | Reserved | R/W |
| 4 | REFEN<2> | 1 | PREF2 output control<br>1: Enable<br>0: Disable | R/W |
| 3 | REFEN<1> | 1 | PREF1 output control<br>1: Enable<br>0: Disable | R/W |
| 2 | REFEN<0> | 1 | PREF0 output control<br>1: Enable<br>0: Disable | R/W |
| 1 | F48EN | 1 | PUSB48 output control<br>1: Enable<br>0: Disable | R/W |
| 0 | Reserved | 0 | Reserved | R/W |

### 7.6 Register 5: ( Default : 02h )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | Reserved | 0 | Reserved | R/W |
| 6 | CNT_EN | 0 | Program this bit =><br>1 : Enable Watchdog Timer feature.<br>0 : Disable Watchdog Timer feature.<br>**Enable WD sequence =>**<br>**Program this bit to 1 firstly, then program the Reg-20 to start the counting**<br>Read-back this bit => | R/W |

| | | | | |
|---|---|---|---|---|
| | | | During timer count down the bit read back to 1.<br>If count to zero, this bit read back to 0. | |
| 5 | WD_TIMEOUT | 0 | Read Back only. Timeout Flag.<br>1 : Watchdog has ever started and count to zero.<br>0 : a.) Watchdog is restarted and counting.<br>b.) Power on default state | R |
| 4 | SAF_FREQ<4> | 0 | These bits will be reloaded in Reg-0 to select frequency table. As the watchdog is timeout and EN_SAFE_FREQ=1. | R/W |
| 3 | SAF_FREQ<3> | 0 | | |
| 2 | SAF_FREQ<2> | 0 | | |
| 1 | SAF_FREQ<1> | 1 | | |
| 0 | SAF_FREQ<0> | 0 | | |

### 7.7 Register 6: ( Default : FFh )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | SRCEN<7> | 1 | SRC7 output control<br>1: Enable<br>0: Disable | R/W |
| 6 | SRCEN<6> | 1 | SRC6 output control<br>1: Enable<br>0: Disable | R/W |
| 5 | SRCEN<5> | 1 | SRC5 output control<br>1: Enable<br>0: Disable | R/W |
| 4 | SRCEN<4> | 1 | SRC4 output control<br>1: Enable<br>0: Disable | R/W |
| 3 | SRCEN<3> | 1 | SRC3 output control<br>1: Enable<br>0: Disable | R/W |
| 2 | ATIGEN<1> | 1 | ATIG1 output control<br>1: Enable<br>0: Disable<br>ATI clock can't be controlled by CLKREQ# pins | R/W |
| 1 | ATIGEN<0> | 1 | ATIG0 output control<br>1: Enable<br>0: Disable<br>ATI clock can't be controlled by CLKREQ# pins | R/W |
| 0 | SRCEN<0> | 1 | SRC0 output control<br>1: Enable<br>0: Disable | R/W |

### 7.8 Register 7: Winbond Chip ID – Project Code Register ( Default : 06h )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | CHIP_ID [7] | 0 | Winbond Chip ID.W83195CG/W-416 (BA5A06). | R |
| 6 | CHIP_ID [6] | 0 | Winbond Chip ID. | R |
| 5 | CHIP_ID [5] | 0 | Winbond Chip ID. | R |
| 4 | CHIP_ID [4] | 0 | Winbond Chip ID. | R |
| 3 | CHIP_ID [3] | 0 | Winbond Chip ID. | R |
| 2 | CHIP_ID [2] | 1 | Winbond Chip ID. | R |
| 1 | CHIP_ID [1] | 1 | Winbond Chip ID. | R |
| 0 | CHIP_ID [0] | 0 | Winbond Chip ID. | R |

### 7.9 Register 8: ( Default :D0h )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | NVAL<8> | 1 | Programmable N divisor value. Bit 7 ~0 are defined in the Register 9. | R/W |
| 6 | NVAL<9> | 1 | Programmable N divisor value. Bit 7 ~0 are defined in the Register 9. | R/W |
| 5 | MVAL<5> | 0 | Programmable M divisor | R/W |
| 4 | MVAL<4> | 1 | | |
| 3 | MVAL<3> | 0 | | |
| 2 | MVAL<2> | 0 | | |
| 1 | MVAL<1> | 0 | | |
| 0 | MVAL<0> | 0 | | |

### 7.10 Register 9: ( Default : 7Ah )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | NVAL<7> | 0 | Programmable N divisor bit 7 ~0. The bit 8,9 is defined in Register 8.<br>Default value follow FS=0 | R/W |
| 6 | NVAL<6> | 1 | | |
| 5 | NVAL<5> | 1 | | |
| 4 | NVAL<4> | 1 | | |
| 3 | NVAL<3> | 1 | | |
| 2 | NVAL<2> | 0 | | |
| 1 | NVAL<1> | 1 | | |
| 0 | NVAL<0> | 0 | | |

### 7.11 Register 10: Reserved ( Default : 3Bh )

### 7.12 Register 11: ( Default : 0Eh )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | SPH VAL<3> | 0 | Spread Spectrum Up Counter bit 3 ~ bit 0. | R/W |
| 6 | SPH VAL<2> | 0 | | |
| 5 | SPH VAL<1> | 0 | | |
| 4 | SPH VAL<0> | 0 | | |
| 3 | SPL VAL<3> | 1 | Spread Spectrum Down Counter bit 3 ~ bit 0<br>2's complement representation.<br>Ex: 1 -> 1111 ; 2 -> 1110 ; 7 -> 1001 ; 8 -> 1000 | |
| 2 | SPL VAL<2> | 1 | | |
| 1 | SPL VAL<1> | 1 | | |
| 0 | SPL VAL<0> | 0 | | |

### 7.13 Register 12: ( Default : XXh )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | Reserved | 0 | Reserved | R/W |
| 6 | KVAL<9> | X | Define the **PCI** divider ratio<br>Table-2 integrate the all divider configuration | R/W |
| 5 | KVAL<5> | X | | |
| 4 | KVAL<4> | X | Define the **SRC** divider ratio<br>Refer to Table-2 | R/W |
| 3 | KVAL<3> | X | | |
| 2 | KVAL<2> | X | Define the **CPU** divider ratio<br>Refer to Table-2 | R/W |
| 1 | KVAL<1> | X | | |
| 0 | KVAL<0> | X | | |

**Table-2 CPU, SRC, PCI divider ratio selection Table**

| LSB / MSB | | HTT/PCI | | SRC | | CPU | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | BIT5 | | BIT3 | | BIT1,0 | | | |
| | | 0 | 1 | 0 | 1 | 00 | 01 | 10 | 11 |
| Bit2/ Bit4/ Bit9 | 0 | **Reserved** | Div10 | **Reserved** | Div6 | Div2 | Div3 | Div4 | Div6 |
| | 1 | Div12 | Div15 | Div8 | Div10 | Div8 | Div8 | Div8 | Div8 |

### 7.14 Register 13: ( Default : 3Fh )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | EN_MN_PROG | 0 | 0: Output frequency depend on frequency table<br>1: Program all clock frequency by changing M/N value<br>The equation is<br>**VCO =14.318MHz*(N+4)/ M**.<br>Once the watchdog timer timeout, the bit will be clear. Then the frequency will be decided by hardware default FS<4:0> or desired frequency select SAF_FREQ[4:0] depend on EN_SAFE_FREQ (Reg0 – bit0). | |
| 6 | Reserved | 0 | Reserved | R/W |
| 5 | Reserved | 1 | Reserved | R/W |
| 4 | Reserved | 1 | | |
| 3 | IVAL<3> | 1 | Charge pump current selection | R/W |
| 2 | IVAL<2> | 1 | | |
| 1 | IVAL<1> | 1 | | |
| 0 | IVAL<0> | 1 | | |

### 7.15 Register 14: ( Default : D0h )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | Reserved | 1 | Reserved | R/W |
| 6 | Reserved | 1 | Reserved | R/W |
| 5 | SPCNT<5> | 0 | Spread Spectrum Programmable time, the resolution is 280ns. Default period is 11.8us | R/W |
| 4 | SPCNT<4> | 1 | | |
| 3 | SPCNT<3> | 0 | | |
| 2 | SPCNT<2> | 0 | | |
| 1 | SPCNT<1> | 0 | | |
| 0 | SPCNT<0> | 0 | | |

### 7.16 Register 15: ( Default : 5Ch )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | INV_CPU | 0 | Invert the CPUCLKT1/0 phase<br>0: Default<br>1: Inverse | R/W |
| 6 | Reserved | 1 | Reserved | R/W |

| | | | | |
|---|---|---|---|---|
| 5 | DRI_CONT | 0 | SRCT/ ATIG output state in during POWER DOWN assertion.<br>1: Driven (2*Iref)<br>0: Tristate (Floating)<br>SRCT/ ATIG output state in during STOP Mode assertion.<br>1: Driven (6*Iref)<br>0: Tristate (Floating)<br>Complementary parts always tri-state (floating) in power down or stop mode. | R/W |
| 4 | Reserved | 1 | Reserved | R/W |
| 3 | CPU2HTT_SYNC | 1 | CPU align with HTT<br>1 : Enable<br>0 : Disable | R/W |
| 2 | AZSKEW<2> | 1 | CPU1 to HTT66 skew control.<br>Skew resolution is 300ps<br>**The decision of skew direction is same as ASKEW<2:0> setting** | R/W |
| 1 | AZSKEW<1> | 0 | | |
| 0 | AZSKEW<0> | 0 | | |

### 7.17 Register 16: ( Default : 24h )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | INV_SRC | 0 | Invert the SRC phase<br>0: Default<br>1: Inverse | R/W |
| 6 | INV_PCI | 0 | Invert the HTT & PCI phase<br>0: Default<br>1: Inverse | R/W |
| 5 | CSKEW<2> | 1 | CPUCLKT1 to CPUCLKT0 skew control<br>Skew resolution is 300ps<br>**The decision of skew direction is same as CSKEW<2:0> setting** | R/W |
| 4 | CSKEW<1> | 0 | | |
| 3 | CSKEW<0> | 0 | | |
| 2 | PSKEW<2> | 1 | CPU1 to PCI skew control<br>Skew resolution is 300ps<br>**The decision of skew direction is same as PSKEW<2:0> setting** | R/W |
| 1 | PSKEW<1> | 0 | | |
| 0 | PSKEW<0> | 0 | | |

### 7.18 Register 17: Reserved ( Default : 07h )

### 7.19 Register 18: Reserved ( Default : 7Ah )

### 7.20 Register 19: ( Default : 04h )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | **SRC_FS<4>** | 0 | SRC frequency table. See Table-3.<br>**SRC_FS<4> also is spread spectrum enable bit.** | R/W |
| 6 | SRC_FS<3> | 0 | | R/W |
| 5 | SRC_FS<2> | 0 | | R/W |
| 4 | SRC_FS<1> | 0 | | |
| 3 | SRC_FS<0> | 0 | | |
| 2 | CENTERSKEW<2> | 1 | CPU1 center skew control<br>Skew resolution is 300ps<br>The decision of skew direction is same as CENTERSKEW<2:0> setting | R/W |
| 1 | CENTERSKEW<1> | 0 | | |
| 0 | CENTERSKEW<0> | 0 | | |

### 7.21 Register 20: ( Default : 88h )

| BIT | AFFECTED PIN/ FUNCTION NAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | Reserved | 1 | Reserved | R/W |
| 6 | SEC<6> | 0 | Setting the down count depth (Failure decision). One bit resolution represent 250ms. Default time depth is 8*250ms = 2.0 second. If the watchdog timer is counting, this register will return present down count value. | R/W |
| 5 | SEC<5> | 0 | | |
| 4 | SEC<4> | 0 | | |
| 3 | SEC<3> | 1 | | |
| 2 | SEC<2> | 0 | | |
| 1 | SEC<1> | 0 | | |
| 0 | SEC<0> | 0 | | |

### 7.22 Register 21: ( Default : ECh )

| BIT | AFFECTED PIN/ FUNCTIONNAME(S) | PWD | FUNCTION DESCRIPTION | TYPE |
|---|---|---|---|---|
| 7 | Reserved | 1 | Reserved | R/W |
| 6 | CPU2SRC_SYNC | 1 | CPU align with SRC<br>1 : Enable<br>0 : Disable | R/W |
| 5 | CPU2PCI_SYNC | 1 | CPU align with PCI<br>1 : Enable<br>0 : Disable | |
| 4 | Reserved | 0 | Reserved | R/W |
| 3 | Reserved | 1 | Reserved | R/W |

| | | | | |
|---|---|---|---|---|
| 2 | SRCSKEW<2> | 1 | CPU1 to SRC skew control<br>Skew resolution is 300ps<br>The decision of skew direction is same as SRCSKEW<2:0> setting | R/W |
| 1 | SRCSKEW<1> | 0 | | R/W |
| 0 | SRCSKEW<0> | 0 | | R/W |

**Table3: SRC & ATIG Frequency Selection Table**

| BIT 7 FS4 | BIT 6 FS3 | BIT 5 FS2 | BIT 4 FS1 | BIT 3 FS0 | SRC,ATIG (MHZ) | SPREAD(%) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 100.00 | 0 |
| 0 | 0 | 0 | 0 | 1 | 100.00 | 0 |
| 0 | 0 | 0 | 1 | 0 | 100.00 | 0 |
| 0 | 0 | 0 | 1 | 1 | 100.00 | 0 |
| 0 | 0 | 1 | 0 | 0 | 101.00 | 0 |
| 0 | 0 | 1 | 0 | 1 | 101.00 | 0 |
| 0 | 0 | 1 | 1 | 0 | 101.00 | 0 |
| 0 | 0 | 1 | 1 | 1 | 101.00 | 0 |
| 0 | 1 | 0 | 0 | 0 | 102.00 | 0 |
| 0 | 1 | 0 | 0 | 1 | 102.00 | 0 |
| 0 | 1 | 0 | 1 | 0 | 102.00 | 0 |
| 0 | 1 | 0 | 1 | 1 | 102.00 | 0 |
| 0 | 1 | 1 | 0 | 0 | 104.00 | 0 |
| 0 | 1 | 1 | 0 | 1 | 104.00 | 0 |
| 0 | 1 | 1 | 1 | 0 | 104.00 | 0 |
| 0 | 1 | 1 | 1 | 1 | 104.00 | 0 |
| 1 | 0 | 0 | 0 | 0 | 100.00 | -0.5 |
| 1 | 0 | 0 | 0 | 1 | 100.00 | -0.5 |
| 1 | 0 | 0 | 1 | 0 | 100.00 | -0.5 |
| 1 | 0 | 0 | 1 | 1 | 100.00 | -0.5 |
| 1 | 0 | 1 | 0 | 0 | 101.00 | -0.5 |
| 1 | 0 | 1 | 0 | 1 | 101.00 | -0.5 |
| 1 | 0 | 1 | 1 | 0 | 101.00 | -0.5 |
| 1 | 0 | 1 | 1 | 1 | 101.00 | -0.5 |
| 1 | 1 | 0 | 0 | 0 | 102.00 | -0.5 |
| 1 | 1 | 0 | 0 | 1 | 102.00 | -0.5 |
| 1 | 1 | 0 | 1 | 0 | 102.00 | -0.5 |
| 1 | 1 | 0 | 1 | 1 | 102.00 | -0.5 |
| 1 | 1 | 1 | 0 | 0 | 104.00 | -0.5 |
| 1 | 1 | 1 | 0 | 1 | 104.00 | -0.5 |
| 1 | 1 | 1 | 1 | 0 | 104.00 | -0.5 |
| 1 | 1 | 1 | 1 | 1 | 104.00 | -0.5 |

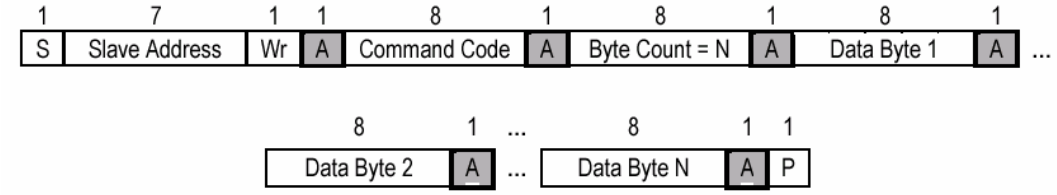
## 8. ACCESS INTERFACE

The W83195BR-416 provides $I^2C$ Serial Bus for microprocessor to read/write internal registers. In the W83195BR-416 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The $I^2C$ address is defined at 0xD2.

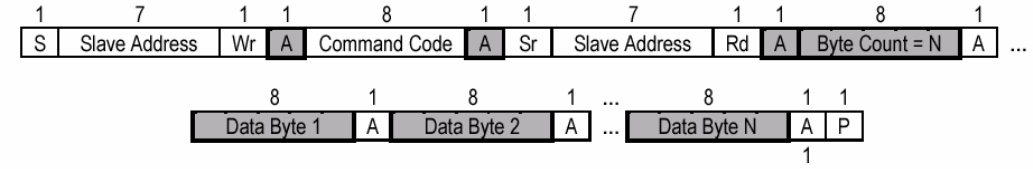
The register number is increased by one if using byte data read/write protocol.

**Example:** In block mode, byte number of program register is 1
In byte mode, byte number of program register is 2 (Byte number of block mode +1)

### 8.1 Block Write protocol

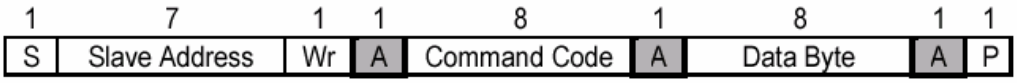



### 8.2 Block Read protocol

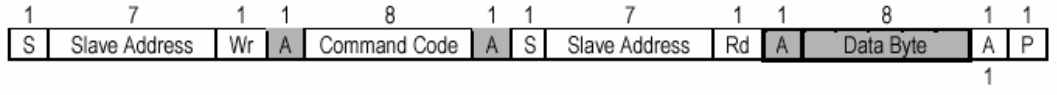



**## In block mode, the command code must filled 8'h00**

### 8.3 Byte Write protocol




### 8.4 Byte Read protocol



# 9. SPECIFICATIONS

## 9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

| PARAMETER | RATING |
|---|---|
| Absolute 3.3V Core Supply Voltage | -0.5V to +4.6V |
| Absolute 3.3V I/O Supple Voltage | - 0.5V to + 4.6V |
| Operating 3.3V Core Supply Voltage | 3.135V to 3.465V |
| Operating 3.3V I/O Supple Voltage | 3.135V to 3.465V |
| Storage Temperature | - 65°C to + 150°C |
| Ambient Temperature | - 55°C to + 125°C |
| Operating Temperature | 0°C to + 70°C |
| Input ESD protection (Human body model) | 2000V |

## 9.2 General Operating Characteristics

| ***VDD= 3.3V ±5 %, TA = 0℃ to +70℃,*** | | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Units** | **Test Conditions** |
| Input Low Voltage | $V_{IL}$ | | 0.8 | $V_{dc}$ | |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{dc}$ | |
| Output Low Voltage | $V_{OL}$ | | 0.4 | $V_{dc}$ | |
| Output High Voltage | $V_{OH}$ | 2.4 | | $V_{dc}$ | |
| Operating Supply Current | $I_{dd}$ | | 350 | mA | CPU = 100 to 400 MHz<br>PCI = 33.3 Mhz with load 10pF |
| Input pin capacitance | Cin | | 5 | pF | |
| Output pin capacitance | Cout | | 6 | pF | |
| Input pin inductance | Lin | | 7 | nH | |

## 9.3 Skew Group timing clock

| ***VDD = 3.3V ±5 %, TA = 0℃ to +70℃, Cl=10pF*** | | | | |
|---|---|---|---|---|
| **Parameter** | **Min** | **Max** | **Units** | **Test Conditions** |
| CPU pair to CPU pair Skew | | 100 | ps | Measure Crossing point |
| SRC pair to SRC pair Skew | | 125 | ps | Measure Crossing point |
| PCI to PCI Skew | | 250 | ps | Measured at 1.5V |
| 48MHz to 48MHz Skew | | 1000 | ps | Measured at 1.5V |

## 9.4 CPU 0.7V Electrical Characteristics

| ***VDDC= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF*** | | | | |
|---|---|---|---|---|
| **Parameter** | **Min** | **Max** | **Units** | **Test Conditions** |
| Rise Time | 175 | 700 | ps | Measure Single Ended waveform |
| Fall Time | 175 | 700 | ps | Measure Single Ended waveform |
| Absolute crossing point Voltages | 250 | 550 | mV | Measure Single Ended waveform |
| Voltage High | 660 | 850 | mV | Measure Single Ended waveform |
| Voltage Low | -150 | | mV | Measure Single Ended waveform |
| Cycle to Cycle jitter | | 100 | ps | Measure Differential waveform |
| Duty Cycle | 45 | 55 | % | Measure Differential waveform |

## 9.5 SRC 0.7V Electrical Characteristics

| ***VDDS= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF*** | | | | |
|---|---|---|---|---|
| **Parameter** | **Min** | **Max** | **Units** | **Test Conditions** |
| Rise Time | 175 | 700 | ps | Measure Single Ended waveform |
| Fall Time | 175 | 700 | ps | Measure Single Ended waveform |
| Absolute crossing point Voltages | 250 | 550 | mV | Measure Single Ended waveform |
| Voltage High | 660 | 850 | mV | Measure Single Ended waveform |
| Voltage Low | -150 | | mV | Measure Single Ended waveform |
| Cycle to Cycle jitter | | 100 | ps | Measure Differential waveform |
| Duty Cycle | 45 | 55 | % | Measure Differential waveform |

## 9.6 ATIG 0.7V Electrical Characteristics

| ***VDDPE= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF*** | | | | |
|---|---|---|---|---|
| **Parameter** | **Min** | **Max** | **Units** | **Test Conditions** |
| Rise Time | 175 | 700 | ps | Measure Single Ended waveform |
| Fall Time | 175 | 700 | ps | Measure Single Ended waveform |
| Absolute crossing point Voltages | 250 | 550 | mV | Measure Single Ended waveform |
| Voltage High | 660 | 850 | mV | Measure Single Ended waveform |
| Voltage Low | -150 | | mV | Measure Single Ended waveform |
| Cycle to Cycle jitter | | 100 | ps | Measure Differential waveform |
| Duty Cycle | 45 | 55 | % | Measure Differential waveform |

## 9.7 PCI Electrical Characteristics

| *VDDP= 3.3V ±5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,* | | | | |
|---|---|---|---|---|
| **Parameter** | **Min** | **Max** | **Units** | **Test Conditions** |
| Rise Time | 500 | 2000 | ps | Vol=0.4V, Voh=2.4V |
| Fall Time | 500 | 2000 | ps | Voh=2.4V, Vol=0.4V |
| Cycle to Cycle jitter | | 250 | ps | Measured at 1.5V |
| Duty Cycle | 45 | 55 | % | Measured at 1.5V |
| Pull-Up Current Min | -33 | | mA | Vout=1.0V |
| Pull-Up Current Max | | -33 | mA | Vout=3.135V |
| Pull-Down Current Min | 30 | | mA | Vout=1.95V |
| Pull-Down Current Max | | 38 | mA | Vout=0.4V |

## 9.8 USB Electrical Characteristics

| *VDD48= 3.3V ±5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,* | | | | |
|---|---|---|---|---|
| **Parameter** | **Min** | **Max** | **Units** | **Test Conditions** |
| Rise Time | 500 | 2000 | ps | Vol=0.4V, Voh=2.4V |
| Fall Time | 500 | 2000 | ps | Voh=2.4V, Vol=0.4V |
| Long term jitter | | 300 | ps | Measured at 1.5V |
| Duty Cycle | 45 | 55 | % | Measured at 1.5V |
| Pull-Up Current Min | -29 | | mA | Vout=1.0V |
| Pull-Up Current Max | | -23 | mA | Vout=3.135V |
| Pull-Down Current Min | 29 | | mA | Vout=1.95V |
| Pull-Down Current Max | | 27 | mA | Vout=0.4V |

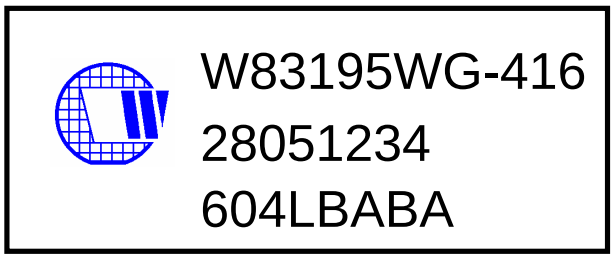
## 9.9 REF Electrical Characteristics

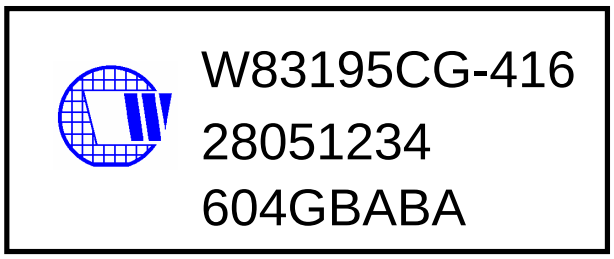
| *VDD= 3.3V ±5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,* | | | | |
|---|---|---|---|---|
| **Parameter** | **Min** | **Max** | **Units** | **Test Conditions** |
| Rise Time | 500 | 2000 | ps | Vol=0.4V, Voh=2.4V |
| Fall Time | 500 | 2000 | ps | Voh=2.4V, Vol=0.4V |
| Cycle to Cycle jitter | | 700 | ps | Measured at 1.5V |
| Duty Cycle | 45 | 55 | % | Measured at 1.5V |
| Pull-Up Current Min | -33 | | mA | Vout=1.0V |
| Pull-Up Current Max | | -33 | mA | Vout=3.135V |
| Pull-Down Current Min | 30 | | mA | Vout=1.95V |
| Pull-Down Current Max | | 38 | mA | Vout=0.4V |

## 10. ORDERING INFORMATION

| PART NUMBER | PACKAGE TYPE | PRODUCTION FLOW |
|---|---|---|
| W83195WG-416 | 56 PIN TSSOP | Commercial, 0°C to +70°C |
| W83195CG-416 | 56 PIN SSOP | Commercial, 0°C to +70°C |

## 11. HOW TO READ THE TOP MARKING




1st line: Winbond logo and the type number: W83195WG-416/W83195CG-416

2nd line: Tracking code 2 8051234

**2**: wafers manufactured in Winbond FAB 2

**8051234**: wafer production series lot number

3rd line: Tracking code 604 L B A BA

**604**: packages made in '2006, week 04

**L**: assembly house ID; O means OSE, G means GR, L means Lingsen.

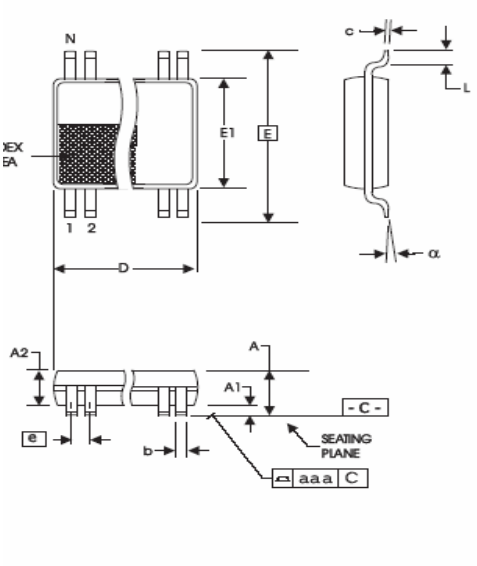
**B**: Internal use code

**A**: IC revision

**BA**: mask version

## 12. PACKAGE DRAWING AND DIMENSIONS

56 PIN TSSOP-240mil




**56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP**
**(240 mil) (20 mil)**

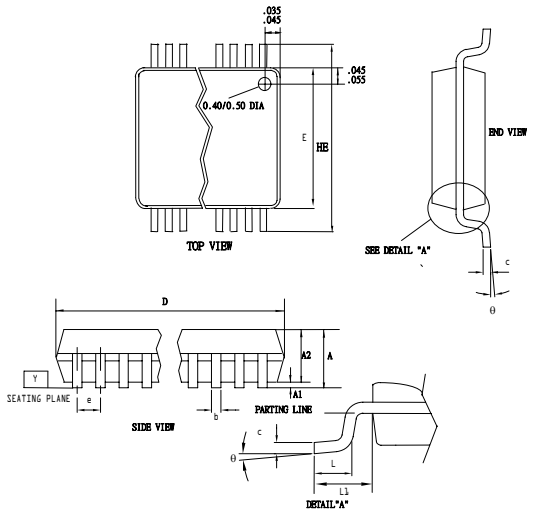
| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | – | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |
| aaa | – | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 56 | 13.90 | 14.10 | .547 | .555 |

Reference Doc.: JEDEC Publication 95, MO-153
10-0039

56 PIN SSOP-300mil




| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM | MAX. | MIN. | NOM | MAX. |
| A | 2.41 | 2.57 | 2.79 | 0.095 | 0.101 | 0.110 |
| A1 | 0.20 | 0.30 | 0.41 | 0.008 | 0.012 | 0.016 |
| A2 | 2.24 | 2.29 | 2.34 | 0.088 | 0.090 | 0.092 |
| b | 0.20 | 0.25 | 0.34 | 0.008 | 0.010 | 0.0135 |
| c | 0.13 | — | 0.25 | 0.005 | — | 0.010 |
| D | 18.2 | 18.42 | 18.54 | 0.720 | 0.725 | 0.730 |
| $H_E$ | 10.16 | 10.31 | 10.41 | 0.400 | 0.406 | 0.410 |
| E | 7.42 | 7.52 | 7.59 | 0.292 | 0.296 | 0.299 |
| e | 0.51 | 0.64 | 0.76 | 0.020 | 0.025 | 0.030 |
| L | 0.61 | 0.81 | 1.02 | 0.024 | 0.032 | 0.040 |
| L1 | — | 1.40 | — | — | 0.055 | — |
| Y | — | — | 0.08 | — | — | 0.003 |
| θ | 0 | — | 8 | 0 | — | 8 |

## Important Notice

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