阅读申明

1. 本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2. 本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3. 本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4. 如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有"数据手册"字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets".

Home > Products > Clock / Timing Devices > PC-Notebook-Server Clocks > Clock Synthesizer by Chipset Vendor > Desktop Chipsets > 953202 > 953202BGT

Add to myIDT [?]

You may also like...

953202BGT

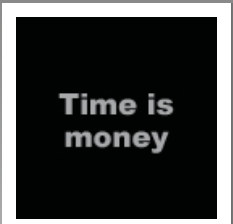|	
Category:	Desktop Chipsets
Generic Part:	953202
Market Group:	PC CLOCK
Description:	PC MAIN CLOCK

The ICS953202 is part of a whole new line of ICS clock generators and buffers called TCHâ„¢ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Output Features:
- 2 - Differential pair push-pull CPU clocks @ 3.3V
- 6 - PCI-Ex differential pairs
- 7 - PCICLK @ 3.3V
- 3 - AGPCLK @ 3.3V
- 1 - 48MHz @ 3.3V fixed.
- 1 - 24/48MHz @ 3.3V
- 2 - REF @ 3.3V, 14.318MHz.

Parameters

Package	TSSOP 56 (PA56)
Voltage	3.3 V
Package	TSSOP 56
Speed	NA
Temperature	C
Status	Active
Sample	No
Minimum Order Quantity	2000
Factory Order Increment	2000

Distributor Inventory

No Pricing information is available from our Distributors at this time.

Documents

Type	Title	Size	Revision Date
Misc	PC Clocks Contact Info	61 KB	05/29/2007

Package

Description	TSSOP 6.10 MM
Class	PLASTIC
Moisture Sensitivity Level (MSL)	1
Category	Standard
Moisture Exposure Floor Life	Unlimited @ <30°C/85% RH
Peak Reflow Temprature	240°C
Rebake Conditions	N/A
Length	14.0
Mark	G
Width	6.1
Pitch	0.5
Thickness	1.0
Status	Active