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DIFFERENTIAL SPREAD SPECTRUM CLOCK DRIVER MK1493-05

Description

The MK1493-05 is a spread-spectrum clock generator used as a companion chip with a CK410 system clock. The device is used in a PC or embedded system to substantially reduce electro-magnetic interference (EMI). The device provides a differential spread-spectrum high frequency output and a reference output clock. An SMBus is connected to the CK410 for command and control of the MK1493-05. The input reference clock to the MK1493-05 comes directly from the CK410. No external, expensive crystal or crystal oscillator is required.

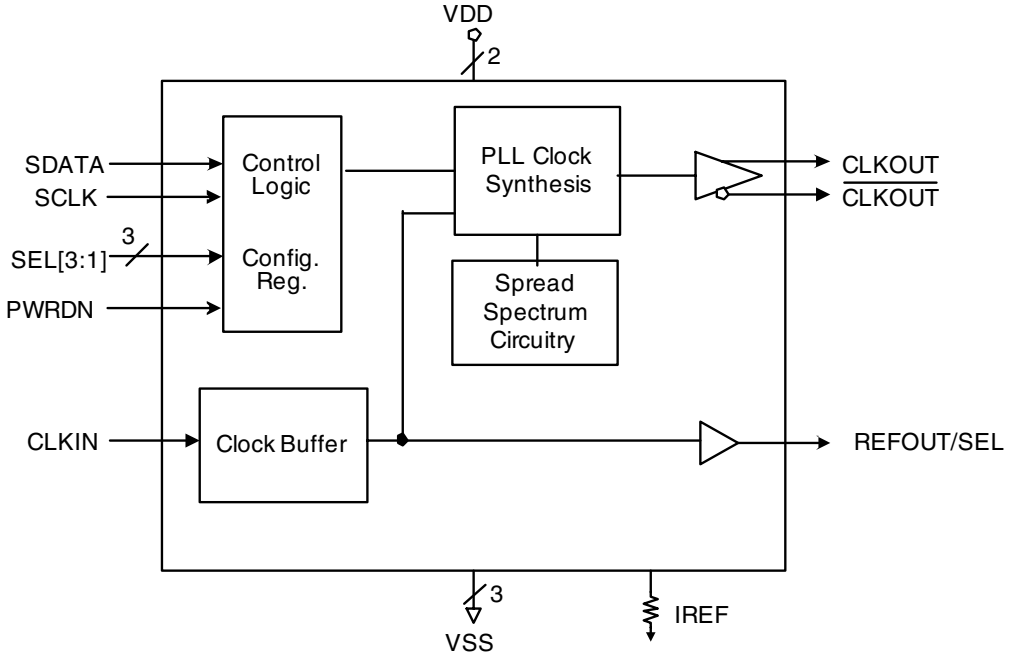
A 16-pin TSSOP package is employed to maximize board space utilization.

Features

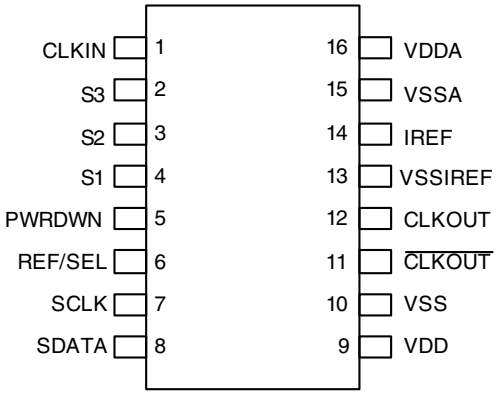
- Packaged in 16-pin TSSOP package
- Available in Pb (lead) free package
- Single differential spread spectrum clock
- Spread spectrum for EMI control
- Supports SMBUS index read/write and blocks read/write operations
- Uses external 14.31818 MHz clock from CK410
- Low output jitter design
- Power down mode lowers Idd
- Spread selection via hardware pins (down and center)
- Industrial temperature range available (-40°C to +85°C)

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



Pin Assignment



16 Pin 173 Mil (0.65mm) TSSOP

Spread Spectrum Selection Table

S3	S2	S1	S0	Spread%	Spread Type
0	0	0	0	0.8	Down
0	0	0	1	1.0	Down
0	0	1	0	1.25	Down
0	0	1	1	1.5	Down
0	1	0	0	1.75	Down
0	1	0	1	2.0	Down
0	1	1	0	2.5	Down
0	1	1	1	3.0	Down
1	0	0	0	±0.3	Center
1	0	0	1	±0.4	Center
1	0	1	0	±0.5	Center
1	0	1	1	±0.6	Center
1	1	0	0	±0.8	Center
1	1	0	1	±1.0	Center
1	1	1	0	±1.25	Center
1	1	1	1	±1.5	Center

The spread enable and spread select[3:0] SMBus register bits control spread modulation and enable/disable. The CLKIN clock input and REF clock output will not have or be spread. At device power-up the spread-spectrum is enabled and hardware control is enabled. The S0 configuration bit is hard-coded to zero when hardware control mode is selected.

Pin Descriptions

Pin	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	14.31818 MHz single-ended clock input.
2	S3	Input	Spread spectrum select pin #3. See table above. Internal pull-down.
3	S2	Input	Spread spectrum select pin #2. See table above. Internal pull-down.
4	S1	Input	Spread spectrum select pin #1. See table above. Internal pull-down.
5	PWRDN	Input	Power down pin. Active high. Internal pull-down.
6	REF/SEL	I/O	Strap input for selecting CLKOUT frequency and 14.31818 MHz reference clock.
7	SCLK	Input	SMBus compatible clock.
8	SDATA	I/O	SMBus compatible data.
9	VDD	Power	+3.3 V power supply for logic and outputs.
10	VSS	Power	Ground for logic and outputs.
11	$\overline{\text{CLKOUT}}$	Output	Selectable 96/100 MHz spread spectrum differential clock output.
12	CLKOUT	Output	Selectable 96/100 MHz spread spectrum differential clock output.
13	VSSIREF	Power	Ground for current reference.
14	IREF	Input	Precision resistor attached to this pin is connected to the internal current reference.
15	VSSA	Power	Ground for PLL.
16	VDDA	Power	+3.3 V power supply for PLL.

General SMBus Serial Interface

How to Write:

- Controller (host) sends a start bit
- Controller (host) sends the write address $D4_{(H)}$
- IDT clock will *acknowledge*
- Controller (host) sends the beginning byte location =N
- IDT clock will *acknowledge*
- Controller (host) sends the data byte count = X
- IDT clock will *acknowledge*
- Controller (host) starts sending *Byte N through Byte N + X - 1* (see Note 2)
- IDT clock will *acknowledge* each byte *one at a time*
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) sends a start bit
- Controller (host) sends the write address $D4_{(H)}$
- IDT clock will *acknowledge*
- Controller (host) sends the beginning byte location =N
- IDT clock will *acknowledge*
- Controller (host) will send a separate start bit
- Controller (host) sends the read address $D5_{(H)}$
- IDT clock will *acknowledge*
- Controller (host) sends the data byte count = X
- IDT clock sends *Byte N + X - 1*
- IDT clock sends *Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)*
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			IDT (Slave/Receiver)
T	starTbit		
Slave Address $D4_{H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte = N		.	
			ACK
O			
O		X	O
O		B	O
		Y	O
Byte N + X - 1		T	
		E	ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			IDT (Slave/Receiver)
T	starTbit		
Slave Address $D4_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D5_{(H)}$			
RD	ReaD		
			ACK
			Data Bye Count = X
ACK			
		.	Beginning Byte N
ACK			
		X	O
O		B	O
O		Y	O
O		T	
		E	Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Address

The MK1493-05 is a slave-only device that supports block read and block write protocol using a single 7 bit address and read/write bit. A block write (D4h) or block read (D5h) is made up of seven (7) bits and one (1) read/write bit.

A6	A5	A4	A3	A2	A1	A0	R/W#
1	1	0	1	0	1	0	X

The applications where the indexed block write and block are used, the dummy byte (bit 11-18) functions as a register-offset (8 bits) pointer.

Byte 0: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Spread Select 0	RW	0	CLKOUT, $\overline{\text{CLKOUT}}$	1,2,3
6	Spread Select 1	RW	S1	CLKOUT, $\overline{\text{CLKOUT}}$	1,2,3
5	Spread Select 2	RW	S2	CLKOUT, $\overline{\text{CLKOUT}}$	1,2,3
4	Spread Select 3	RW	S3	CLKOUT, $\overline{\text{CLKOUT}}$	1,2,3
3	Select Output Frequency, 1=100 MHz, 0=96 MHz	RW	SEL 100/$\overline{96}$	CLKOUT, $\overline{\text{CLKOUT}}$	1,2
2	Reserved, must be written as 0	RW	0	Not applicable	1
1	Spread spectrum enable, 0=spread OFF, 1=spread ON	RW	1=spread ON	CLKOUT, $\overline{\text{CLKOUT}}$	1
0	Hardware/Software control of spread enable, S[3:0], and output frequency. 0=h.w cinttrol, 1=s/w control	RW	0=h/w control	Not applicable	

Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Reserved, must be written as 0	R	Undefined	Not applicable	
6	Reserved, must be written as 0	R	Undefined	Not applicable	
5	Reserved, must be written as 0	R	Undefined	Not applicable	
4	Reserved, must be written as 0	R	Undefined	Not applicable	
3	Reserved, must be written as 0	R	Undefined	Not applicable	
2	CLKOUT enable, 0=disable, 1=enabled	RW	1=enabled	Not applicable	
1	Reserved, must be written as 0	R	Undefined	Not applicable	
0	Reserved, must be written as 0	R	Undefined	Not applicable	

Byte 2 through 5: Control

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved, must be written as 0	R	Undefined	Not applicable	

Byte 6: Control Register

Bit	Description	Type	Power Up	Output(s) Affected	Notes
7	Revision ID bit 3	R	--	Not applicable	
6	Revision ID bit 2	R	--	Not applicable	
5	Revision ID bit 1	R	--	Not applicable	
4	Revision ID bit 0	R	--	Not applicable	
3	Vendor ID bit 3	R	--	Not applicable	4
2	Vendor ID bit 2	R	--	Not applicable	4
1	Vendor ID bit 1	R	--	Not applicable	4
0	Vendor ID bit 0	R	--	Not applicable	4

Notes:

1. These bits are read-only when the hardware/software bit is set to hardware control.

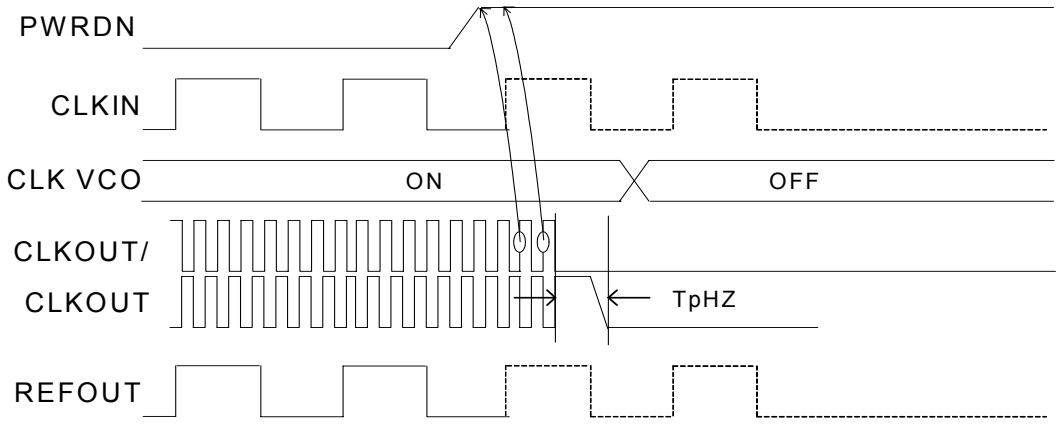
2. When the hardware/software bit is set to hardware control these bits reflect the state of the S[3:1] and SEL100/96# pins and the SO bit is set to zero. When the hardware/software bit is set to software control the S[3:1] and SEL100/96# pins are overridden by these bits.

3. See Spread Spectrum Selection Table on page 2 for spread selection options.

4. Use the same vendor ID as is used for the CK408 clock chip.

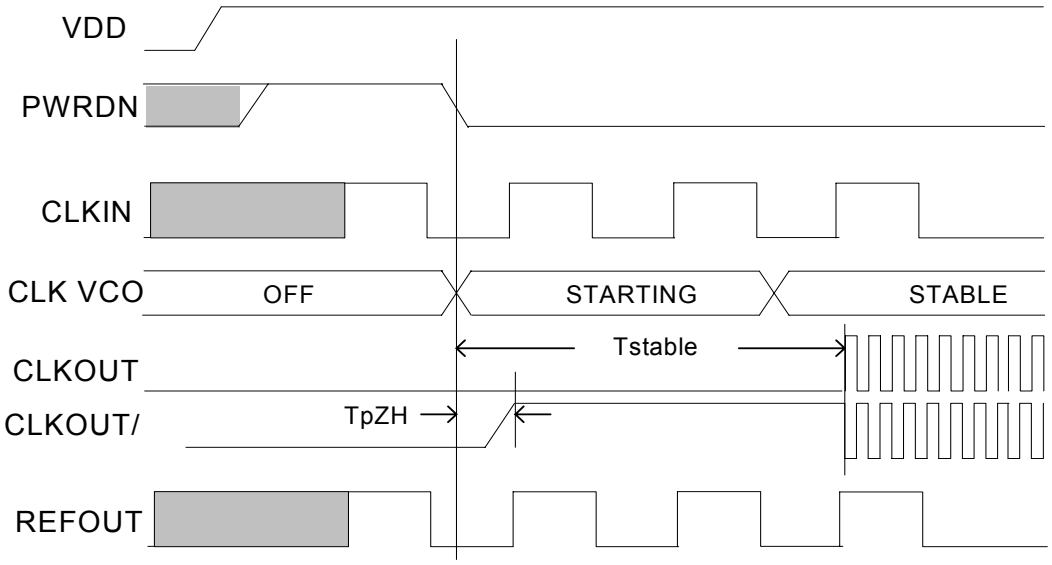
Power Down Mode Operation

The Power Down pin is used to shut off the clock cleanly prior to shutting off power to the device. The power down pin is an active high asynchronous input. When PWRDWN is sampled low for two output clock periods then all clocks need to be stopped prior to turning off the VCO. ALL clocks need to be stopped in a predictable manner.



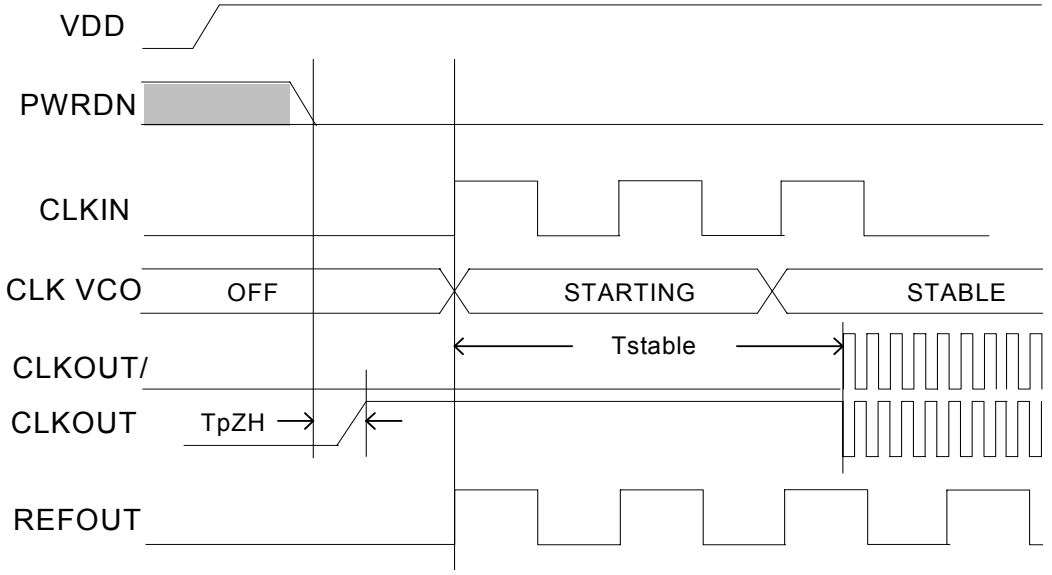
CLKOUT is driven differentially when PWRDWN# is de-asserted unless the CLKOUT is disabled through the SMBus register bit.

PWRDN/ De-Assertion, CLKIN Already Running



CLKIN must have a stable clock input when PWRDN is de-asserted. If CLKIN starts after PWRDN is de-asserted then Tstable specification applies to when CLKIN is ON. If CLKIN is full ON before PWRDN is de-asserted then the Tstable specification applies.

PWRDN/ De-Assertion, CLKIN Not Yet Running



Application Information

Series Termination Resistor

Clock output traces should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitors

As with any high-performance mixed-signal IC, the MK1493-05 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and the PCB ground plane.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) To minimize EMI, and obtain the best signal integrity, the 33Ω series termination resistor should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the MK1493-05.

This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1493-05. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD, VDDA	5.5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C
ESD Protection (Input)	2000 V min. (HBM)

Electrical Characteristics - DC

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V		3.135		3.465	
Input High Voltage[2]	V_{IH}		2.0		VDD +0.3	V
Input Low Voltage[2]	V_{IL}		VSS-0.3		0.8	V
Input Leakage Current[3]	I_{IL}	0 < Vin < VDD	-5		5	µA
Output High Voltage[2]	V_{OH}	I_{OH} = -1 mA	2.4			V
Output Low Voltage[2]	V_{OH}	I_{OH} = 1 mA			0.4	V
Output Current[5]	IoH	CLKOUT, Voh@Z=0.7 V@50 ohms	6*Iref		+12% x I	
Operating Supply Current	I_{DD}	No load			55	mA
	I_{DDPD}	No load, input low			400	µA
Input Capacitance	C_{IN}	Input pin capacitance			7	pF
Output Capacitance	C_{OUT}	Output pin capacitance			6	pF
Pin Inductance	L_{PIN}				5	nH
Output Resistance	Rout	CLKOUT	3.0			kΩ
Pull-up Resistor[1,4]	Rpu	Real time, asynchronous assertion		120		kΩ
Pull-down Resistor[1,4]	Rpd	Real time, asynchronous assertion		120		kΩ

[1]Includes ±50K ohm internal.
[2]Single edge is monotonic when transitioning through region.
[3]Inputs with pull-ups/-downs are not included.
[4]Internal leakage to ground is less than equal to 5 uA to ensure high level if input is floating.
[5]Configuration is Rr=475 ohms at 1%. Iref=2.32 mA. Iref=VDD/(3 x Rr).

Electrical Characteristics - CLKIN/REFOUT

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Rise Time	t_{RISE}	from 0.8 V to 2.0 V	500		1200	ps
Fall Time	t_{FALL}	from 2.0 V to 0.8 V	500		1200	ps
Edge Rate		Rising Edge	1.0		4.0	V/ns
Edge Rate		Falling Edge	1.0		4.0	V/ns
Duty Cycle[1]			40		60	%
Jitter, Cycle-to-Cycle[1]					1000	ps
Accuracy		Long Term Accuracy			300	ppm

[1]Measured from VDD/2.

Electrical Characteristics - CLKOUT

Unless stated otherwise, **VDD=3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
High Voltage[1,2]	V_H		660	700	850	mV
Low Voltage[1,2]	V_L		-150	0		mV
Crossing Point Voltage[1,2]		absolute	250		550	mV
Crossing Point Voltage[1,2,4]		variation over all edges			140	mV
Jitter, Cycle-to-Cycle[1,3]				80		ps
Modulation Frequency		spread spectrum		32.5		kHz
Rise Time[1,2]	t_{RISE}	from 0.175 V to 0.525 V. Rising edge CLKOUT and falling edge CLKOUT/.	175		700	ps
Fall Time[1,2]	t_{FALL}	from 2.0 V to 0.8 V	175		700	ps
Rise/Fall Time Variation[1,2]					125	ps
Rise/Fall Time Matching[1,2]					20	%
Duty Cycle[1,3]			45		55	%
Output Voltage Variation[1,2]		undershoot, overshoot	-0.3		Vhigh+0.3	V

[1]Test setup is Rs=33.2 ohms, Rp=49.9 ohms with 2 pF.

[2]Measurement taken from a single-ended waveform.

[3]Measurement taken from a differential waveform

[4]Measured at the crossing point where instantaneous voltages of both CLKOUT and CLKOUT/ are equal

Electrical Characteristics - AC

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C, C_L= 15 pF

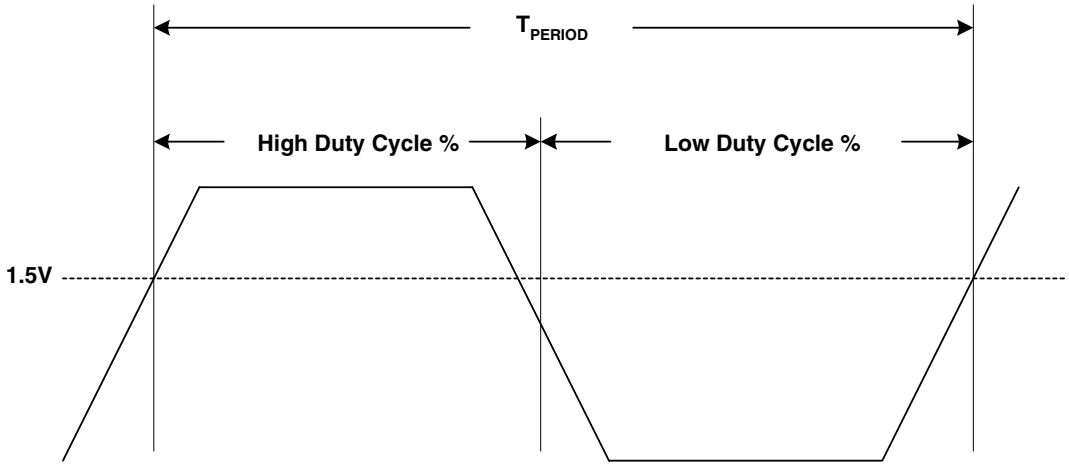
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Enable Time[1]	TpZL,TpZH	All outputs			10	us
Output Disable Time[1]	TpLZ,TpHZ	All outputs	600		1200	ps
Stabilization Time[2]	Tstable	from power-up		3.0		ms
Spread Change Time	Tspread	Settling period after spread change		3.0		ms

[1]CLKOUT and SMBus pins are tri-stated when PWRDN/ is asserted. CLKOUT is driven differential when PWRDN/ is de-asserted unless its already disabled.

[2]The period is when VDD equals its typical VDD condition.

Measurement Diagrams

Measurement diagram for duty cycle and jitter.



Current Reference Source (Iref)

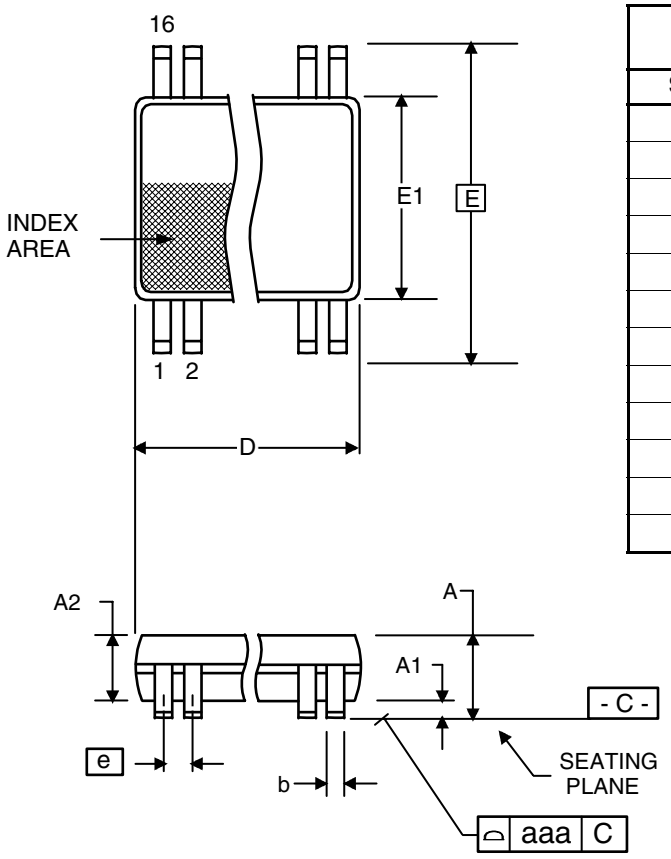
If board target trace impedance (Z) is 50Ω, then Rr = 475Ω (1%), providing IREF of 2.32 mA, output current (I_{OH}) is equal to 6*IREF.

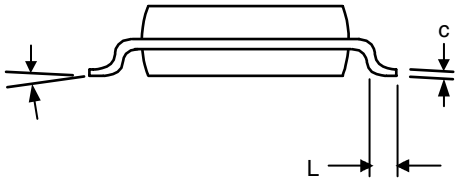
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153





	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
MK1493-05G*	149305G	Tubes	16-pin TSSOP	0 to +70° C
MK1493-05GTR*	149305G	Tape and Reel	16-pin TSSOP	0 to +70° C
MK1493-05GLF	149305GL	Tubes	16-pin TSSOP	0 to +70° C
MK1493-05GLFTR	149305GL	Tape and Reel	16-pin TSSOP	0 to +70° C
MK1493-05GLN	149305GN	Tubes	16-pin TSSOP	0 to +70° C
MK1493-05GLNTR	149305GN	Tape and Reel	16-pin TSSOP	0 to +70° C
MK1493-05GILF	49305GIL	Tubes	16-pin TSSOP	-40 to +85° C
MK1493-05GILFTR	49305GIL	Tape and Reel	16-pin TSSOP	-40 to +85° C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

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