

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

3.3V, 125-MHz, Multi-Output Zero Delay Buffer

Features

- Output frequency up to 125 MHz
- Supports PowerPC®, and Pentium® processors
- 12 clock outputs: frequency configurable
- Configurable Output Disable
- Two reference clock inputs for dynamic toggling
- Oscillator or PECL reference input
- Spread spectrum compatible
- Glitch-free output clocks transitioning
- 3.3V power supply
- Pin compatible with SC973X
- Industrial temperature range: -40°C to +85°C
- 52-Pin TQFP package

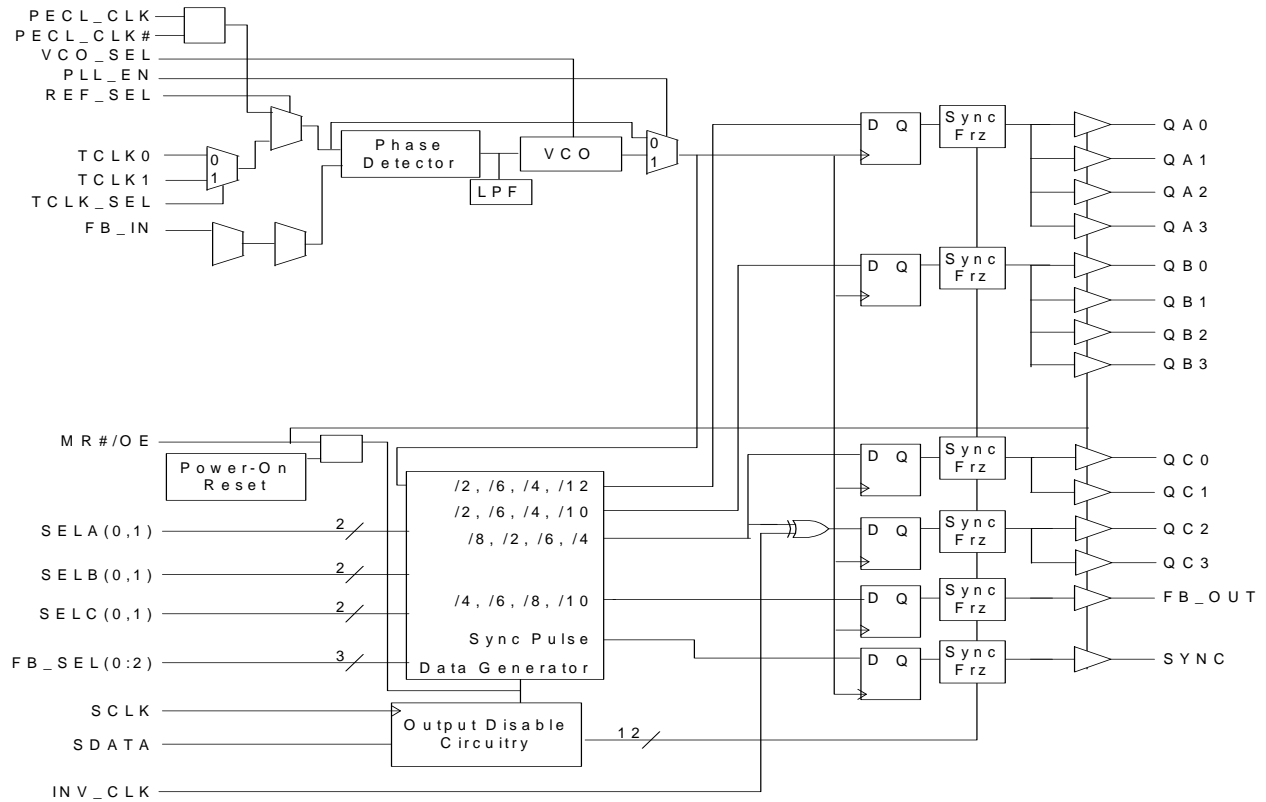
Table 1. Frequency Table^[1]

| VC0_SEL | FB_SEL2 | FB_SEL1 | FB_SEL0 | F _{VCO} |
|---------|---------|---------|---------|------------------|
| 0 | 0 | 0 | 0 | 8x |
| 0 | 0 | 0 | 1 | 12x |
| 0 | 0 | 1 | 0 | 16x |
| 0 | 0 | 1 | 1 | 20x |
| 0 | 1 | 0 | 0 | 8x |
| 0 | 1 | 0 | 1 | 12x |
| 0 | 1 | 1 | 0 | 16x |
| 0 | 1 | 1 | 1 | 20x |
| 1 | 0 | 0 | 0 | 4x |
| 1 | 0 | 0 | 1 | 6x |
| 1 | 0 | 1 | 0 | 8x |
| 1 | 0 | 1 | 1 | 10x |
| 1 | 1 | 0 | 0 | 4x |
| 1 | 1 | 0 | 1 | 6x |
| 1 | 1 | 1 | 0 | 8x |
| 1 | 1 | 1 | 1 | 10x |

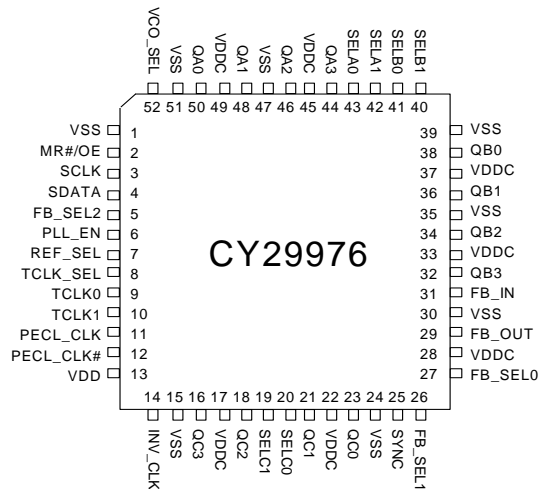
Note

1. x = the reference input frequency, 200MHz < F_{VCO} < 480MHz.

Logic Block Diagram



Pinouts



Pin Definitions^[2]

| Pin No. | Pin Name | PWR | IO | Type | Description |
|-------------------------------|-------------|------------------|----|------|---|
| 11 | PECL_CLK | | I | PU | PECL Clock Input. |
| 12 | PECL_CLK# | | I | PD | PECL Clock Input. |
| 9 | TCLK0 | | I | PU | External Reference/Test Clock Input. |
| 10 | TCLK1 | | I | PU | External Reference/Test Clock Input. |
| 44, 46, 48, 50 | QA(3:0) | V _{DDC} | O | | Clock Outputs. See Table 2 on page 4 for frequency selections. |
| 32, 34, 36, 38 | QB(3:0) | V _{DDC} | O | | Clock Outputs. See Table 2 on page 4 for frequency selections. |
| 16, 18, 21, 23 | QC(3:0) | V _{DDC} | O | | Clock Outputs. See Table 2 on page 4 for frequency selections. |
| 29 | FB_OUT | V _{DDC} | O | | Feedback Clock Output. Connect to FB_IN for normal operation. The divider ratio for this output is set by FB_SEL(0:2). See Table 1 on page 1. A bypass delay capacitor at this output controls Input Reference/ Output Banks phase relationships. |
| 25 | SYNC | V _{DDC} | O | | Synchronous Pulse Output. This output is used for system synchronization. The rising edge of the output pulse is in sync with both the rising edges of QA (0:3) and QC(0:3) output clocks regardless of the divider ratios selected. |
| 42, 43 | SELA(1,0) | | I | PU | Frequency Select Inputs. These inputs select the divider ratio at QA(0:3) outputs. See Table 2 on page 4. |
| 40, 41 | SELB(1,0) | | I | PU | Frequency Select Inputs. These inputs select the divider ratio at QB(0:3) outputs. See Table 2 on page 4. |
| 19, 20 | SELC(1,0) | | I | PU | Frequency Select Inputs. These inputs select the divider ratio at QC(0:3) outputs. See Table 2 on page 4. |
| 5, 26, 27 | FB_SEL(2:0) | | I | PU | Feedback Select Inputs. These inputs select the divide ratio at FB_OUT output. See Table 1 on page 1. |
| 52 | VCO_SEL | | I | PU | VCO Divider Select Input. When set LOW, the VCO output is divided by 2. When set HIGH, the divider is bypassed. See Table 1 on page 1. |
| 31 | FB_IN | | I | PU | Feedback Clock Input. Connect to FB_OUT for accessing the PLL. |
| 6 | PLL_EN | | I | PU | PLL Enable Input. When asserted HIGH, PLL is enabled. When LOW, PLL is bypassed. |
| 7 | REF_SEL | | I | PU | Reference Select Input. When HIGH, the PECL clock is selected. When LOW, TCLK (0,1) is the reference clock. |
| 8 | TCLK_SEL | | I | PU | TCLK Select Input. When LOW, TCLK0 is selected and when HIGH TCLK1 is selected. |
| 2 | MR#/OE | | I | PU | Master Reset/Output Enable Input. When asserted LOW, resets all of the internal flip-flops and also disables all of the outputs. When pulled HIGH, releases the internal flip-flops from reset and enables all of the outputs. |
| 14 | INV_CLK | | I | PU | Inverted Clock Input. When set HIGH, QC(2,3) outputs are inverted. When set LOW, the inverter is bypassed. |
| 3 | SCLK | | I | PU | Serial Clock Input. Clocks data at SDATA into the internal register. |
| 4 | SDATA | | I | PU | Serial Data Input. Input data is clocked to the internal register to enable/disable individual outputs. This provides flexibility in power management. |
| 17, 22, 28, 33, 37, 45, 49 | VDDC | | | | 3.3V Power Supply for Output Clock Buffers. |
| 13 | VDD | | | | 3.3V Supply for PLL |
| 1, 15, 24, 30, 35, 39, 47, 51 | VSS | | | | Common Ground |

Note

2. A bypass capacitor (0.1 μ F) must be placed as close as possible to each positive power (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristics are cancelled by the lead inductance of the traces.

Description

The CY29976 has an integrated PLL that provides low-skew and low-jitter clock outputs for high-performance microprocessors. Three independent banks of four outputs and an independent PLL feedback output, FB_OUT, provide exceptional flexibility for possible output configurations. The PLL is ensured stable operation given that the VCO is configured to run between 200 MHz to 480 MHz. This allows a wide range of output frequencies up to 125 MHz.

The phase detector compares the input reference clock to the external feedback input. For normal operation, the external feedback input, FB_IN, is connected to the feedback output, FB_OUT. The internal VCO is running at multiples of the input reference clock set by FB_SEL(0:2) and VCO_SEL select inputs,

refer to Frequency Table. The VCO frequency is then divided down to provide the required output frequencies. These dividers are set by SELA(0,1), SELB(0,1), SELC(0,1) select inputs, see Table 2. For situations where the VCO needs to run at relatively low frequencies and hence might not be stable, assert VCO_SEL low to divide the VCO frequency by 2. This maintains the desired output relationships, but provides an enhanced PLL lock range.

The CY29976 is also capable of providing inverted output clocks. When INV_CLK is asserted HIGH, QC2 and QC3 output clocks are inverted. These clocks could be used as feedback outputs to the CY29976 or a second PLL device to generate early or late clocks for a specific design. This inversion does not affect the output to output skew.

Table 2. Divider Table

| VCO_SEL | SELA1 | SELA0 | QA | SELB1 | SELB0 | QB | SELC1 | SELC0 | QC |
|---------|-------|-------|--------|-------|-------|--------|-------|-------|--------|
| 0 | 0 | 0 | VCO/4 | 0 | 0 | VCO/4 | 0 | 0 | VCO/16 |
| 0 | 0 | 1 | VCO/12 | 0 | 1 | VCO/12 | 0 | 1 | VCO/4 |
| 0 | 1 | 0 | VCO/8 | 1 | 0 | VCO/8 | 1 | 0 | VCO/12 |
| 0 | 1 | 1 | VCO/24 | 1 | 1 | VCO/20 | 1 | 1 | VCO/8 |
| 1 | 0 | 0 | VCO/2 | 0 | 0 | VCO/2 | 0 | 0 | VCO/8 |
| 1 | 0 | 1 | VCO/6 | 0 | 1 | VCO/6 | 0 | 1 | VCO/2 |
| 1 | 1 | 0 | VCO/4 | 1 | 0 | VCO/4 | 1 | 0 | VCO/6 |
| 1 | 1 | 1 | VCO/12 | 1 | 1 | VCO/10 | 1 | 1 | VCO/4 |

Zero Delay Buffer

When used as a zero delay buffer the CY29976 is likely be in a nested clock tree application. For these applications the CY29976 offers a low voltage PECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The CY29976 then can lock onto the LVPECL reference and translate with near zero delay to low skew outputs.

By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs. Because the static phase offset is a function of the reference clock the Tpd of the CY29976 is a function of the configuration used.

Glitch-Free Output Frequency Transitions

Customarily when output buffers have their internal counter's changed "on the fly" their output clock periods will:

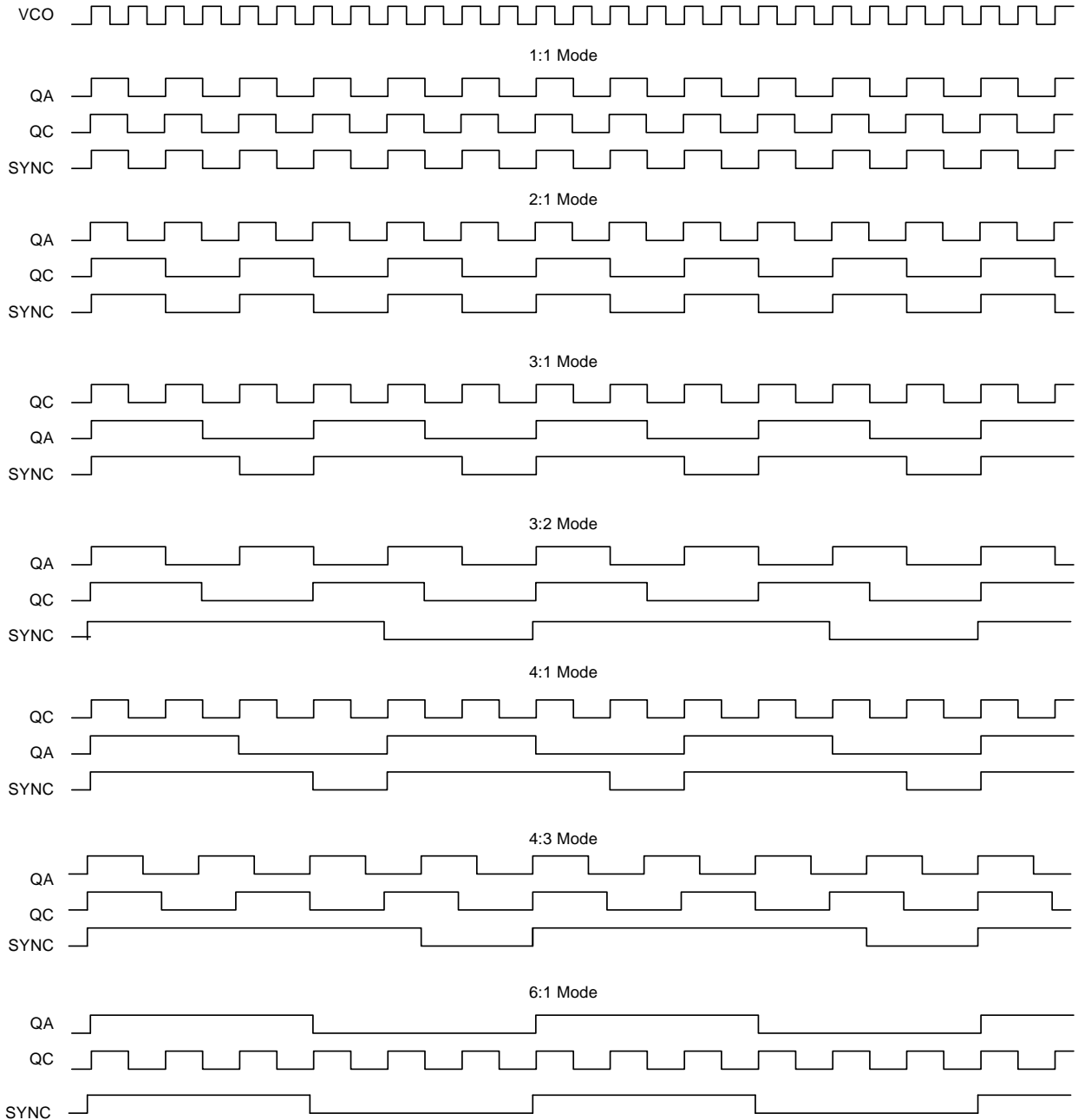
- Contain short or "runt" clock periods. These are clock cycles in which the cycle(s) are shorter in period than either the old or new frequency that is being transitioned to.
- Contain stretched clock periods. These are clock cycles in which the cycle(s) are longer in period than either the old or new frequency that is being transitioned to.

This device specifically includes logic to guarantee that runt and stretched clock pulses do not occur if the device logic levels of any or all of the following pins changed "on the fly" while it is operating: SELA, SELB, SELC, and VCO_SEL.

SYNC Output

In situations where output frequency relationships are not integer multiples of each other the SYNC output provides a signal for system synchronization. The CY29976 monitors the relationship between the QA and the QC output clocks. It provides a low going pulse, one period in duration, one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse depend on the higher of the QA and QC output frequencies. The following timing diagram (Figure 1) illustrates various waveforms for the SYNC output. Note that the SYNC output is defined for all possible combinations of the QA and QC outputs even though under some relationships the lower frequency clock could be used as a synchronizing signal.

Figure 1. SYNC output for different input and out ratio



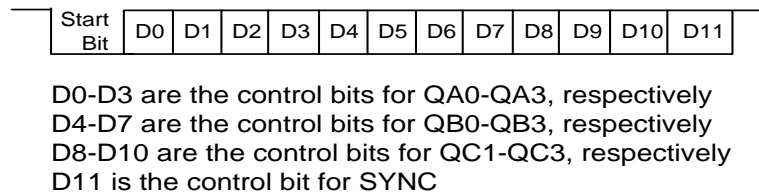
Power Management

The individual output enable/freeze control of the CY29976 allows the user to implement unique power management schemes into the design. The outputs are stopped in the logic '0' state when the freeze control bits are activated. The serial input register contains one programmable freeze enable bit for 12 of the 14 output clocks. The QC0 and FB_OUT outputs can not be frozen with the serial port, this avoids any potential lock up situation must an error occur in the loading of the serial data. An output is frozen when a logic '0' is programmed and enabled

when a logic '1' is written. The enabling and freezing of individual outputs is done in such a manner as to eliminate the possibility of partial "runt" clocks.

The serial input register is programmed through the SDATA input by writing a logic '0' start bit followed by 12 NRZ freeze enable bits. The period of each SDATA bit equals the period of the free running SCLK signal. The SDATA is sampled on the rising edge of SCLK.

Figure 2. Control Bit Map



Maximum Ratings^[3]

Input Voltage Relative to V_{SS} : $V_{SS} - 0.3V$
 Input Voltage Relative to V_{DD} : $V_{DD} + 0.3V$
 Storage Temperature: $-65^{\circ}C$ to $+150^{\circ}C$
 Operating Temperature: $-40^{\circ}C$ to $+85^{\circ}C$
 Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions must be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} must be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters $V_{DD} = V_{DDC} = 3.3V \pm 10\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

| Parameter | Description | Conditions | Min | Typ. | Max | Unit |
|-----------|--|------------------------------------|----------------|------|----------------|---------|
| V_{IL} | Input Low Voltage | | V_{SS} | | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.0 | | V_{DD} | V |
| V_{PP} | Peak-to-Peak Input Voltage PECL_CLK | Note 4 | 300 | | 1000 | mV |
| V_{CMR} | Common Mode Range PECL_CLK | | $V_{DD} - 2.0$ | | $V_{DD} - 0.6$ | V |
| I_{IL} | Input Low Current (at $V_{IL} = V_{SS}$) | Note 5 | | | -120 | μA |
| I_{IH} | Input High Current (at $V_{IH} = V_{DD}$) | Note 5 | | | 120 | μA |
| V_{OL} | Output Low Voltage | $I_{OL} = 20 \text{ mA}$, Note 6 | | | 0.5 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -20 \text{ mA}$, Note 6 | 2.4 | | | V |
| I_{DDC} | Quiescent Supply Current | All V_{DDC} and V_{DD} | | 10 | 15 | mA |
| I_{DD} | PLL Supply Current | V_{DD} only | | | 15 | mA |
| C_{in} | Input Pin Capacitance | | | 4 | | pF |

Notes

3. Multiple Supplies: The voltage on any input or IO pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.
4. The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when "High" input is within the V_{CMR} range and the input lies within the V_{PP} specification.
5. Inputs have pull up/pull down resistors that effect input current.
6. Driving series or parallel terminated 50 Ω (or 50 Ω to $V_{DD}/2$) transmission lines.

AC Parameters^[7] $V_{DD} = V_{DDC} = 3.3V \pm 10\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

| Parameter | Description | Conditions | Min | Typ. | Max | Unit | |
|------------|---|----------------------------------|--------------------|-----------|--------|------|----|
| Tr/Tf | TCLK Input Rise / Fall | | | | 3.0 | ns | |
| Fref | Reference Input Frequency | | Note 8 | | Note 8 | MHz | |
| FrefDC | Reference Input Duty Cycle | | 25 | | 75 | % | |
| Fvco | PLL VCO Lock Range | | 200 | | 480 | MHz | |
| Tlock | Maximum PLL lock Time | | | | 10 | ms | |
| Tr/Tf | Output Clocks Rise/Fall Time ^[9] | 0.8V to 2.0V | 0.15 | | 1.2 | ns | |
| Fout | Maximum Output Frequency | Q ($\div 2$) | - | | 125 | MHz | |
| | | Q ($\div 4$) | | | 120 | | |
| | | Q ($\div 6$) | | | 80 | | |
| | | Q ($\div 8$) | | | 60 | | |
| FoutDC | Output Duty Cycle ^[9] | | 45 | | 55 | % | |
| tpZL, tpZH | Output Enable Time ^[9] (all outputs) | | 2 | | 10 | ns | |
| tpLZ, tpHZ | Output Disable Time ^[9] (all outputs) | | 2 | | 8 | ns | |
| TCCJ | Cycle to Cycle Jitter ^[9] (peak to peak) | | | ± 100 | | ps | |
| TSKEW | Any Output to Any Output Skew ^[9,10] | All outputs at same frequency | | | 350 | ps | |
| | | Outputs at different frequencies | | | 550 | ps | |
| Tpd | Propagation Delay ^[10,11] | PECL_CLK ^[12] | QFB = ($\div 8$) | -225 | -25 | 175 | ps |
| | | TCLK0/1 | | -130 | | 270 | |

Ordering Information

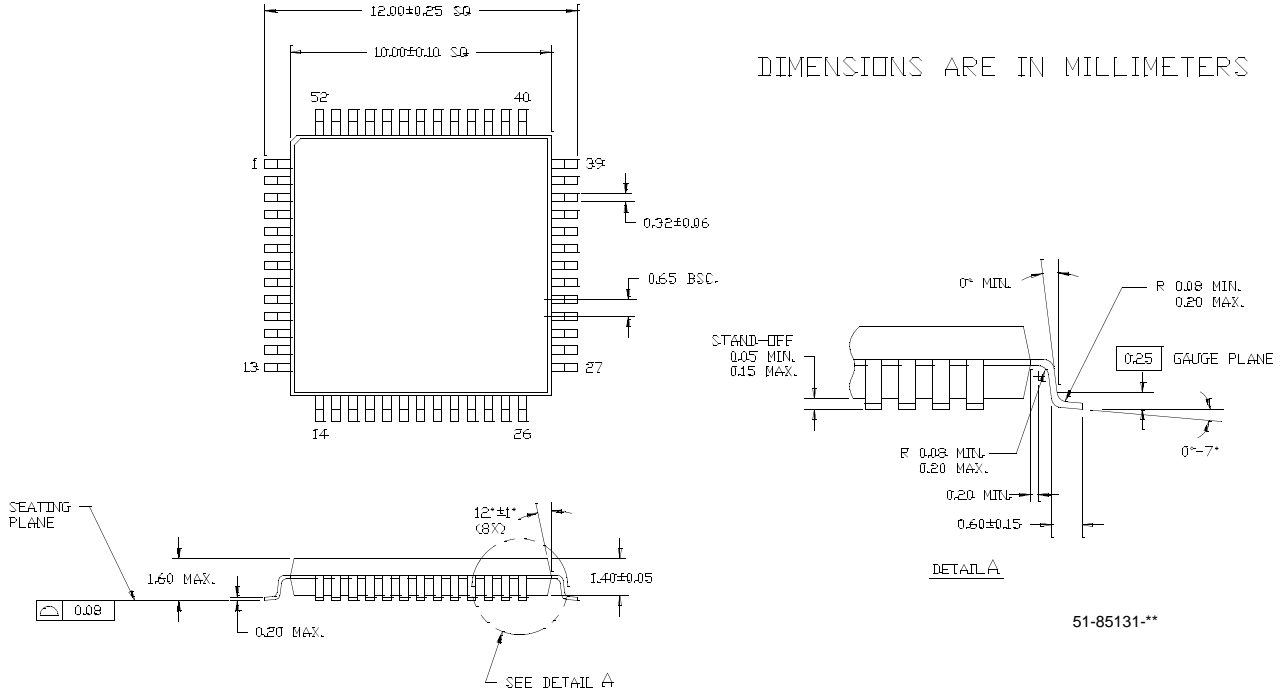
| Part Number | Package Name | Package Type | Production Flow |
|--------------------------|--------------|-----------------------------|--|
| CY29976A ^[13] | A52 | 52-Pin TQFP | Industrial, $-40^{\circ}C$ to $+85^{\circ}C$ |
| Pb-Free | | | |
| CY29976AXI | A52 | 52-Pin TQFP | Industrial, $-40^{\circ}C$ to $+85^{\circ}C$ |
| CY29976AXIT | A52 | 52-Pin TQFP – Tape and reel | Industrial, $-40^{\circ}C$ to $+85^{\circ}C$ |

Notes

7. Parameters are guaranteed by design and characterization. Not 100% tested in production.
8. Maximum and minimum input reference is limited by VCO lock range.
9. Outputs loaded with 30 pF each.
10. 50 Ω transmission line terminated into $V_{DD}/2$.
11. Tpd is specified for a 50 MHz input reference. Tpd is the static phase error of the device and does not include jitter.
12. $V_{CMR} = 2.0V$ and $V_{PP} = 650\mu V$. Tpd window varies with different V_{CMR} and V_{PP} values.
13. Not Recommended for new designs.

Package Drawing and Dimensions

Figure 3. 52-Pin Thin Plastic Quad Flat Pack (10x10x1.4 mm) A52



Document History Page

| Document Title: CY29976 3.3V, 125-MHz, Multi-Output Zero Delay Buffer Document Number: 38-07413 | | | | |
|--|---------|-----------------|-----------------|--|
| REV | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 114663 | HWT | 05/14/02 | New Data Sheet |
| *A | 122922 | RBI | 12/27/02 | Add power up requirements to maximum ratings information. |
| *B | 2562606 | AESA | 09/09/08 | Updated template. Added Note "Not recommended for new designs." Added part number CY29976AXI and CY29976AXIT in ordering information table. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer’s representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

| | |
|------------------|--|
| PSoC | psoc.cypress.com |
| Clocks & Buffers | clocks.cypress.com |
| Wireless | wireless.cypress.com |
| Memories | memory.cypress.com |
| Image Sensors | image.cypress.com |

PSoC Solutions

| | |
|-----------------------|--|
| General | psoc.cypress.com/solutions |
| Low Power/Low Voltage | psoc.cypress.com/low-power |
| Precision Analog | psoc.cypress.com/precision-analog |
| LCD Drive | psoc.cypress.com/lcd-drive |
| CAN 2.0b | psoc.cypress.com/can |
| USB | psoc.cypress.com/usb |

© Cypress Semiconductor Corporation, 2002 - 2008. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress’ product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.