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CY28378

FTG for Pentium 4® and Intel® 845 Series Chipset

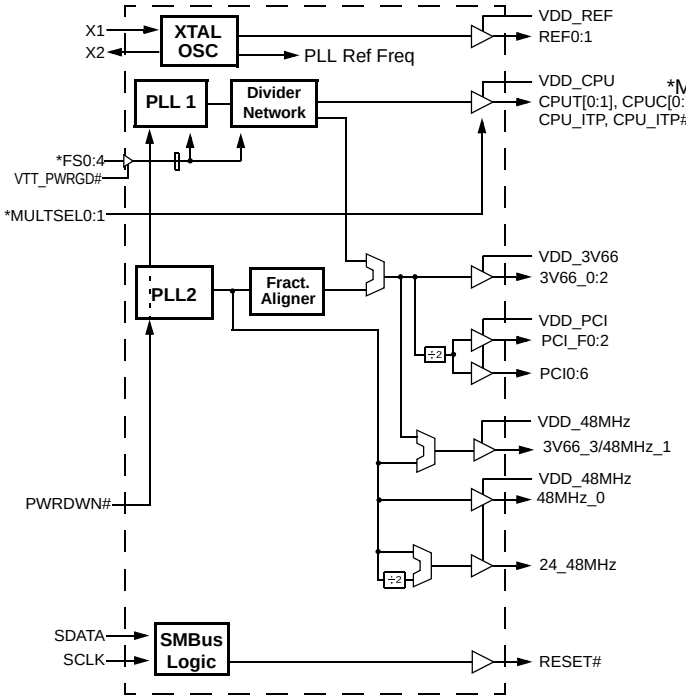
Features

- **Compatible with Intel® CK-Titan and CK-408 Clock Synthesizer/Driver specifications**
- **System frequency synthesizer for Intel Brookdale 845 and Brookdale – G Pentium 4® chipsets**
- **Programmable clock output frequency with less than 1-MHz increment**
- **Integrated fail-safe Watchdog timer for system recovery**
- **Automatically switch to HW selected or SW programmed clock frequency when Watchdog timer time-out**
- **Programmable 3V66 and PCI output frequency mode**
- **Capable of generating system RESET after a Watchdog timer time-out or a change in output frequency via SMBus interface occurs**
- **Support SMBus byte read/write and block read/ write operations to simplify system BIOS development**
- **Vendor ID and Revision ID support**
- **Programmable drive strength support**
- **Programmable output skew support**
- **Power management control inputs**
- **Available in 48-pin SSOP**

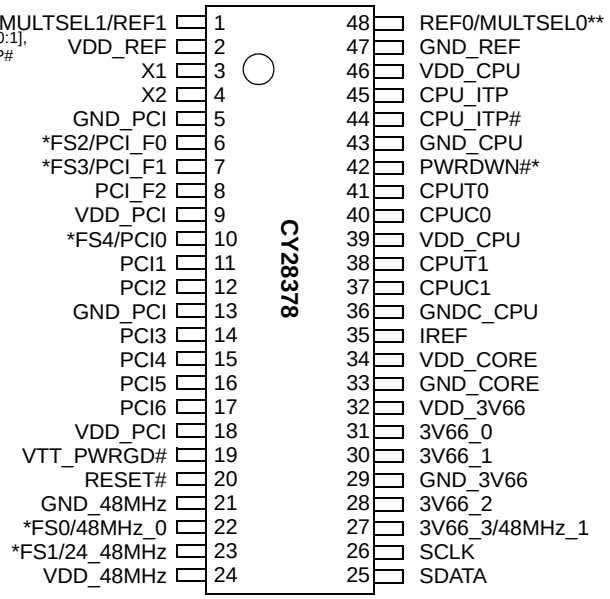
Table 1. Frequency Table

CPU	3V66	PCI	REF	48M	24_48M
x 3	x 4	x 10	x 2	x 1	x 1

Block Diagram



Pin Configuration[1]



SSOP-48

Note:
1. Signals marked with '*' and '**' have internal pull-up and pull-down resistors, respectively.

400 West Cesar Chavez, Austin, TX 78701 1+(512) 416-8500 1+(512) 416-9669 www.silabs.com

Pin Description

Pin #	Name	Type	Description
3	X1	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
4	X2	O	***Crystal Connection:*** Connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
48	REF0/MULTSEL0	I/O	***Reference Clock 0/Current Multiplier Selection 0:*** 3.3V 14.318-MHz clock output. This pin also serves as a power-on strap option to determine the current multiplier for the CPU clock outputs. The MULTSEL1:0 definitions are as follows: MULTSEL1:0 00 = Ioh is 4 x IREF 01 = Ioh is 5 x IREF 10 = Ioh is 6 x IREF 11 = Ioh is 7 x IREF 150k internal pull down.
1	REF1/MULTSEL1	I/O	***Reference Clock 1/Current Multiplier Selection 1:*** 3.3V 14.318-MHz clock output. This pin also serves as a power-on strap option to determine the current multiplier for the CPU clock outputs. The MULTSEL1:0 definitions are as follows: MULTSEL1:0 00 = Ioh is 4 x IREF 01 = Ioh is 5 x IREF 10 = Ioh is 6 x IREF 11 = Ioh is 7 x IREF 150k internal pull up.
41, 38, 40, 37	CPUT(0:1), CPUC(0:1)	O	***CPU Clock Outputs:*** Frequency is set by the FS0:4 inputs or through serial input interface.
44, 45	CPU_ITP, CPU_ITP#	O	***CPU Clock Output for ITP:*** Frequency is set by the FS0:4 inputs or through serial input interface.
31, 30, 28	3V66_0:2	O	***66MHz Clock Outputs:*** 3.3V fixed 66-MHz clock.
6	PCI_F0/FS2	I/O	***Free-running PCI Output 0/Frequency Select 2:*** 3.3V free-running PCI output. This pin also serves as a power-on strap option to determine device operating frequency as described in the Frequency Selection Table. 150k internal pull up.
7	PCI_F1/FS3	I/O	***Free-running PCI Output 1/Frequency Select 3:*** 3.3V free-running PCI output. This pin also serves as a power-on strap option to determine device operating frequency as described in the *Table 2*. 150k internal pull up.
8	PCI_F2	O	***Free-running PCI Output 2:*** 3.3V free-running PCI output.
10	PCI0/FS4	I/O	***PCI Output 0/Frequency Select 4:*** 3.3V PCI output. This pin also serves as a power-on strap option to determine device operating frequency as described in *Table 2*. 150k internal pull up.
11, 12, 14, 15, 16, 17	PCI(1:6)	O	***PCI Clock Output 1 to 6:*** 3.3V PCI clock outputs.
22	48MHz_0/FS0	I/O	***48MHz Output/Frequency Select 0:*** 3.3V fixed 48-MHz, non-spread spectrum output. This pin also serves as a power-on strap option to determine device operating frequency as described in *Table 2*. This output will be used as the reference clock for USB host controller in Intel 845 (Brookdale) platforms. For Intel Brookdale – G platforms, this output will be used as the VCH reference clock. 150k internal pull up.

Pin Description

Pin #	Name	Type	Description
23	24_48MHz/FS1	I/O	***24 or 48MHz Output/Frequency Select 1:*** 3.3V fixed 24-MHz or 48-MHz non-spread spectrum output. This pin also serves as a power-on strap option to determine device operating frequency as described in *Table 2*. This output will be used as the reference clock for SIO devices in Intel 845 (Brookdale) platforms. For Intel Brookdale – G platforms, this output will be used as the reference clock for both USB host controller and SIO devices. We recommend system designer to configure this output as 48 MHz and “HIGH Drive” by setting Byte [5], Bit [0] and Byte [9], Bit [7], respectively.150k internal pull up.
27	3V66_3/48MHz_1	O	***48MHz or 66MHz Output:*** 3.3V output.
42	PWRDWN#	I	***Power Down Control:*** 3.3V LVTTL compatible input that places the device in power down mode when held low. 150k internal pull up.
26	SCLK	I	***SMBus Clock Input:*** Clock pin for serial interface.
25	SDATA	I/O	***SMBus Data Input:*** Data pin for serial interface.
20	RESET#	O (open-drain)	***System Reset Output:*** Open-drain system reset output.
35	IREF	I	***Current Reference for CPU Output:*** A precision resistor is attached to this pin which is connected to the internal current reference.
19	VTT_PWRGD#	I	***Powergood from Voltage Regulator Module (VRM):*** 3.3V LVTTL input. VTT_PWRGD# is a level sensitive strobe used to determine when FS0:4 and MULTSEL0:1 inputs are valid and OK to be sampled (Active LOW). Once VTT_PWRGD# is sampled LOW, the status of this input will be ignored.
2, 9, 18, 24, 32, 39, 46	VDD_REF, VDD _PCI, VDD_48MHz, VDD_3V66, VDD_CPU	P	***3.3V Power Connection:*** Power supply for CPU outputs buffers, 3V66 output buffers, PCI output buffers, reference output buffers and 48-MHz output buffers. Connect to 3.3V.
5, 13, 21, 29, 36, 43, 47	GND_PCI, GND_48MHz, GND_3V66, GND_CPU, GND_REF,	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.
34	VDD_CORE	P	***3.3V Analog Power Connection:*** Power supply for core logic, PLL circuitry. Connect to 3.3V.
33	GND_CORE	G	***Analog Ground Connection:*** Ground for core logic, PLL circuitry.

Table 2. Frequency Selection Table

Input Conditions					Output Frequency			VCO Freq.	PLL Gear Constants (G)
FS4	FS3	FS2	FS1	FS0					
SEL4	SEL3	SEL2	SEL1	SEL0	CPU	3V66	PCI		
0	0	0	0	0	100.7	67.1	33.6	402.80	47.99750
0	0	0	0	1	100.9	67.3	33.6	403.60	47.99750
0	0	0	1	0	108.0	72.0	36.0	432.00	47.99750
0	0	0	1	1	101.2	67.5	33.7	404.80	47.99750
0	0	1	0	0	114.0	76.0	38.0	456.00	47.99750
0	0	1	0	1	117.0	78.0	39.0	468.00	47.99750
0	0	1	1	0	120.0	80.0	40.0	480.00	47.99750
0	0	1	1	1	123.0	82.0	41.0	492.00	47.99750
0	1	0	0	0	125.7	62.9	31.4	377.12	63.99667
0	1	0	0	1	130.3	65.1	32.6	390.80	63.99667
0	1	0	1	0	133.9	67.0	33.5	401.70	63.99667
0	1	0	1	1	134.2	67.1	33.6	402.60	63.99667
0	1	1	0	0	134.5	67.3	33.6	403.50	63.99667
0	1	1	0	1	148.0	74.0	37.0	444.00	63.99667
0	1	1	1	0	152.0	76.0	38.0	456.00	63.99667
0	1	1	1	1	156.0	78.0	39.0	468.00	63.99667
1	0	0	0	0	160.0	80.0	40.0	480.00	63.99667
1	0	0	0	1	164.0	82.0	41.0	492.00	63.99667
1	0	0	1	0	167.4	66.9	33.5	334.80	95.99500
1	0	0	1	1	170.0	68.0	34.0	340.00	95.99500
1	0	1	0	0	175.0	70.0	35.0	350.00	95.99500
1	0	1	0	1	180.0	72.0	36.0	360.00	95.99500
1	0	1	1	0	185.0	74.0	37.0	370.00	95.99500
1	0	1	1	1	190.0	76.0	38.0	380.00	95.99500
1	1	0	0	0	166.8	66.7	33.4	333.60	95.99500
1	1	0	0	1	100.2	66.8	33.4	400.80	47.99750
1	1	0	1	0	133.6	66.8	33.4	400.80	63.99667
1	1	0	1	1	200.4	66.8	33.4	400.80	95.99500
1	1	1	0	0	166.6	66.6	33.3	333.33	95.99500
1	1	1	0	1	100.0	66.6	33.3	400.00	47.99750
1	1	1	1	0	200.0	66.6	33.3	400.00	95.99500
1	1	1	1	1	133.3	66.6	33.3	400.00	63.99667

Swing Select Functions

MULTSEL1	MULTSEL0	Board Target Trace/Term Z	Reference R, IREF = VDD/(3*Rr)	Output Current	V_{OH} @ Z
0	0	50Ω	Rr = 221 1%, IREF = 5.00 mA	I_{OH} = 4*Iref	1.0V @ 50
1	0	50Ω	Rr = 475 1%, IREF = 2.32 mA	I_{OH} = 6*Iref	0.7V @ 50

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface (SDI), various device functions such as individual clock output buffers, etc. can be individually enabled or disabled.

The register associated with the SDI initializes to it's default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write and block read operation from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 3*.

The block write and block read protocol is outlined in *Table 4* while *Table 5* outlines the corresponding byte write and byte read protocol.

The slave receiver address is 11010010 (D2h).

Table 3. Command Code Definition

Bit	Descriptions
7	0 = Block read or block write operation 1 = Byte read or byte write operation
6:0	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'.

Table 4. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 Bit '00000000' stands for block operation	11:18	Command Code – 8 Bit '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 2 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	.....	39:46	Data byte from slave – 8 bits
....	Data Byte (N–1) –8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave – 8 bits
....	Data Byte N –8 bits	56	Acknowledge
....	Acknowledge from slave	....	Data bytes from slave/Acknowledge
....	Stop	....	Data byte N from slave – 8 bits
		....	Not Acknowledge
		....	Stop

Table 5. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Not Acknowledge
		39	Stop

Byte Configuration Map

Byte 0

Bit	@Pup	Name	Description
Bit 7	0	Spread Select2	'000' = OFF '001' = +0.12, – 0.62% '010' = +0.25, – 0.75% '011' = +0.50, – 1.00% '100' = ± 0.25% '101' = +0.00, – 0.50% '110' = ±0.5% '111' = ±0.38%
Bit 6	0	Spread Select1	
Bit 5	0	Spread Select0	
Bit 4	0	SEL4	SW Frequency selection bits. See *Table 2*.
Bit 3	0	SEL3	
Bit 2	0	SEL2	
Bit 1	0	SEL1	
Bit 0	0	SEL0	

Byte 1

Bit	@Pup	Name	Description
Bit 7	1	CPUT1, CPUC1	(Active/Inactive)
Bit 6	1	CPUT0, CPUC0	
Bit 5	1	48MHz	(Active/Inactive)
Bit 4	1	24_48MHz	(Active/Inactive)
Bit 3	1	3V66_3	(Active/Inactive)
Bit 2	1	3V66_2	(Active/Inactive)
Bit 1	1	3V66_1	(Active/Inactive)
Bit 0	1	3V66_0	(Active/Inactive)

Byte 2

Bit	@pup	Name	Pin Description
Bit 7	0	Reserved	Reserved
Bit 6	1	PCI6	(Active/Inactive)
Bit 5	1	PCI5	(Active/Inactive)
Bit 4	1	PCI4	(Active/Inactive)
Bit 3	1	PCI3	(Active/Inactive)
Bit 2	1	PCI2	(Active/Inactive)
Bit 1	1	PCI1	(Active/Inactive)
Bit 0	1	PCI0	(Active/Inactive)

Byte 3

Bit	@Pup	Name	Pin Description
Bit 7	1	PCI_F2	(Active/Inactive)
Bit 6	1	PCI_F1	(Active/Inactive)
Bit 5	1	PCI_F0	(Active/Inactive)
Bit 4	0	Reserved	Reserved
Bit 3	1	CPU_ITP, CPU_ITP#	(Active/Inactive)
Bit 2	0	Reserved	Reserved
Bit 1	1	REF1	(Active/Inactive)
Bit 0	1	REF0	(Active/Inactive)

Byte 4

Bit	@Pup	Name	Pin Description
Bit 7	0	MULTSEL_Override	This bit control the selection of IREF multiple. 0 = HW control; IREF multiplier is determined by MULTSEL[0:1] input pins 1 = SW control; IREF multiplier is determined by Byte[4], Bit[5:6].
Bit 6	HW	SW_MULTSEL1	IREF multiplier 00 = Ioh is 4 x IREF 01 = Ioh is 5 x IREF 10 = Ioh is 6 x IREF 11 = Ioh is 7 x IREF
Bit 5	HW	SW_MULTSEL0	
Bit 4	0	Reserved	Reserved
Bit 3	0	Reserved	Reserved
Bit 2	0	Reserved	Reserved
Bit 1	0	Reserved	Reserved
Bit 0	0	Reserved	Vendor Test Mode (always program to 0)

Byte 5

Bit	@Pup	Name	Pin Description
Bit 7	HW	Latched FS4 input	Latched FS[4:0] inputs. These bits are read only.
Bit 6	HW	Latched FS3 input	
Bit 5	HW	Latched FS2 input	
Bit 4	HW	Latched FS1 input	
Bit 3	HW	Latched FS0 input	
Bit 2	0	FS_Override	0 = Select operating frequency by FS[4:0] input pins 1 = Select operating frequency by SEL[4:0] settings
Bit 1	0	SEL 3V66	0 = 48-MHz output on pin 27, 1 = 66-MHz output on pin 27
Bit 0	1	SEL 48MHZ	0 = 24-MHz,1 = 48-MHz

Byte 6

Bit	@Pup	Name	Pin Description
Bit 7	0	Revision_ID3	Revision ID bit[3]
Bit 6	0	Revision_ID2	Revision ID bit[2]
Bit 5	0	Revision_ID1	Revision ID bit[1]
Bit 4	1	Revision_ID0	Revision ID bit[0]
Bit 3	1	Vendor_ID3	Bit[3] of Cypress Semiconductor's Vendor ID. This bit is read only.
Bit 2	0	Vendor_ID2	Bit[2] of Cypress Semiconductor's Vendor ID. This bit is read only.
Bit 1	0	Vendor _ID1	Bit[1] of Cypress Semiconductor's Vendor ID. This bit is read only.
Bit 0	0	Vendor _ID0	Bit[0] of Cypress Semiconductor's Vendor ID. This bit is read only.

Byte 7

Bit	@Pup	Name	Pin Description
Bit 7	0	Reserved	Vendor Test Mode (always program to 0)
Bit 6	0	Reserved	Vendor Test Mode (always program to 0)
Bit 5	0	Reserved	Vendor Test Mode (always program to 0)
Bit 4	0	Reserved	Vendor Test Mode (always program to 0)
Bit 3	0	3V66 Fract_Align3	3V66 Frequency Fractional Aligner: These bits determine the 3V66 fixed frequency. This option does not incorporate spread spectrum and is enabled through Byte10, bit 4
Bit 2	0	3V66 Fract_Align2	[illegible]
Bit 1	0	3V66 Fract_Align1	001067.533.7
Bit 0	0	3V66 Fract_Align0	001168.534.3 010069.534.8 010170.635.3 011071.635.8 011172.636.3 100073.636.8 100174.737.3 101075.737.8 101176.738.4 110077.738.9

Byte 8

Bit	@Pup	Name	Pin Description
Bit 7	0	WD_Alarm	This bit is set to "1" when the Watchdog times out. It is reset to "0" when the system clears the WD_TIMER time stamp
Bit 6	0	Frequency_Revert	This bit allows setting the Revert Frequency once the system is rebooted 0: Hardware 1: Last Programmed
Bit 5	0	Reserved	Reserved
Bit 4	0	WD_TIMER3	Watchdog timer time stamp selection: 0000: Off 0001: 1 second 0010: 2 seconds . . . 1110: 14 seconds 1111: 15 seconds
Bit 3	0	WD_TIMER2	
Bit 2	0	WD_TIMER1	
Bit 1	0	WD_TIMER0	
Bit 0	1	Reserved	Reserved

Byte 9

Bit	@Pup	Name	Pin Description
Bit 7	0	48MHz_DRV	48MHz and 24_48MHz clock output drive strength 0 = Normal 1 = High Drive (Recommend to set to high drive if this output is being used to drive both USB and SIO devices in Intel Brookdale – G platforms)
Bit 6	0	PCI_DRV	PCI clock output drive strength 0 = Normal 1 = High Drive
Bit 5	0	3V66_DRV	3V66 clock output drive strength 0 = Normal 1 = High Drive
Bit 4	0	Reserved	Reserved
Bit 3	0	Reserved	Reserved
Bit 2	0	Reserved	Reserved
Bit 1	0	Reserved	Reserved
Bit 0	0	Reserved	Reserved

Byte 10

Bit	@Pup	Name	Pin Description
Bit 7	0	CPU_Skew2	CPU skew control 000 = Normal 001 = –150 ps 010 = –300 ps 011 = –450 ps 100 = +150 ps 101 = +300 ps 110 = +450 ps 111 = +600 ps
Bit 6	0	CPU_Skew1	
Bit 5	0	CPU_Skew0	
Bit 4	0	Fixed 3V66_SEL	3V66 and PCI output frequency select mode 0 = Set according to Frequency Selection Table 1 = Set according to Fractional Aligner settings
Bit 3	0	PCI_Skew1	PCI skew control 00 = Normal 01 = –500 ps 10 = Reserved 11 = +500 ps
Bit 2	0	PCI_Skew0	
Bit 1	0	3V66_Skew1	3V66 skew control 00 = Normal 01 = –150 ps 10 = +150 ps 11 = +300 ps
Bit 0	0	3V66_Skew0	

Byte 11

Bit	@Pup	Name	Pin Description
Bit 7	0	Reserved	Reserved
Bit 6	0	Reserved	Reserved
Bit 5	0	Reserved	Reserved
Bit 4	0	Reserved	Reserved
Bit 3	0	Reserved	Reserved
Bit 2	0	Reserved	Reserved
Bit 1	0	Reserved	Reserved
Bit 0	0	Reserved	Reserved

Byte 12

Bit	@Pup	Name	Pin Description
Bit 7	0	Reserved	Reserved
Bit 6	0	Reserved	Reserved
Bit 5	0	Reserved	Reserved
Bit 4	0	Reserved	Reserved
Bit 3	0	Reserved	Reserved
Bit 2	0	Reserved	Reserved
Bit 1	0	Reserved	Reserved
Bit 0	0	Reserved	Reserved

Byte 13

Bit	@Pup	Name	Pin Description
Bit 7	0	Reserved	If Prog_Freq_EN is set, the values programmed in CPU_FSEL_N[6:0] and CPU_FSEL_M[5:0] will be used to determine the CPU output frequency. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used.
Bit 6	0	CPU_FSEL_N6	
Bit 5	0	CPU_FSEL_N5	
Bit 4	0	CPU_FSEL_N4	
Bit 3	0	CPU_FSEL_N3	
Bit 2	0	CPU_FSEL_N2	
Bit 1	0	CPU_FSEL_N1	
Bit 0	0	CPU_FSEL_N0	

Byte 14

Bit	@Pup	Name	Pin Description
Bit 7	0	Pro_Freq_EN	Programmable output frequencies enabled 0 = disabled 1 = enabled
Bit 6	0	Reserved	Reserved
Bit 5	0	CPU_FSEL_M5	If Prog_Freq_EN is set, the values programmed in CPU_FSEL_N[6:0] and CPU_FSEL_M[5:0] will be used to determine the CPU output frequency. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used.
Bit 4	0	CPU_FSEL_M4	
Bit 3	0	CPU_FSEL_M3	
Bit 2	0	CPU_FSEL_M2	
Bit 1	0	CPU_FSEL_M1	
Bit 0	0	CPU_FSEL_M0	

Watchdog Self Recovery Sequence

This feature is designed to allow the system designer to change frequency while the system is running and reboot the operation of the system in case of a hang up due to the frequency change.

When the system sends an SMBus command requesting a frequency change through the Dial-a-Frequency Control Registers, it must have previously sent a command to the Watchdog Timer to select which time out stamp the Watchdog must perform, otherwise the System Self Recovery feature will not be applicable. Consequently, this device will change frequency and then the Watchdog timer starts timing. Meanwhile, the system BIOS is running its operation with the new frequency. If this device receives a new SMBus command to clear the bits originally programmed in the Watchdog Timer bits (reprogram to 0000) before the Watchdog times out, then this device will keep operating in its normal condition with the new selected frequency.

The Watchdog timer will also be triggered if you program the software frequency select bits (FSEL) to a new frequency selection. If the Watchdog times out before the new SMBus reprograms the Watchdog Timer bits to (0000), then this device will send a low system reset pulse, on SRESET# and changes WD Time-out bit to “1.”

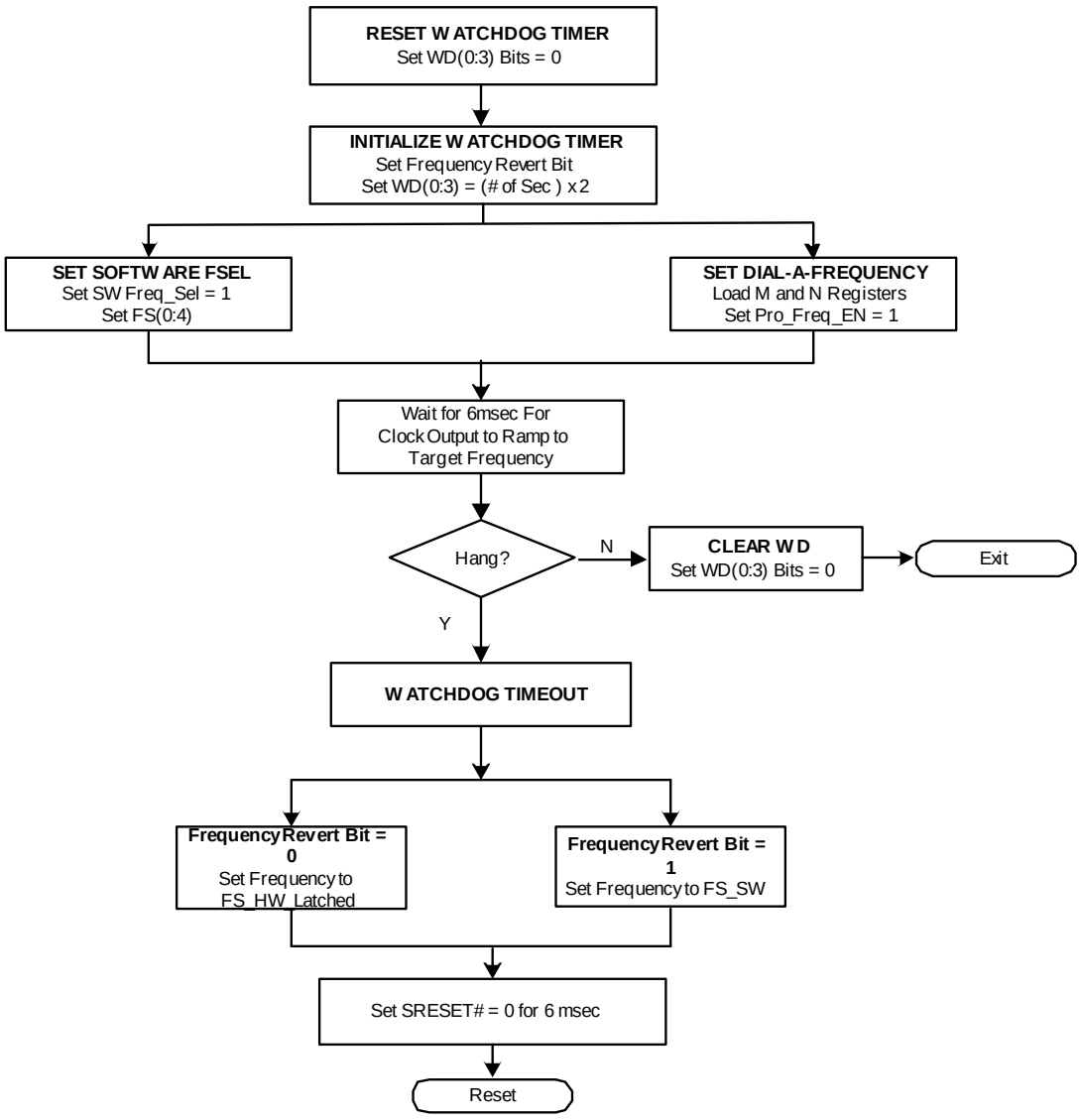


Figure 1. Watchdog Flowchart

Program the CPU output frequency

When the programmable output frequency feature is enabled (Pro_Freq_EN bit is set), the CPU output frequency is determined by the following equation:

Fcpu = G * N/M.

"N" and "M" are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively.

"G" stands for the PLL Gear Constant, which is determined by the programmed value of FS[4:0] or SEL[4:0]. The value is listed in *Table 2*.

The ratio of N and M need to be greater than "1" [N/M> 1].

The following table lists set of N and M values for different frequency output ranges. This example use a fixed value for the M-Value Register and select the CPU output frequency by changing the value of the N-Value Register.

Table 6. Examples of N and M Value for Different CPU Frequency Range

Frequency Ranges	Gear Constants	Fixed Value for M-Value Register	Range of N-Value Register for Different CPU Frequency
66 – 127	47.99750	48	66 – 127
128 – 203	63.99667	40	80 – 127

Table 7. Maximum Lumped Capacitive Output Loads

Clock	Max Load	Units
PCI, PCI_F	20	pF
3V66	30	pF
48M_24MHz, 48MHz	20	pF
REF	30	pF
CPUT/C CPU_ITP	See *Figure 4*	pF

Table 8. Group Timing Relationship and Tolerances

	Offset	Tolerance (or Range)	Conditions	Notes
3V66 to PCI	Typical 2.5 ns	1.5 – 3.5 ns	3V66 leads	See *Note 2*

PD# (Power-down) Clarification

The PD# (Power Down) pin is used to shut off ALL clocks prior to shutting off power to the device. PD# is an asynchronous active LOW input. This signal is synchronized internally to the device powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. When PD# is low, all clocks are driven to a LOW value and held there and the VCO and PLLs are also powered down. All clocks are shut down in a synchronous manner so has not to cause glitches while transitioning to the low “stopped” state.

PD# – Assertion

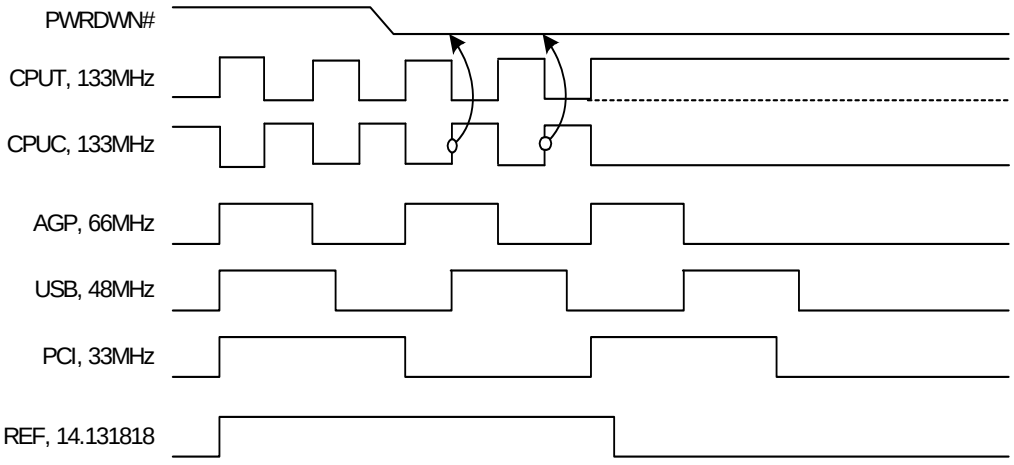


Figure 2. Power-down Assertion Timing Waveforms

PD# – Deassertion

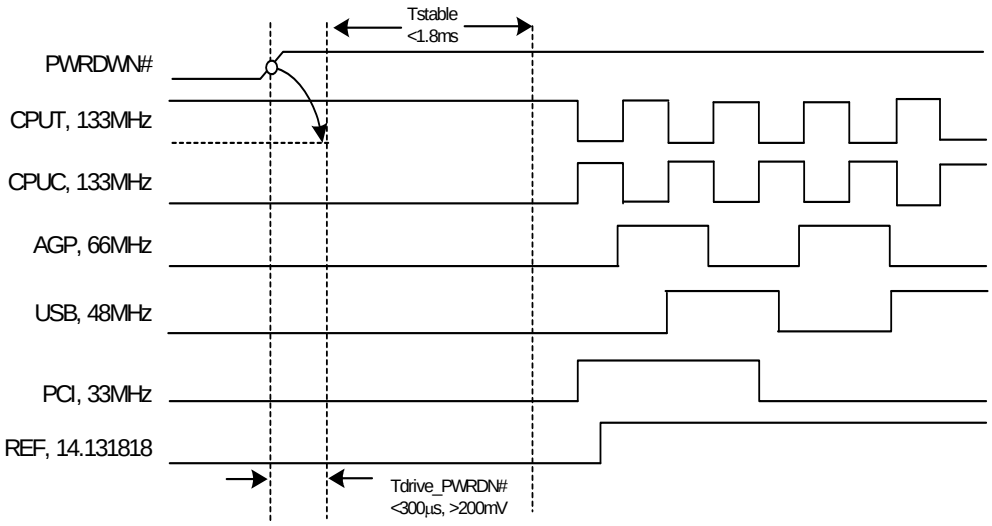


Figure 3. Power-down Deassertion Timing Waveforms

After the clock chip internal PLL is powered up and locked, all outputs will be enabled within a few clock cycles of each other, with the first to last active clock taking no more than two full PCI clock cycles.

Table 9. PWRDWN# Functionality

PWRDWN#	CPUT	CPUC	3V66	PCI_F/PCI	48MHz
1	Normal	Normal	66MHz	3V66/2	48M
0	Iref x2	Float	Low	Low	Low

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–0.5	4.6	V
V_{DDA}	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	0	70	°C
T_J	Temperature, Junction	Functional	–	150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
$Ø_{JC}$	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	15		°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	45		°C/W
UL–94	Flammability Rating	At 1/8 in.	V–0		

DC Electrical Specifications

Parameter	Description	Condition		Min.	Max.	Unit
V_{DD_REF}, V_{DD_PCI}, $V_{DD–CORE}$, V_{DD_3V66}, $V_{DD\_48\ MHz}$, V_{DD_CPU},	3.3V Supply Voltages			3.135	3.465	V
C_{in}	Input Pin Capacitance				5	pF
C_{XTAL}	XTAL Pin Capacitance				22.5	pF
C_L	Max. Capacitive Load on 48MHz, REF PCICLK, 3V66				2030	pF
$f_{(REF)}$	Reference Frequency Oscillator Nominal Value			14.318	14.318	MHz
V_{IH}	High-level Input Voltage	Except Crystal Pads. Threshold voltage for crystal pads = $V_{DD}/2$		2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Pads			0.8	V
V_{OH}	High-level Output Voltage	48MHz, REF, 3V66	I_{OH} = –1 mA	2.4		V
		PCI	I_{OH} = –1 mA	2.4		V
V_{OL}	Low-level Output Voltage	48MHz, REF, 3V66	I_{OL} = 1 mA		0.4	V
		PCI	I_{OL} = 1 mA		0.55	V
I_{IH}	Input High Current	$0 \le V_{IN} \le V_{DD}$		–5	5	mA
I_{IL}	Input Low Current	$0 \le V_{IN} \le V_{DD}$		–5	5	mA
I_{OH}	High-level Output Current	CPU For I_{OH} =6*IRef Configuration	Type X1, V_{OH} = 0.65V	12.9		mA
			Type X1, V_{OH} = 0.74V		14.9	
		REF, 48 MHz	Type 3, V_{OH} = 1.00V	–29		
			Type 3, V_{OH} = 3.135V		–23	
		3V66, PCI	Type 5, V_{OH} = 1.00V	–33		
			Type 5, V_{OH} = 3.135V		–33	
I_{OL}	Low-level Output Current	REF, 48MHz	Type 3, V_{OL} = 1.95V	29		mA
			Type 3, V_{OL} = 0.4V		27	
		3V66, PCI,	Type 5, V_{OL} =1.95 V	30		
			Type 5, V_{OL} = 0.4V		38	
I_{OZ}	Output Leakage Current	Three-state			10	mA
I_{DD3}	3.3V Power Supply Current	V_{DD_CORE}/V_{DD33} = 3.465V, F_{CPU} = 133 MHz			250	mA

DC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
I_{DDPD3}	3.3V Shutdown Current	V_{DD_CORE}/V_{DDQ3} = 3.465V		25	mA

AC Electrical Specifications[2]

Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t_1	All	Output Duty Cycle[3]	$t_{1A}/(t_{1B})$	45	55	%
t_2	CPUT/C	Rise Time	Measured at 20% to 80% of V_{oh}	175	800	ps
t_2	48MHz, REF	Rising Edge Rate	Between 0.4V and 2.4V	0.5	2.0	V/ns
t_2	PCI, 3V66,	Rising Edge Rate	Between 0.4V and 2.4V	1.0	4.0	V/ns
t_3	CPUT/C	Fall Time	Measured at 80% to 20% of V_{oh}	175	800	ps
t_3	48MHz, REF	Falling Edge Rate	Between 2.4V and 0.4V	0.5	2.0	V/ns
t_3	PCI, 3V66	Falling Edge Rate	Between 2.4V and 0.4V	0.7	4.0	V/ns
t_4	CPUT/C	CPU-CPU Skew	Measured at Crossover		150	ps
t_5	3V66 [0:1]	3V66-3V66 Skew	Measured at 1.5V		500	ps
t_6	PCI	PCI-PCI Skew	Measured at 1.5V		500	ps
t_7	3V66,PCI	3V66-PCI Clock Skew	3V66 leads. Measured at 1.5V	1.0	4.5	ns
t_8	CPUT/C	Cycle-Cycle Clock Jitter	Measured at Crossover $t_8 = t_{8A} - t_{8B}$ with all outputs running		600	ps
t_9	3V66	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		600	ps
t_9	48MHz	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		600	ps
t_9	PCI	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		600	ps
t_9	REF	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		1000	ps
	CPUT/C, PCI	Settle Time	CPU and PCI clock stabilization from power-up		3	ms
t_{RFM}	CPUT/C	Rise/Fall Matching	Measured with test loads[4, 5]		30	
V_{OVS}	CPUT/C	Overshoot	Measured with test loads[5]		V_{oh} + 0.2	V
V_{UDS}	CPUT/C	Undershoot	Measured with test loads[5]	–0.2		V
V_{OH}	CPUT/C	High-level Output Voltage	Measured with test loads[5]	0.65	0.74	V
V_{OL}	CPUT/C	Low-level Output Voltage	Measured with test loads[5]	0.0	0.05	V
V_{OX}	CPUT/C	Crossover Voltage	Measured with test loads[5]	250	550	mv

Notes:
2. All parameters specified with loaded outputs.
3. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.
4. Determined as a fraction of 2*(Trp – Trn)/(Trp +Trn) Where Trp is a rising edge and Trp is an intersecting falling edge.
5. The test load is R_s = 33.2W, R_p = 49.9W in test circuit.

Test and Measurement Set-up

For Differential CPU Output Signals

The following diagram shows lumped test load configurations for the differential Host Clock Outputs.

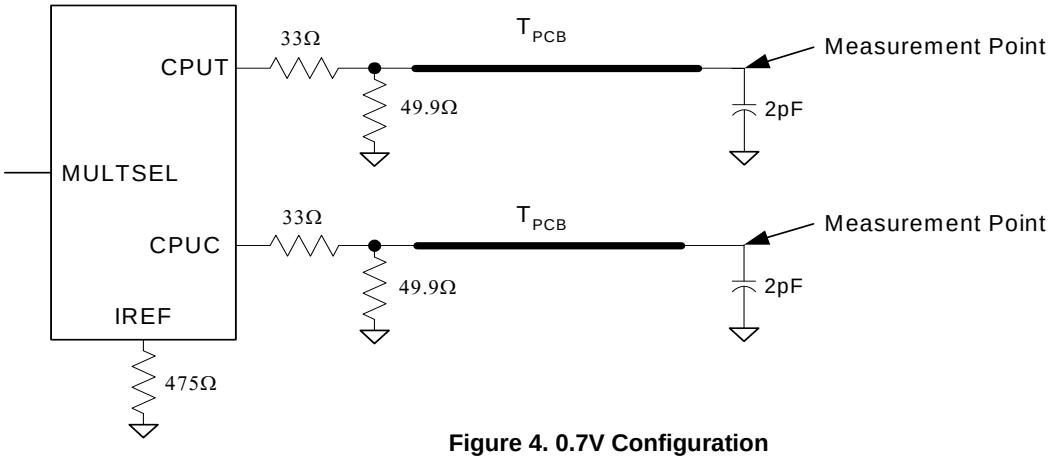
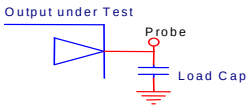


Figure 4. 0.7V Configuration



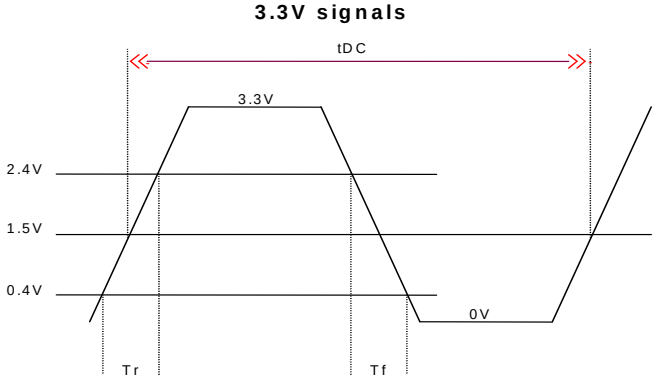


Figure 5. Lumped Load For Single-Ended Output Signals (for AC Parameters Measurement)

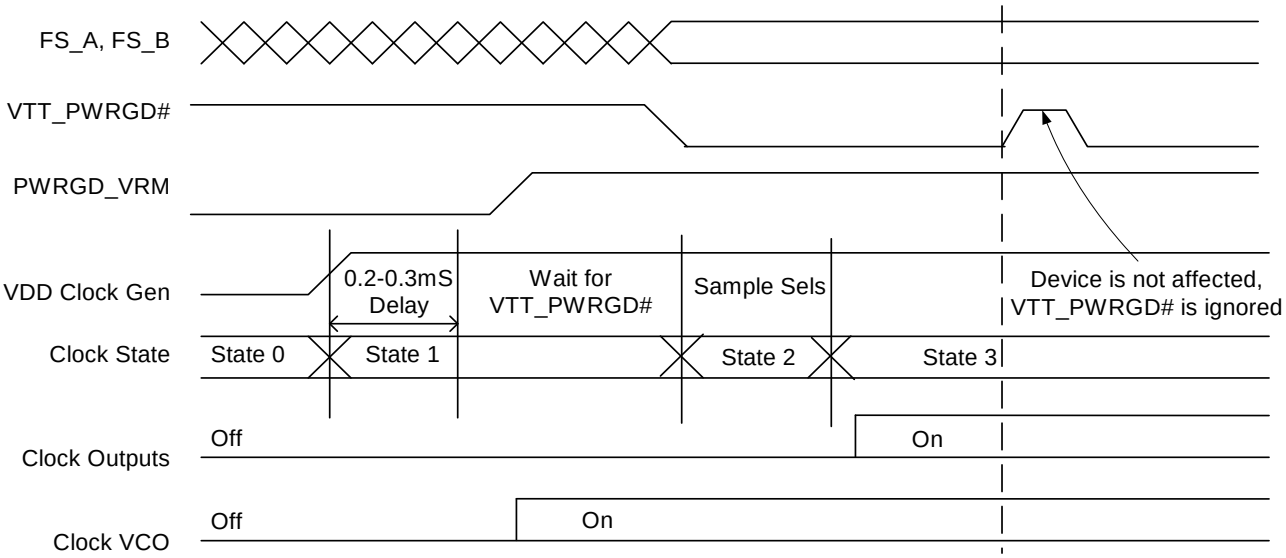


Figure 6. VTT_PWRGD# Timing Diagram[6]

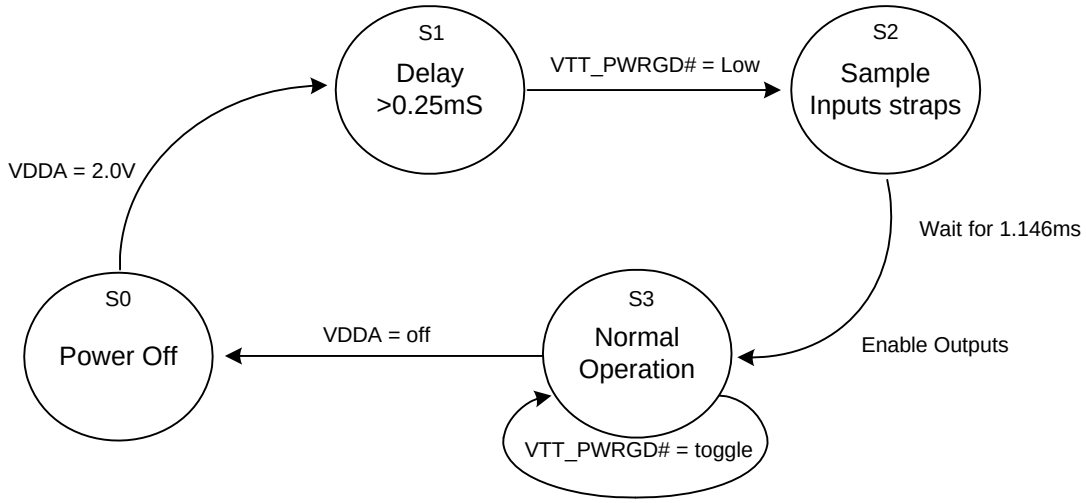
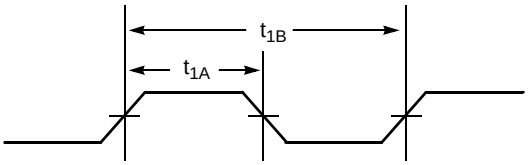


Figure 7. Clock Generator Power-up/Run State Diagram

Switching Waveforms

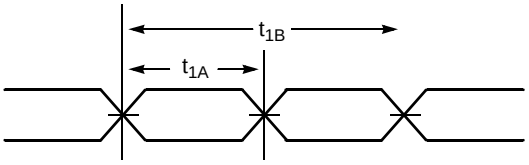
Duty Cycle Timing (Single-ended Output)



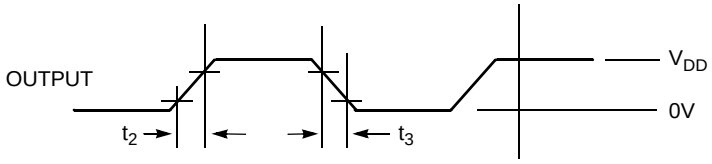
Note:
6. Device is not affected, VTT_PWRGD# is ignored.

Switching Waveforms (continued)

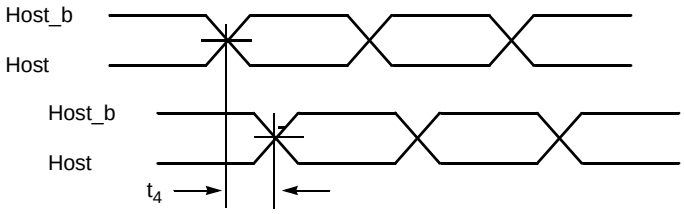
Duty Cycle Timing (CPU Differential Output)



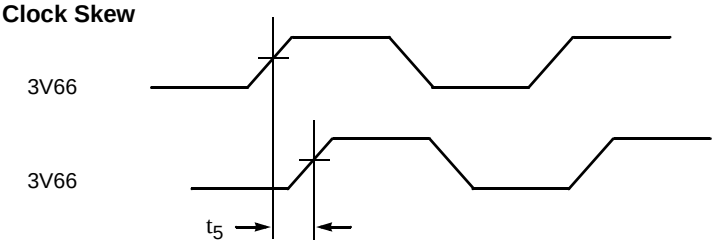
All Outputs Rise/Fall Time



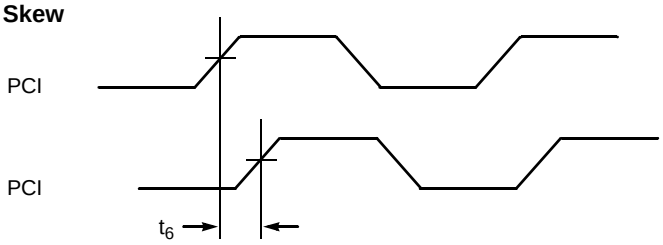
CPU-CPU Clock Skew



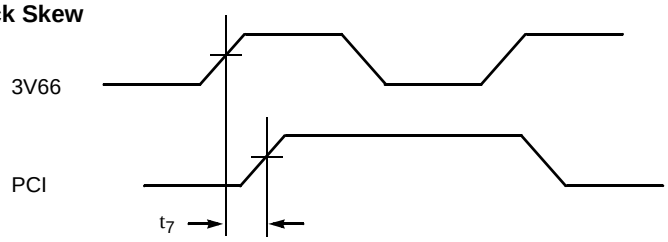
3V66-3V66 Clock Skew



PCI-PCI Clock Skew

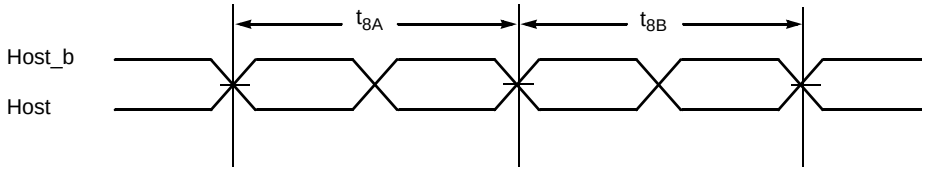


3V66-PCI Clock Skew

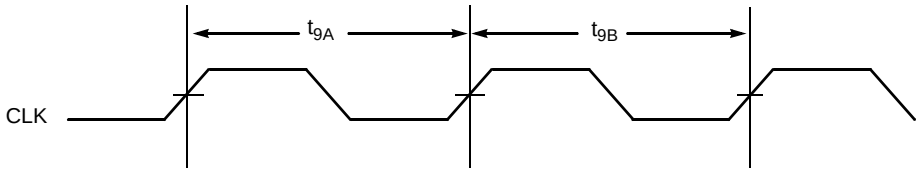


Switching Waveforms (continued)

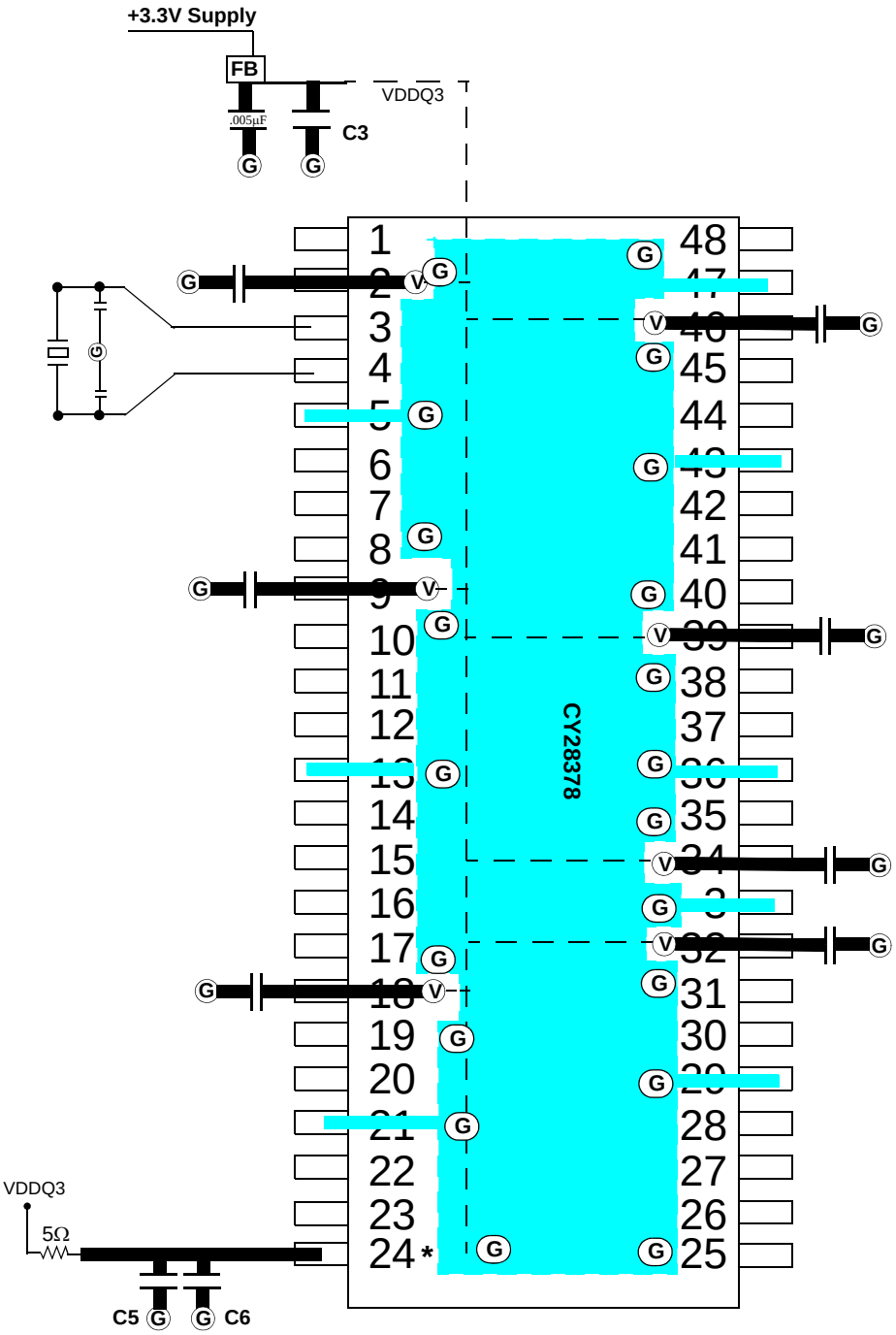
CPU Clock Cycle-Cycle Jitter



Cycle-Cycle Clock Jitter



Layout Example



FB = Dale ILB1206 - 300 (300 Ω @ 100 MHz)

Cermaic Caps C3 = 10 - 22 µF C4 = .005 µF C5 = 10µF C6 = .1µF

(G) = VIA to GND plane layer (V) =VIA to respective supply plane layer

Note: Each supply plane or strip should have a **ferrite bead and capacitors**
All bypass caps = .1µf ceramic
***** For use with onboard video using 48 MHz for Dot Clock or connect to VDDQ3

Ordering Information

Ordering Code	Package Type	Operating Range
CY28378OC	48-pin Small Shrunk Outline Package (SSOP)	Commercial, 0°C to 70°C
CY28378OCT	48-pin Small Shrunk Outline Package (SSOP) –Tape and Reel	Commercial, 0°C to 70°C

Package Diagram

48-Lead Shrunk Small Outline Package O48