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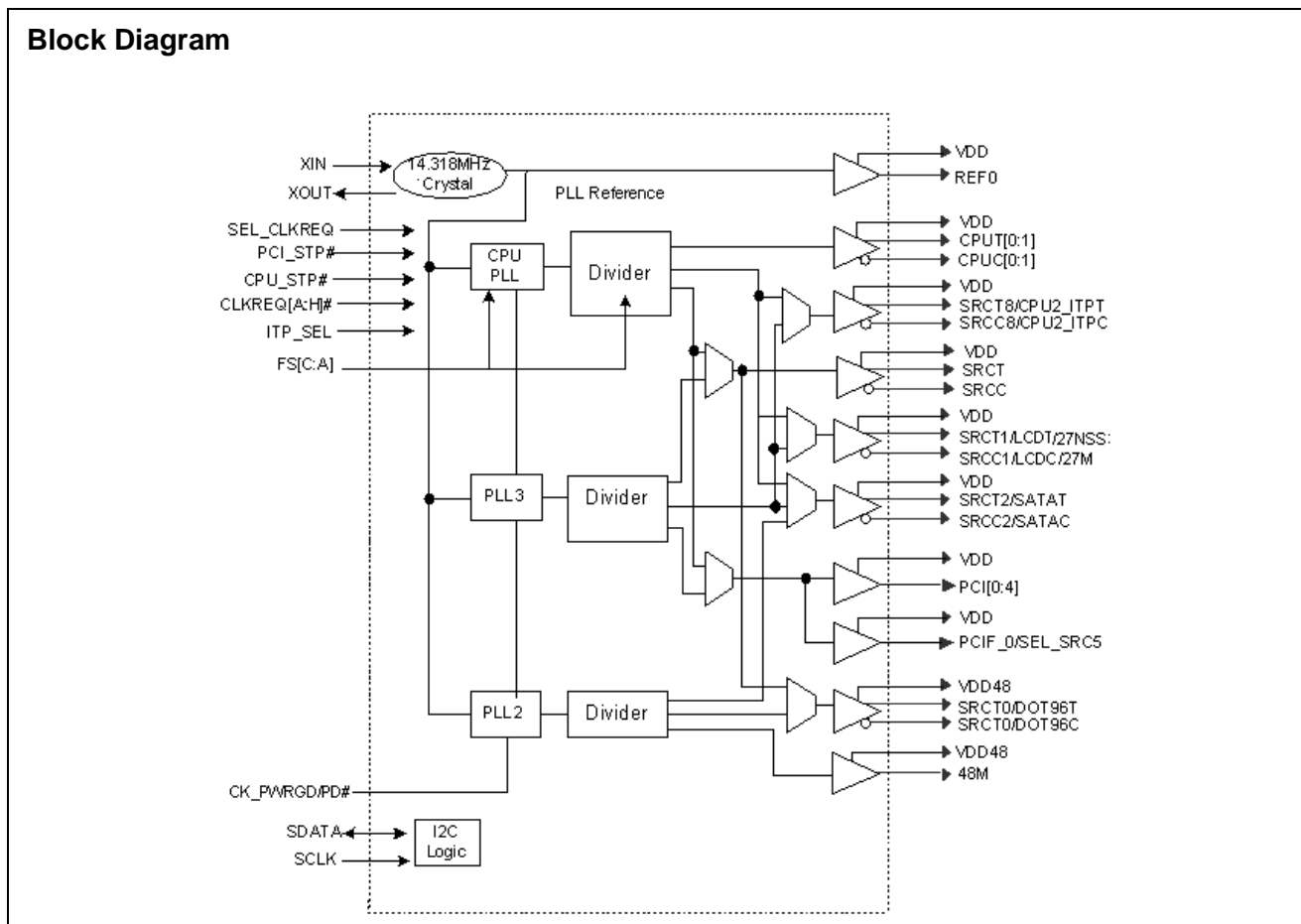
Clock Generator for Intel® Crestline Chipset

Features

- Compliant to Intel® CK505
- Low power push-pull type differential output buffers
- Integrated voltage regulator
- Integrated resistors on differential clocks
- Scalable low voltage VDD_IO (3.3V to 1.25V)
- Differential CPU clocks with selectable frequency
- 100 MHz Differential SRC clocks
- 100 MHz Differential LCD clock
- 96 MHz Differential DOT clock
- 48 MHz USB clocks
- 33 MHz PCI clock
- 27 MHz Video clocks
- Buffered Reference Clock 14.318 MHz
- Low-voltage frequency select input
- I²C support with readback capabilities
- Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V Power supply
- 64-pin QFN/TSSOP packages

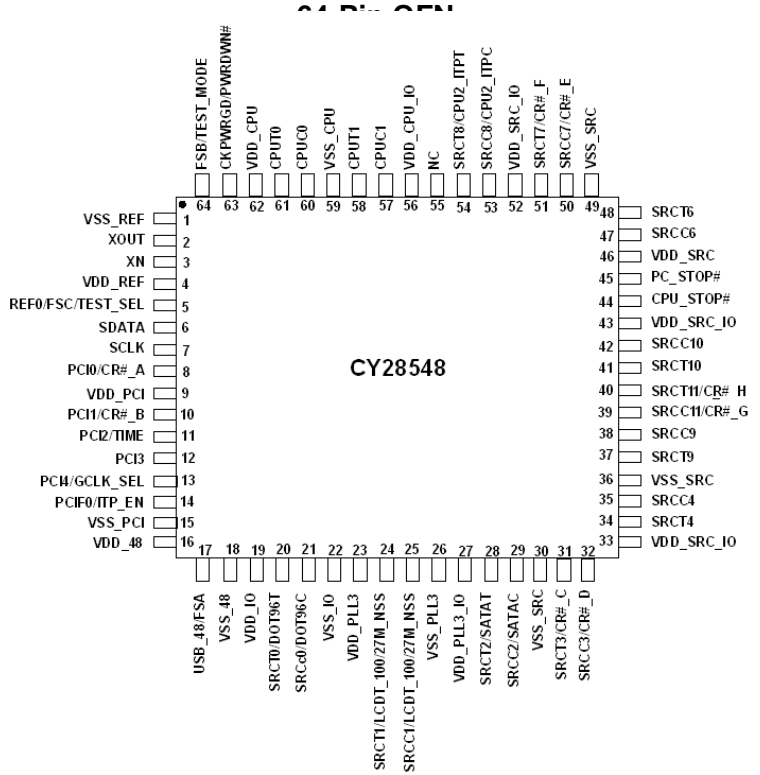
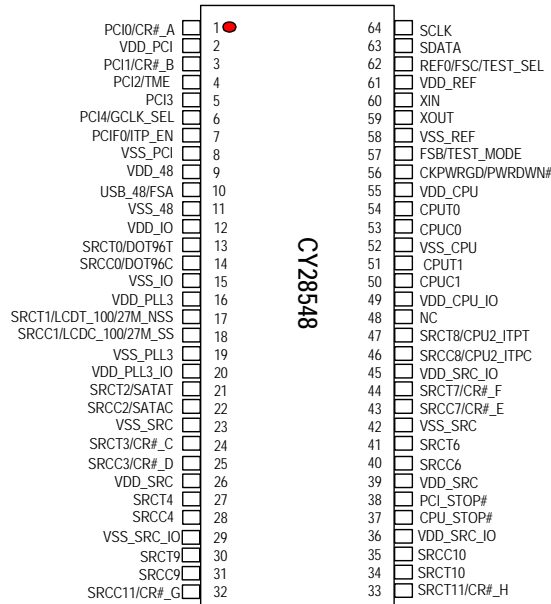
| CPU | SRC | PCI | REF | DOT96 | USB_48 | LCD | 27M |
|---------|-------|-----|-----|-------|--------|-----|-----|
| x2 / x3 | x7/11 | x6 | x 1 | x 1 | x 1 | x1 | x2 |

Block Diagram



Pin Configuration

64-Pin TSSOP



QFN Pin Definitions

| Pin No. | Name | Type | Description |
|---------|-----------------------|-------|---|
| 1 | VSS_REF | GND | Ground for outputs. |
| 2 | Xout | O, SE | 14.318 MHz Crystal output. |
| 3 | Xin | I | 14.318 MHz Crystal input. |
| 4 | VDD_REF | PWR | 3.3V Power supply for outputs and maintains SMBUS registers during power down. |
| 5 | REF0 / FSC / TEST_SEL | I/O | Fixed 14.318 clock output/3.3V-tolerant input for CPU frequency selection/ Selects test mode if pulled to V _{IHFS_C} when CK_PWRGD is asserted HIGH. Refer to DC Electrical Specifications table for V _{ILFS_C} , V _{IMFS_C} , V _{IHFS_C} specifications. |
| 6 | SDATA | I/O | SMBus compatible SDATA. |
| 7 | SCLK | I | SMBus compatible SCLOCK. |

QFN Pin Definitions (continued)

| Pin No. | Name | Type | Description | | | | | | | | | | | | | | | |
|----------|--------------------------|------------|--|----------------|--------|--------|--------|--------|---|--------|--------|----------------|----------------|---|-------|-------|---------|--------|
| 8 | PCI0 / CR#_A | I/O, SE | <p>33 MHz Clock/3.3V Clock Request # Input Mappable via I2C to control either SRC 0 or SRC 2. Default PCI0. To configure this pin to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_A_EN bit located in byte 5 bit 7, first disable PCI output (Hi-z) in byte 2, bit 1. 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6: 0 = CR#_A controls SRC0 pair (default) 1 = CR#_A controls SRC2 pair</p> | | | | | | | | | | | | | | | |
| 9 | VDD_PCI | PWR | 3.3V power supply for PCI PLL | | | | | | | | | | | | | | | |
| 10 | PCI1 / CR#_B | I/O, SE | <p>33 MHz Clock/3.3V Clock Request # Input Mappable via I2C to control either SRC 1 or SRC 4. Default PCI1. To configure this pin to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_B_EN bit located in byte 5, bit 5, first disable PCI output (Hi-z) in byte 2, bit 1. 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 4 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4: 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair</p> | | | | | | | | | | | | | | | |
| 11 | PCI2 / TME | I/O, SE | <p>33 MHz Clock output/3.3V-tolerance input for enabling Trusted Mode Sampled at CKPWRGD assertion: 0 = Normal mode, 1 = Trusted mode (no overclocking)</p> | | | | | | | | | | | | | | | |
| 12 | PCI3 | O, SE | 33 MHz Clock output | | | | | | | | | | | | | | | |
| 13 | PCI4 / GCLK_SEL | I/O, SE | <p>33 MHz Clock output/3.3V-tolerant input for selecting graphic clock source on pin 20, 21, 24 and 25 Sampled on CKPWRGD assertion;</p> <table border="1" data-bbox="678 1171 1409 1283"> <thead> <tr> <th>GCLK_SEL</th> <th>Pin 20</th> <th>Pin 21</th> <th>Pin 24</th> <th>Pin 25</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DOT96T</td> <td>DOT96C</td> <td>SRC1T/LCD_100T</td> <td>SRC1C/LCD_100C</td> </tr> <tr> <td>1</td> <td>SRCT0</td> <td>SRCC0</td> <td>27M_NSS</td> <td>27M_SS</td> </tr> </tbody> </table> | GCLK_SEL | Pin 20 | Pin 21 | Pin 24 | Pin 25 | 0 | DOT96T | DOT96C | SRC1T/LCD_100T | SRC1C/LCD_100C | 1 | SRCT0 | SRCC0 | 27M_NSS | 27M_SS |
| GCLK_SEL | Pin 20 | Pin 21 | Pin 24 | Pin 25 | | | | | | | | | | | | | | |
| 0 | DOT96T | DOT96C | SRC1T/LCD_100T | SRC1C/LCD_100C | | | | | | | | | | | | | | |
| 1 | SRCT0 | SRCC0 | 27M_NSS | 27M_SS | | | | | | | | | | | | | | |
| 14 | PCIF0 / ITP_EN | I/O, SE | <p>33 MHz free running clock output/3.3V LVTTTL input to enable SRC8 or CPU2_ITP (sampled on the CKPWRGD assertion) 1 = CPU2_ITP, 0 = SRC8</p> | | | | | | | | | | | | | | | |
| 15 | VSS_PCI | GND | Ground for outputs. | | | | | | | | | | | | | | | |
| 16 | VDD_48 | PWR | 3.3V power supply for outputs and PLL. | | | | | | | | | | | | | | | |
| 17 | USB_48 / FSA | I/O | Fixed 48 MHz clock output/3.3V-tolerant input for CPU frequency selection Refer to DC Electrical Specifications table for V _{il_FS} and V _{ih_FS} specifications. | | | | | | | | | | | | | | | |
| 18 | VSS_48 | GND | Ground for outputs. | | | | | | | | | | | | | | | |
| 19 | VDD_IO | PWR | 3.3V-1.25V power supply for outputs | | | | | | | | | | | | | | | |
| 20 | SRCT0 / DOT96T | O, DIF | True 100 MHz Differential serial reference clocks/Fixed True 96 MHz clock output. Selected via GCLK_SEL at CKPWRGD assertion | | | | | | | | | | | | | | | |
| 21 | SRCC0 / DOT96C | O, DIF | Complementary 100 MHz Differential serial reference clocks/Fixed complement 96 MHz clock output. Selected via GCLK_SEL at CKPWRGD assertion | | | | | | | | | | | | | | | |
| 22 | VSS_IO | GND | Ground for outputs. | | | | | | | | | | | | | | | |
| 23 | VDD_PLL3 | PWR | 3.3V Power supply for PLL3. | | | | | | | | | | | | | | | |
| 24 | SRCT1 / LCDT_100/27M_NSS | O, DIF, SE | True 100 MHz differential serial reference clock output/True 100 MHz LCD video clock output / Non spread 27-MHz video clock output. Selected via GCLK_SEL at CKPWRGD assertion. | | | | | | | | | | | | | | | |

QFN Pin Definitions (continued)

| Pin No. | Name | Type | Description |
|---------|-----------------------------|---------------|--|
| 25 | SRCC1 / LCD_C_100/27M_SS | O, DIF, SE | Complementary 100 MHz differential serial reference clock output/Complementary 100 MHz LCD video clock output /Spread 27 MHz video clock output. Selected via GCLK_SEL at CKPWRGD assertion. |
| 26 | VSS_PLL3 | GND | Ground for PLL3. |
| 27 | VDD_PLL3_IO | PWR | 3.3V-1.25V power supply for outputs. |
| 28 | SRCT2 / SATAT | O, DIF | True 100 MHz differential serial reference clock output. |
| 29 | SRCC2 / SATAC | O, DIF | Complementary 100 MHz differential serial reference clock output. |
| 30 | VSS_SRC | GND | Ground for outputs. |
| 31 | SRCT3 / CR#_C | I/O, DIF | True 100 MHz differential serial reference clock output /3.3V Clock Request #_C/D input Selected via CR#_C_EN/CR#_D_EN bit located in byte 5 bit 3and 1. The CR#_C_SEL and CR#_D_SEL bits in byte 5 bit 2 and 0 will select which SRC to stop when asserted |
| 32 | SRCC3 / CR#_D | I/O, DIF | Complementary 100 MHz differential serial reference clock output/3.3V Clock Request #_C/D input Selected via CR#_C_EN/CR#_D_EN bit located in byte 5 bit 3and 1. The CR#_C_SEL and CR#_D_SEL bits in byte 5 bit 2 and 0 will select which SRC to stop when asserted |
| 33 | VDD_SRC_IO | PWR | 3.3V-1.25V Power supply for outputs. |
| 34 | SRCT4 | O, DIF | True 100 MHz differential serial reference clocks. |
| 35 | SRCC4 | O, DIF | Complementary 100 MHz differential serial reference clocks. |
| 36 | VSS_SRC | GND | Ground for outputs. |
| 37 | SRCT9 | O, DIF | True 100 MHz differential serial reference clocks. |
| 38 | SRCC9 | O, DIF | Complementary 100 MHz differential serial reference clocks. |
| 39 | SRCC11/ CR#_G | I/O, DIF | True 100 MHz differential serial reference clocks/3.3V CR#_G Input. Selected via CR#_G_EN/CR#_H_EN bit located in byte 6 bit 5 and 4. When selected, CR#_G controls SRC9, CR#_H controls SRC10 |
| 40 | SRCT11/ CR#_H | I/O, DIF | Complementary 100 MHz Differential serial reference clocks/3.3V CR#_H Input. Selected via CR#_G_EN/CR#_H_EN bit located in byte 6 bit 5 and 4. When selected, CR#_G controls SRC9, CR#_H controls SRC10 |
| 41 | SRCT10 | O, DIF | True 100 MHz Differential serial reference clocks. |
| 42 | SRCC10 | O, DIF | Complementary 100 MHz Differential serial reference clocks. |
| 43 | VDD_SRC_IO | PWR | 3.3V-1.25V power supply for outputs. |
| 44 | CPU_STOP# | I | 3.3V-tolerant input for stopping CPU outputs During direct clock off to M1 mode transition, a serial load of BSEL data is driven on CPU_STOP# and sampled on the rising edge of PCI_STOP#. See <i>Figure 13</i> for more information. |
| 45 | PCI_STOP# | I | 3.3V-tolerant input for stopping PCI and SRC outputs During direct clock off to M1 mode transition, a serial load of BSEL data is driven on CPU_STOP# and sampled on the rising edge of PCI_STOP#. See <i>Figure 13</i> for more information. |
| 46 | VDD_SRC | PWR | 3.3V power supply for SRC PLL. |
| 47 | SRCC6 | O, DIF | Complementary 100 MHz Differential serial reference clocks. |
| 48 | SRCT6 | O, DIF | True 100 MHz Differential serial reference clocks. |
| 49 | VSS_SRC | GND | Ground for outputs. |
| 50 | SRCC7/ CR#_E | I/O, DIF | Complementary 100 MHz differential serial reference clocks/3.3V CR#_E Input. Selected via CR#_E_EN/CR#_F_EN bit located in byte 6 bit 7 and 6. When selected, CR#_E controls SRC6, CR#_F controls SRC8 |

QFN Pin Definitions (continued)

| Pin No. | Name | Type | Description |
|---------|--------------------|----------|---|
| 51 | SRCT7/ CR#_F | I/O, DIF | True 100 MHz differential serial reference clocks/3.3V CR#_F Input. Selected via CR#_E_EN/CR#_F_EN bit located in byte 6 bit 7 and 6. When selected, CR#_E controls SRC6, CR#_F controls SRC8 |
| 52 | VDD_SRC_IO | PWR | 3.3V-1.25V Power supply for outputs. |
| 53 | SRCC8 / CPUC2_ITP | O, DIF | Selectable complementary differential CPU or SRC clock output. ITP_EN = 0 @ CK_PWRGD assertion = SRC8 ITP_EN = 1 @ CK_PWRGD assertion = CPU2 |
| 54 | SRCT8 / CPUT2_ITP, | O, DIF | Selectable True differential CPU or SRC clock output. ITP_EN = 0 @ CK_PWRGD assertion = SRC8 ITP_EN = 1 @ CK_PWRGD assertion = CPU2 |
| 55 | NC | NC | No connect. |
| 56 | VDD_CPU_IO | PWR | 3.3V-1.25V Power supply for outputs. |
| 57 | CPUC1 | O, DIF | Complementary differential CPU clock outputs. Note that CPU1 is the iAMT clock and is on in that mode. |
| 58 | CPUT1 | O, DIF | True differential CPU clock outputs. Note that CPU1 is the iAMT clock and is on in that mode. |
| 59 | VSS_CPU | GND | Ground for outputs. |
| 60 | CPUC0 | O, DIF | Complement differential CPU clock outputs. |
| 61 | CPUT0 | O, DIF | True differential CPU clock outputs. |
| 62 | VDD_CPU | PWR | 3.3V Power supply for CPU PLL. |
| 63 | CKPWRGD / PWRDWN# | I | 3.3V LVTTTL input. This pin is a level sensitive strobe used to latch the FS_A, FS_B, FS_C, GLCK_SEL and ITP_EN. After CKPWRGD (active HIGH) assertion, this pin becomes a real-time input for asserting power down (active LOW). |
| 64 | FSB / TEST_MODE | I | 3.3V-tolerant input for CPU frequency selection / Selects Ref/N or Tri-state when in test mode. 0 = Tri-state, 1 = Ref/N Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications. |

TSSOP Pin Definitions

| Pin No. | Name | Type | Description |
|---------|--------------|---------|---|
| 1 | PCI0 / CR#_A | I/O, SE | 33 MHz clock/3.3V Clock Request # Input. Selected via CR#_A_EN bit located in byte 5 bit 7. The CR#_A_SEL bit in byte 5 bit 6 will select to control SRC0 or SRC2 when asserted. |
| 2 | VDD_PCI | PWR | 3.3V Power supply for PCI PLL. |
| 3 | PCI1 / CR#_B | I/O, SE | 33 MHz Clock/3.3V Clock Request # Input. Selected via CR#_B_EN bit located in byte 5 bit 5. The CR#_B_SEL bit in byte 5 bit 4 will select to control SRC1 or SRC4 when asserted. |
| 4 | PCI2 / TME | I/O, SE | 33 MHz clock output / 3.3V-tolerance input for enabling trusted mode Sampled at CKPWRGD assertion: 0 = Normal mode, 1 = Trusted mode (no overclocking) |
| 5 | PCI3 | O, SE | 33 MHz clock output |

TSSOP Pin Definitions (continued)

| Pin No. | Name | Type | Description | | | | | | | | | | | | | | | |
|----------|--------------------------|------------|--|----------------|-------|-------|-------|--------|---|--------|--------|----------------|----------------|---|-------|-------|---------|--------|
| 6 | PCI4 / GCLK_SEL | I/O, SE | <p>33 MHz clock output/3.3V-tolerant input for selecting graphic clock source on pin 13, 14, 17 and 18 Sampled on CKPWRGD assertion</p> <table border="1" data-bbox="711 411 1398 516"> <thead> <tr> <th>GCLK_SEL</th> <th>Pin13</th> <th>Pin14</th> <th>Pin17</th> <th>Pin 18</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DOT96T</td> <td>DOT96C</td> <td>SRC1T/LCD_100T</td> <td>SRC1C/LCD_100C</td> </tr> <tr> <td>1</td> <td>SRCT0</td> <td>SRCC0</td> <td>27M_NSS</td> <td>27M_SS</td> </tr> </tbody> </table> | GCLK_SEL | Pin13 | Pin14 | Pin17 | Pin 18 | 0 | DOT96T | DOT96C | SRC1T/LCD_100T | SRC1C/LCD_100C | 1 | SRCT0 | SRCC0 | 27M_NSS | 27M_SS |
| GCLK_SEL | Pin13 | Pin14 | Pin17 | Pin 18 | | | | | | | | | | | | | | |
| 0 | DOT96T | DOT96C | SRC1T/LCD_100T | SRC1C/LCD_100C | | | | | | | | | | | | | | |
| 1 | SRCT0 | SRCC0 | 27M_NSS | 27M_SS | | | | | | | | | | | | | | |
| 7 | PCIF0 / ITP_EN | I/O, SE | <p>33 MHz free running clock output / 3.3V LVTTTL input to enable SRC8 or CPU2_ITP (sampled on the CKPWRGD assertion) 1 = CPU2_ITP, 0 = SRC8</p> | | | | | | | | | | | | | | | |
| 8 | VSS_PCI | GND | Ground for outputs. | | | | | | | | | | | | | | | |
| 9 | VDD_48 | PWR | 3.3V power supply for outputs and PLL. | | | | | | | | | | | | | | | |
| 10 | USB_48 / FSA | I/O | Fixed 48 MHz clock output / 3.3V-tolerant input for CPU frequency selection Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications. | | | | | | | | | | | | | | | |
| 11 | VSS_48 | GND | Ground for outputs. | | | | | | | | | | | | | | | |
| 12 | VDD_IO | PWR | 3.3V-1.25V power supply for outputs | | | | | | | | | | | | | | | |
| 13 | SRCT0 / DOT96T | O, DIF | True 100 MHz differential serial reference clocks / Fixed True 96 MHz clock output. Selected via GCLK_SEL at CKPWRGD assertion | | | | | | | | | | | | | | | |
| 14 | SRCC0 / DOT96C | O, DIF | Complementary 100 MHz differential serial reference clocks / Fixed Complementary 96 MHz clock output. Selected via GCLK_SEL at CKPWRGD assertion | | | | | | | | | | | | | | | |
| 15 | VSS_IO | GND | Ground for outputs | | | | | | | | | | | | | | | |
| 16 | VDD_PLL3 | PWR | 3.3V Power supply for PLL3 | | | | | | | | | | | | | | | |
| 17 | SRCT1 / LCDT_100/27M_NSS | O, DIF, SE | True 100 MHz differential serial reference clock output / True 100 MHz LCD video clock output / Non spread 27 MHz video clock output. Selected via GCLK_SEL at CKPWRGD assertion | | | | | | | | | | | | | | | |
| 18 | SRCC1 / LCDC_100/27M_SS | O, DIF, SE | Complementary 100 MHz differential serial reference clock output / Complementary 100 MHz LCD video clock output / Spread 27 MHz video clock output. Selected via GCLK_SEL at CKPWRGD assertion | | | | | | | | | | | | | | | |
| 19 | VSS_PLL3 | GND | Ground for PLL3. | | | | | | | | | | | | | | | |
| 20 | VDD_PLL3_IO | PWR | 3.3V-1.25V power supply for outputs. | | | | | | | | | | | | | | | |
| 21 | SRCT2 / SATAT | O, DIF | True 100 MHz differential serial reference clock output. | | | | | | | | | | | | | | | |
| 22 | SRCC2 / SATAC | O, DIF | Complementary 100 MHz differential serial reference clock output. | | | | | | | | | | | | | | | |
| 23 | VSS_SRC | GND | Ground for outputs. | | | | | | | | | | | | | | | |
| 24 | SRCT3 / CR#_C | I/O, DIF | True 100 MHz differential serial reference clock output / 3.3V CR #_C/D input Selected via CR#_C_EN/CR#_D_EN bit located in byte 5 bit 3 and 1. The CR#_C_SEL and CR#_D_SEL bits in byte 5 bit 2 and 0 will select which SRC to stop when asserted | | | | | | | | | | | | | | | |
| 25 | SRCC3 / CR#_D | I/O, DIF | Complementary 100 MHz differential serial reference clock output / 3.3V CR #_C/D input Selected via CR#_C_EN/CR#_D_EN bit located in byte 5 bit 3 and 1. The CR#_C_SEL and CR#_D_SEL bits in byte 5 bit 2 and 0 will select which SRC to stop when asserted | | | | | | | | | | | | | | | |
| 26 | VDD_SRC_IO | PWR | 3.3V-1.25V power supply for outputs. | | | | | | | | | | | | | | | |
| 27 | SRCT4 | O, DIF | True 100 MHz differential serial reference clocks. | | | | | | | | | | | | | | | |
| 28 | SRCC4 | O, DIF | Complementary 100 MHz differential serial reference clocks. | | | | | | | | | | | | | | | |
| 29 | VSS_SRC | GND | Ground for outputs. | | | | | | | | | | | | | | | |
| 30 | SRCT9 | O, DIF | True 100 MHz differential serial reference clocks. | | | | | | | | | | | | | | | |
| 31 | SRCC9 | O, DIF | Complementary 100 MHz differential serial reference clocks. | | | | | | | | | | | | | | | |

TSSOP Pin Definitions (continued)

| Pin No. | Name | Type | Description |
|---------|-------------------|----------|---|
| 32 | SRCC11/ CR#_G | I/O, DIF | Complementary 100 MHz differential serial reference clocks/3.3V CR#_G Input Selected via CR#_G_EN/CR#_H_EN bit located in byte 6 bit 5 and 4. When selected, CR#_G controls SRC9, CR#_H controls SRC10 |
| 33 | SRCT11/ CR#_H | I/O, DIF | True 100 MHz differential serial reference clocks/3.3V CR#_H Input Selected via CR#_G_EN/CR#_H_EN bit located in byte 6 bit 5 and 4. When selected, CR#_G controls SRC9, CR#_H controls SRC10 |
| 34 | SRCT10 | O, DIF | True 100 MHz differential serial reference clocks. |
| 35 | SRCC10 | O, DIF | Complementary 100 MHz differential serial reference clocks. |
| 36 | VDD_SRC_IO | PWR | 3.3V-1.25V Power supply for outputs. |
| 37 | CPU_STOP# | I | 3.3V-tolerant input for stopping CPU outputs During direct clock off to M1 mode transition, a serial load of BSEL data is driven on CPU_STOP# and sampled on the rising edge of PCI_STOP#. See <i>Figure 13</i> for more information. |
| 38 | PCI_STOP# | I | 3.3V-tolerant input for stopping PCI and SRC outputs During direct clock off to M1 mode transition, a serial load of BSEL data is driven on CPU_STOP# and sampled on the rising edge of PCI_STOP#. See <i>Figure 13</i> for more information. |
| 39 | VDD_SRC | PWR | 3.3V Power supply for SRC PLL. |
| 40 | SRCC6 | O, DIF | Complementary 100 MHz differential serial reference clocks. |
| 41 | SRCT6 | O, DIF | True 100 MHz differential serial reference clocks. |
| 42 | VSS_SRC | GND | Ground for outputs. |
| 43 | SRCC7/ CR#_E | I/O, DIF | Complementary 100 MHz differential serial reference clocks/3.3V CR#_E Input. Selected via CR#_E_EN/CR#_F_EN bit located in byte 6 bit 7 and 6. When selected, CR#_E controls SRC6, CR#_F controls SRC8 |
| 44 | SRCT7/ CR#_F | I/O, DIF | True 100 MHz differential serial reference clocks/3.3V CR#_F Input. Selected via CR#_E_EN/CR#_F_EN bit located in byte 6 bit 7 and 6. When selected, CR#_E controls SRC6, CR#_F controls SRC8 |
| 45 | VDD_SRC_IO | PWR | 3.3V-1.25V power supply for outputs. |
| 46 | SRCC8 / CPUC2_ITP | O, DIF | Selectable Complementary differential CPU or SRC clock output. ITP_EN = 0 @ CK_PWRGD assertion = SRC8 ITP_EN = 1 @ CK_PWRGD assertion = CPU2 |
| 47 | SRCC8 / CPUC2_ITP | O, DIF | Selectable True differential CPU or SRC clock output. ITP_EN = 0 @ CK_PWRGD assertion = SRC8 ITP_EN = 1 @ CK_PWRGD assertion = CPU2 |
| 48 | NC | NC | No connect. |
| 49 | VDD_CPU_IO | PWR | 3.3V-1.25V Power supply for outputs. |
| 50 | CPUC1 | O, DIF | Complementary differential CPU clock outputs. Note that CPU1 is the iAMT clock and is on in that mode. |
| 51 | CPUT1 | O, DIF | True differential CPU clock outputs. Note that CPU1 is the iAMT clock and is on in that mode. |
| 52 | VSS_CPU | GND | Ground for outputs. |
| 53 | CPUC0 | O, DIF | Complementary differential CPU clock outputs. |
| 54 | CPUT0 | O, DIF | True differential CPU clock outputs. |
| 55 | VDD_CPU | PWR | 3.3V Power supply for CPU PLL. |
| 56 | CKPWRGD / PWRDWN# | I | 3.3V LVTTTL input. This pin is a level sensitive strobe used to latch the FS_A, FS_B, FS_C, GLCK_SEL and ITP_EN. After CKPWRGD (active HIGH) assertion, this pin becomes a real-time input for asserting power down (active LOW). |

TSSOP Pin Definitions (continued)

| Pin No. | Name | Type | Description |
|---------|-----------------------|-------|--|
| 57 | FSB / TEST_MODE | I | 3.3V-tolerant input for CPU frequency selection / Selects Ref/N or Tri-state when in test mode: 0 = Tri-state, 1 = Ref/N Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications. |
| 58 | VSS_REF | GND | Ground for outputs. |
| 59 | Xout | O, SE | 14.318 MHz Crystal output. |
| 60 | Xin | I | 14.318 MHz Crystal input. |
| 61 | VDD_REF | PWR | 3.3V Power supply for outputs and also maintains SMBUS registers during power down. |
| 62 | REF0 / FSC / TEST_SEL | I/O | Fixed 14.318 clock output / 3.3V-tolerant input for CPU frequency selection / Selects test mode if pulled to VIHFS_C when CK_PWRGD is asserted HIGH. Refer to DC Electrical Specifications table for VILFS_C, VIMFS_C, VIHFS_C specifications. |
| 63 | SDATA | I/O | SMBus-compatible SDATA. |
| 64 | SCLK | I | SMBus-compatible SCLOCK. |

Table 1. Frequency Select Pin (FSA, FSB and FSC)

| FSC | FSB | FSA | CPU | SRC | PCIF/PCI | 27MHz | REF | DOT96 | USB |
|-----|-----|-----|----------|----------|----------|----------|------------|----------|----------|
| 0 | 0 | 0 | 266 MHz | 100 MHz | 33 MHz | 27 MHz | 14.318 MHz | 96 MHz | 48 MHz |
| 0 | 0 | 1 | 133 MHz | 100 MHz | 33 MHz | 27 MHz | 14.318 MHz | 96 MHz | 48 MHz |
| 0 | 1 | 0 | 200 MHz | 100 MHz | 33 MHz | 27 MHz | 14.318 MHz | 96 MHz | 48 MHz |
| 0 | 1 | 1 | 166 MHz | 100 MHz | 33 MHz | 27 MHz | 14.318 MHz | 96 MHz | 48 MHz |
| 1 | 0 | 0 | 333 MHz | 100 MHz | 33 MHz | 27 MHz | 14.318 MHz | 96 MHz | 48 MHz |
| 1 | 0 | 1 | 100 MHz | 100 MHz | 33 MHz | 27 MHz | 14.318 MHz | 96 MHz | 48 MHz |
| 1 | 1 | 0 | 400 MHz | 100 MHz | 33 MHz | 27 MHz | 14.318 MHz | 96 MHz | 48 MHz |
| 1 | 1 | 1 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

Frequency Select Pin (FSA, FSB and FSC)

Apply the appropriate logic levels to FSA, FSB, and FSC inputs before CK-PWRGD assertion to achieve host clock frequency selection. When the clock chip sampled HIGH on CK-PWRGD and indicates that VTT voltage is stable then FSA, FSB, and FSC input values are sampled. This process employs a one-shot functionality and once the CK-PWRGD sampled a valid HIGH, all other FSA, FSB, FSC, and CK-PWRGD transitions are ignored except in test mode

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is

optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, Access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h)

Table 2. Command Code Definition

| Bit | Description |
|-------|--|
| 7 | 0 = Block read or block write operation, 1 = Byte read or byte write operation |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '000000' |

Table 3. Block Read and Block Write Protocol

| Block Write Protocol | | Block Read Protocol | |
|----------------------|--|---------------------|-------------------------------------|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 8:2 | Slave address–7 bits | 8:2 | Slave address–7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code–8 bits | 18:11 | Command Code–8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Byte Count–8 bits (Skip this step if I ² C_EN bit set) | 20 | Repeat start |
| 28 | Acknowledge from slave | 27:21 | Slave address–7 bits |
| 36:29 | Data byte 1–8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 45:38 | Data byte 2–8 bits | 37:30 | Byte Count from slave–8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| | Data Byte /Slave Acknowledges | 46:39 | Data byte 1 from slave–8 bits |
| | Data Byte N–8 bits | 47 | Acknowledge |
| | Acknowledge from slave | 55:48 | Data byte 2 from slave–8 bits |
| | Stop | 56 | Acknowledge |
| | | | Data bytes from slave / Acknowledge |
| | | | Data Byte N from slave–8 bits |
| | | | NOT Acknowledge |
| | | | Stop |

Table 4. Byte Read and Byte Write Protocol

| Byte Write Protocol | | Byte Read Protocol | |
|---------------------|------------------------|--------------------|------------------------|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 8:2 | Slave address–7 bits | 8:2 | Slave address–7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code–8 bits | 18:11 | Command Code–8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Data byte–8 bits | 20 | Repeated start |
| 28 | Acknowledge from slave | 27:21 | Slave address–7 bits |
| 29 | Stop | 28 | Read |
| | | 29 | Acknowledge from slave |
| | | 37:30 | Data from slave–8 bits |
| | | 38 | NOT Acknowledge |
| | | 39 | Stop |

Control Registers

Byte 0: Control Register 0

| Bit | @Pup | Name | Description |
|-----|------|--------------|--|
| 7 | HW | FS_C | CPU Frequency Select Bit, set by HW |
| 6 | HW | FS_B | CPU Frequency Select Bit, set by HW |
| 5 | HW | FS_A | CPU Frequency Select Bit, set by HW |
| 4 | 0 | iAMT_EN | Set via SMBus or by combination of PWRDWN, CPU_STP, and PCI_STP 0 = Legacy Mode, 1 = iAMT Enabled |
| 3 | 0 | Reserved | Reserved |
| 2 | 0 | SRC_Main_SEL | Select source for SRC clock 0 = SRC_MAIN = PLL1, <i>PLL3_CFG Table applies</i> 1 = SRC_MAIN = PLL3, <i>PLL3_CFG Table does not apply</i> |
| 1 | 0 | SATA_SEL | Select source of SATA clock 0 = SATA = SRC_MAIN, 1 = SATA = PLL2 |
| 0 | 1 | PD_Restore | Save Config. In powerdown 0 = Config. Cleared, 1 = Config. Saved |

Byte 1: Control Register 1

| Bit | @Pup | Name | Description |
|-----|------|------------|---|
| 7 | 0 | SRC0_SEL | Select for SRC0 or DOT96 0 = SRC0, 1 = DOT96 When GCLK_SEL=0, this bit is 1. When GCLK_SEL=1, this bit is 0 |
| 6 | 0 | PLL1_SS_DC | Select for down or center SS 0 = Down spread, 1 = Center spread |
| 5 | 0 | PLL3_SS_DC | Select for down or center SS 0 = Down spread, 1 = Center spread |
| 4 | 0 | PLL3_CFB3 | Bit 4:1 only applies when SRC_Main_SEL = 0 See <i>Table 8: PLL3 / SE configuration table</i> |
| 3 | 0 | PLL3_CFB2 | |
| 2 | 0 | PLL3_CFB1 | |
| 1 | 1 | PLL3_CFB0 | |
| 0 | 1 | Reserved | Reserved |

Byte 2: Control Register 2

| Bit | @Pup | Name | Description |
|-----|------|-------|--|
| 7 | 1 | REF | Output enable for REF 0 = Output Disabled, 1 = Output Enabled |
| 6 | 1 | USB | Output enable for USB 0 = Output Disabled, 1 = Output Enabled |
| 5 | 1 | PCIF0 | Output enable for PCIF0 0 = Output Disabled, 1 = Output Enabled |
| 4 | 1 | PCI4 | Output enable for PCI4 0 = Output Disabled, 1 = Output Enabled |
| 3 | 1 | PCI3 | Output enable for PCI3 0 = Output Disabled, 1 = Output Enabled |
| 2 | 1 | PCI2 | Output enable for PCI2 0 = Output Disabled, 1 = Output Enabled |
| 1 | 1 | PCI1 | Output enable for PCI1 0 = Output Disabled, 1 = Output Enabled |
| 0 | 1 | PCI0 | Output enable for PCI0 0 = Output Disabled, 1 = Output Enabled |

Byte 3: Control Register 3

| Bit | @Pup | Name | Description |
|-----|------|--------------------|---|
| 7 | 1 | SRC[T/C]11 | Output enable for SRC11 0 = Output Disabled, 1 = Output Enabled |
| 6 | 1 | SRC[T/C]10 | Output enable for SRC10 0 = Output Disabled, 1 = Output Enabled |
| 5 | 1 | SRC[T/C]9 | Output enable for SRC9 0 = Output Disabled, 1 = Output Enabled |
| 4 | 1 | SRC[T/C]8/CPU2_ITP | Output enable for SRC8 or CPU2_ITP 0 = Output Disabled, 1 = Output Enabled |
| 3 | 1 | SRC[T/C]7 | Output enable for SRC7 0 = Output Disabled, 1 = Output Enabled |
| 2 | 1 | SRC[T/C]6 | Output enable for SRC6 0 = Output Disabled, 1 = Output Enabled |
| 1 | 1 | Reserved | Reserved |
| 0 | 1 | SRC[T/C]4 | Output enable for SRC4 0 = Output Disabled, 1 = Output Enabled |

Byte 4: Control Register 4

| Bit | @Pup | Name | Description |
|-----|------|-------------------------|--|
| 7 | 1 | SRC[T/C]3 | Output enable for SRC3 0 = Output Disabled, 1 = Output Enabled |
| 6 | 1 | SRC[T/C]2/SATA | Output enable for SRC2/SATA 0 = Output Disabled, 1 = Output Enabled |
| 5 | 1 | SRC[T/C]1/LCD_100M[T/C] | Output enable for SRC1/LCD_100M 0 = Output Disabled, 1 = Output Enabled |
| 4 | 1 | SRC[T/C]0/DOT96[T/C] | Output enable for SRC0/DOT96 0 = Output Disabled, 1 = Output Enabled |
| 3 | 1 | CPU[T/C]1 | Output enable for CPU1 0 = Output Disabled, 1 = Output Enabled |
| 2 | 1 | CPU[T/C]0 | Output enable for CPU0 0 = Output Disabled, 1 = Output Enabled |
| 1 | 1 | PLL1_SS_EN | Enable PLL1s spread modulation, 0 = Spread Disabled, 1 = Spread Enabled |
| 0 | 1 | PLL3_SS_EN | Enable PLL3s spread modulation 0 = Spread Disabled, 1 = Spread Enabled |

Byte 5: Control Register 5

| Bit | @Pup | Name | Description |
|-----|------|-----------|--|
| 7 | 0 | CR#_A_EN | Enable CR#_A (clk req) 0 = Disabled, 1 = Enabled, |
| 6 | 0 | CR#_A_SEL | Set CR#_A → SRC0 or SRC2 0 = CR#_A→SRC0, 1 = CR#_A→SRC2 |
| 5 | 0 | CR#_B_EN | Enable CR#_B (clk req) 0 = Disabled, 1 = Enabled, |
| 4 | 0 | CR#_B_SEL | Set CR#_B → SRC1 or SRC4 0 = CR#_B→SRC1, 1 = CR#_B→SRC4 |
| 3 | 0 | CR#_C_EN | Enable CR#_C (clk req) 0 = Disabled, 1 = Enabled |
| 2 | 0 | CR#_C_SEL | Set CR#_C → SRC0 or SRC2 0 = CR#_C→SRC0, 1 = CR#_C→SRC2 |

Byte 5: Control Register 5 (continued)

| Bit | @Pup | Name | Description |
|-----|------|-----------|--|
| 1 | 0 | CR#_D_EN | Enable CR#_D (clk req) 0 = Disabled, 1 = Enabled |
| 0 | 0 | CR#_D_SEL | Set CR#_D → SRC1 or SRC4 0 = CR#_D→SRC1, 1 = CR#_D→SRC4 |

Byte 6: Control Register 6

| Bit | @Pup | Name | Description |
|-----|------|------------------|--|
| 7 | 0 | CR#_E_EN | Enable CR#_E (clk req) → SRC6 0 = Disabled, 1 = Enabled |
| 6 | 0 | CR#_F_EN | Enable CR#_F (clk req) → SRC8 0 = Disabled, 1 = Enabled |
| 5 | 0 | CR#_G_EN | Enable CR#_G (clk req) → SRC9 0 = Disabled, 1 = Enabled |
| 4 | 0 | CR#_H_EN | Enable CR#_H (clk req) → SRC10 0 = Disabled, 1 = Enabled |
| 3 | 0 | Reserved | Reserved |
| 2 | 0 | Reserved | Reserved |
| 1 | 0 | LCD_100_STP_CTRL | If set, LCD_100 stop with PCI_STOP# 0 = Free running, 1 = PCI_STOP# stoppable |
| 0 | 0 | SRC_STP_CTRL | If set, SRCs stop with PCI_STOP# 0 = Free running, 1 = PCI_STOP# stoppable |

Byte 7: Vendor ID

| Bit | @Pup | Name | Description |
|-----|------|-----------------|---------------------|
| 7 | 0 | Rev Code Bit 3 | Revision Code Bit 3 |
| 6 | 1 | Rev Code Bit 2 | Revision Code Bit 2 |
| 5 | 1 | Rev Code Bit 1 | Revision Code Bit 1 |
| 4 | 0 | Rev Code Bit 0 | Revision Code Bit 0 |
| 3 | 1 | Vendor ID bit 3 | Vendor ID Bit 3 |
| 2 | 0 | Vendor ID bit 2 | Vendor ID Bit 2 |
| 1 | 0 | Vendor ID bit 1 | Vendor ID Bit 1 |
| 0 | 0 | Vendor ID bit 0 | Vendor ID Bit 0 |

Byte 8: Control Register 8

| Bit | @Pup | Name | Description |
|-----|------|------------|--|
| 7 | 1 | Device_ID3 | 0000 = CK505 Yellow Cover Device, 56-pin TSSOP |
| 6 | 0 | Device_ID2 | 0001 = CK505 Yellow Cover Device, 64-pin TSSOP 0010 = CK505 Yellow Cover Device, 48-pin QFN (Reserved) |
| 5 | 0 | Device_ID1 | 0011 = CK505 Yellow Cover Device, 56-pin QFN (Reserved) |
| 4 | 1 | Device_ID0 | 0100 = CK505 Yellow Cover Device, 64-pin QFN 0101 = CK505 Yellow Cover Device, 72-pin QFN (Reserved) 0110 = CK505 Yellow Cover Device, 48-pin SSOP (Reserved) 0111 = CK505 Yellow Cover Device, 48-pin SSOP (Reserved) 1000 = Reserved 1001 = CY28548 1010 = Reserved 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved |
| 3 | 0 | Reserved | Reserved |
| 2 | 0 | Reserved | Reserved |
| 1 | 1 | 27M_NSS_OE | Output enable for 27M_NSS 0 = Output Disabled, 1 = Output Enabled |
| 0 | 1 | 27M_SS_OE | Output enable for 27M_SS 0 = Output Disabled, 1 = Output Enabled |

Byte 9: Control Register 9

| Bit | @Pup | Name | Description |
|-----|------|-----------------------|---|
| 7 | 0 | PCIF_0_with PCI_STOP# | Allows control of PCIF_0 with assertion of PCI_STOP# 0 = Free running PCIF, 1 = Stopped with PCI_STOP# |
| 6 | HW | TME_STRAP | Trusted mode enable strap status 0 = Normal, 1 = No overclocking |
| 5 | 1 | REF drive strength | REF drive strength 0 = Low 1x, 1 = High 2x |
| 4 | 0 | TEST_MODE_SEL | Mode select either REF/N or tri-state 0 = All output tri-state, 1 = All output REF/N |
| 3 | 0 | TEST_MODE_ENTRY | Allow entry into test mode 0 = Normal operation, 1 = Enter test mode |
| 2 | 1 | 12C_VOUT<2> | I2C_VOUT[2,1,0] |
| 1 | 0 | 12C_VOUT<1> | 000 = 0.63V 001 = 0.71V |
| 0 | 1 | 12C_VOUT<0> | 010 = 0.77V 011 = 0.82V 100 = 0.86V 101 = 0.90V (default) 110 = 0.93V 111 = unused |

Byte 10: Control Register 10

| Bit | @Pup | Name | Description |
|-----|------|----------------|--|
| 7 | HW | GCLK_SEL latch | Readback of GCLK_SEL latch 0 = DOT96/LCD_100, 1 = SRC0/27 MHz |
| 6 | 1 | PLL3_EN | PLL3 power down 0 = Power down, 1 = Power up |

Byte 10: Control Register 10 (continued)

| Bit | @Pup | Name | Description |
|-----|------|------------------|--|
| 5 | 1 | PLL2_EN | PLL2 power down 0 = Power down, 1 = Power up |
| 4 | 1 | SRC_DIV_EN | SRC divider disable 0 = Disabled, 1 = Enabled |
| 3 | 1 | PCI_DIV_EN | PCI divider disable 0 = Disabled, 1 = Enabled |
| 2 | 1 | CPU_DIV_EN | CPU divider disable 0 = Disabled, 1 = Enabled |
| 1 | 1 | CPU1 Stop Enable | Enable CPU_STOP# control of CPU1 0 = Free running, 1= Stoppable |
| 0 | 1 | CPU0 Stop Enable | Enable CPU_STOP# control of CPU0 0 = Free running, 1= Stoppable |

Byte 11: Control Register 11

| Bit | @Pup | Name | Description |
|-----|------|----------|-------------|
| 7 | 0 | Reserved | Reserved |
| 6 | 0 | Reserved | Reserved |
| 5 | 0 | Reserved | Reserved |
| 4 | 0 | Reserved | Reserved |
| 3 | 0 | Reserved | Reserved |
| 2 | 0 | Reserved | Reserved |
| 1 | 0 | Reserved | Reserved |
| 0 | 0 | Reserved | Reserved |

Byte 12: Byte Count

| Bit | @Pup | Name | Description |
|-----|------|----------|-------------|
| 7 | 0 | Reserved | Reserved |
| 6 | 0 | Reserved | Reserved |
| 5 | 0 | BC5 | Byte count |
| 4 | 0 | BC4 | Byte count |
| 3 | 1 | BC3 | Byte count |
| 2 | 1 | BC2 | Byte count |
| 1 | 0 | BC1 | Byte count |
| 0 | 1 | BC0 | Byte count |

Byte 13: Control Register 13

| Bit | @Pup | Name | Description |
|-----|------|--------------------------|---|
| 7 | 1 | USB drive strength | USB drive strength 0 = Low, 1= High |
| 6 | 1 | PCI/ PCIF drive strength | PCI drive strength 0 = Low, 1 = High |
| 5 | 0 | PLL1_Spread | Select percentage of spread for PLL1 0 = 0.5%, 1=1% |
| 4 | 1 | SATA_SS_EN | Enable SATA spread modulation, 0 = Spread Disabled, 1 = Spread Enabled |
| 3 | 1 | CPU[T/C]2 | Allow control of CPU2 with assertion of CPU_STOP# 0 = Free running, 1 = Stopped with CPU_STOP# |

Byte 13: Control Register 13 (continued)

| Bit | @Pup | Name | Description |
|-----|------|-------------------------------|--|
| 2 | 1 | SE1/SE2 drive strength 1 of 2 | SE1 and SE2 Drive Strength Setting 1 of 2 (See Byte 0 = Low, 1= High) |
| 1 | 0 | Reserved | Reserved |
| 0 | 1 | SW_PCI | SW PCI_STP# Function 0 = SW PCI_STP assert, 1 = SW PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs are stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs are resumed in a synchronous manner with no short pulses. |

Byte 14: Control Register 14

| Bit | @Pup | Name | Description |
|-----|------|------------|---|
| 7 | 0 | CPU_DAF_N7 | If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] are used to determine the CPU output frequency. |
| 6 | 0 | CPU_DAF_N6 | |
| 5 | 0 | CPU_DAF_N5 | |
| 4 | 0 | CPU_DAF_N4 | |
| 3 | 0 | CPU_DAF_N3 | |
| 2 | 0 | CPU_DAF_N2 | |
| 1 | 0 | CPU_DAF_N1 | |
| 0 | 0 | CPU_DAF_N0 | |

Byte 15: Control Register 15

| Bit | @Pup | Name | Description |
|-----|------|------------|---|
| 7 | 0 | CPU_DAF_N8 | See Byte 14 for description |
| 6 | 0 | CPU_DAF_M6 | If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] are used to determine the CPU output frequency. |
| 5 | 0 | CPU_DAF_M5 | |
| 4 | 0 | CPU_DAF_M4 | |
| 3 | 0 | CPU_DAF_M3 | |
| 2 | 0 | CPU_DAF_M2 | |
| 1 | 0 | CPU_DAF_M1 | |
| 0 | 0 | CPU_DAF_M0 | |

Byte 16: Control Register 16

| Bit | @Pup | Name | Description |
|-----|------|----------|--|
| 7 | 0 | PCI-E_N7 | PCI-E Dial-A-Frequency [®] Bit N7 |
| 6 | 0 | PCI-E_N6 | PCI-E Dial-A-Frequency Bit N6 |
| 5 | 0 | PCI-E_N5 | PCI-E Dial-A-Frequency Bit N5 |
| 4 | 0 | PCI-E_N4 | PCI-E Dial-A-Frequency Bit N4 |
| 3 | 0 | PCI-E_N3 | PCI-E Dial-A-Frequency Bit N3 |
| 2 | 0 | PCI-E_N2 | PCI-E Dial-A-Frequency Bit N2 |
| 1 | 0 | PCI-E_N1 | PCI-E Dial-A-Frequency Bit N1 |
| 0 | 0 | PCI-E_N0 | PCI-E Dial-A-Frequency Bit N0 |

Byte 17: Control Register 17

| Bit | @Pup | Name | Description |
|-----|------|------|-------------|
|-----|------|------|-------------|

Byte 17: Control Register 17 (continued)

| | | | |
|---|---|-----------------------------------|---|
| 7 | 0 | SMSW_EN | Enable Smooth Switching 0 = Disabled, 1= Enabled |
| 6 | 0 | SMSW_SEL | Smooth switch select 0 = CPU_PLL, 1 = SRC_PLL |
| 5 | 0 | SE1/SE2 drive strength 2 of 2 | SE1 and SE2 drive strength Setting 2 of 2 |
| 4 | 0 | Prog_PCI-E_EN | Programmable PCI-E frequency enable 0 = Disabled, 1= Enabled |
| 3 | 0 | Prog_CPU_EN | Programmable CPU frequency enable 0 = Disabled, 1= Enabled |
| 2 | 0 | REF drive strength 2 of 2 | REFdrive strength strength Setting 2 of 2 |
| 1 | 0 | USB drive strength 2 of 2 | USB drive strength strength Setting 2 of 2 |
| 0 | 0 | PCI/ PCIF drive strength 2of 2 | PCI drive strength strength Setting 2 of 2 |

Table 5. Crystal Recommendations

| Frequency (Fund) | Cut | Loading | Load Cap | Drive (max.) | Shunt Cap (max.) | Motional (max.) | Tolerance (max.) | Stability (max.) | Aging (max.) |
|------------------|-----|----------|----------|--------------|------------------|-----------------|------------------|------------------|--------------|
| 14.31818 MHz | AT | Parallel | 20 pF | 0.1 mW | 5 pF | 0.016 pF | 35 ppm | 30 ppm | 5 ppm |

The CY28548 requires a Parallel Resonance Crystal. Substituting a series resonance crystal causes the CY28548 to operate at the wrong frequency and violates the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading

crystal loading correctly. Again, the capacitance on each side is in series with the crystal. The total capacitance on both side is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. It is important that the trim capacitors are in series with the crystal. It is not true that load capacitors are in parallel with the crystal and are approximately equal to the load capacitance of the crystal.

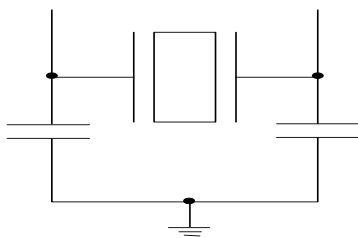


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the

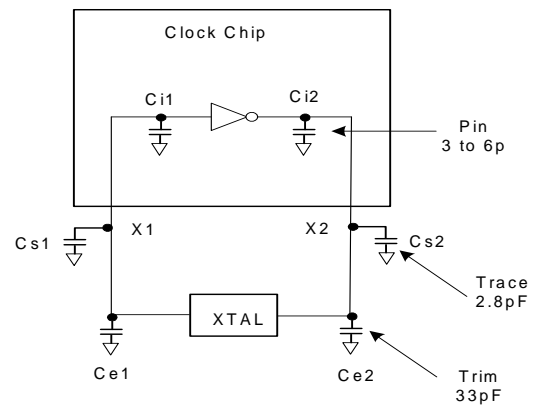


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$C_e = 2 * CL - (C_s + C_i)$$

Total Capacitance (as seen by the crystal)

$$CL_e = \frac{1}{\left(\frac{1}{C_{e1} + C_{s1} + C_{i1}} + \frac{1}{C_{e2} + C_{s2} + C_{i2}} \right)}$$

| | |
|-----------|--|
| CL | Crystal load capacitance |
| CLe | Actual loading seen by crystal using standard value trim capacitors |
| Ce | External trim capacitors |
| Cs | Stray capacitance (terraced) |
| Ci | Internal capacitance (lead frame, bond wires, etc.) |

Dial-A-Frequency® (CPU and PCIEX)

This feature allows the user to over-clock their system by slowly stepping up the CPU or SRC frequency. When the programmable output frequency feature is enabled, the CPU and SRC frequencies are determined by the following equation:

$$F_{cpu} = G * N/M \text{ or } F_{cpu} = G2 * N, \text{ where } G2 = G / M.$$

- “N” and “M” are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively.
- “G” stands for the PLL Gear Constant, which is determined by the programmed value of FS[E:A]. See *Table 1, Frequency Select Table* for the Gear Constant for each Frequency selection. The PCI Express only allows user control of the N register, the M value is fixed and documented in *Table 1, Frequency Select Table*.

In this mode, the user writes the desired N and M values into the DAF I2C registers. The user cannot change only the M value and must change both the M and the N values at the same time, if they require a change to the M value. The user may change only the N value.

Associated Register Bits

- *CPU_DAF Enable* – This bit enables CPU DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the CPU_DAF_N register. Note that the CPU_DAF_N and M register must contain valid values before CPU_DAF is set. Default = 0, (No DAF).
- *CPU_DAF_N* – There are nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in *Table 1, Frequency Select Table*.
- *CPU DAF M* – There are 7 bits (for 128 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, the allowable values for M are detailed in *Table 1, Frequency Select Table*.
- *SRC_DAF Enable* – This bit enables SRC DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the SRC_DAF_N register. Note that the SRC_DAF_N register must contain valid values before SRC_DAF is set. Default = 0, (No DAF).
- *SRC_DAF_N* – There are nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in *Table 1, Frequency Select Table*.

Smooth Switching

The device contains one smooth switch circuit that is shared by the CPU PLL and SRC PLL. The smooth switch circuit ensures that when the output frequency changes by overclocking, the transition from the old frequency to the new frequency is a slow, smooth transition containing no glitches. The rate of change of output frequency when using the smooth switch circuit is less than 1 MHz/0.667 μs. The frequency overshoot and undershoot is less than 2%.

The Smooth Switch circuit assigns auto or manual. In Auto mode, clock generator assigns smooth switch automatically when the PLL does overclocking. For manual mode, assign the smooth switch circuit to PLL via Smbus. By default the smooth switch circuit is set to auto mode. PLL can be over-clocked when it does not have control of the smooth switch circuit but it is not guaranteed to transition to the new frequency without large frequency glitches.

Do not enable over-clocking and change the N values of both PLLs in the same SMBUS block write and use smooth switch mechanism on spread spectrum on/off.

PD_RESTORE

If a '0' is set for Byte 0 bit 0 then, upon assertion of PWRDWN# LOW, the CY28548 initiates a full reset. The result of this is that the clock chip emulates a cold power on start and goes to the “Latches Open” state. If the PD_RESTORE bit is set to a '1' then the configuration is stored upon PWRDWN# asserted LOW. Note that if the iAMT bit, Byte 0 bit 3, is set to a '1' then the PD_RESTORE bit must be ignored. In other words, in Intel iAMT mode, PWRDWN# reset is not allowed.

PWRDWN# (Power down) Clarification

The CKPWRGD/PWRDWN# pin is a dual-function pin. During initial power up, the pin functions as CKPWRGD. Once CKPWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, clocks are driven to a LOW value and held before turning off the VCOs and the crystal oscillator.

PWRDWN# (Power down) Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must held LOW. When PD mode is desired as the initial power on state, PD must be asserted HIGH in less than 10 μs after asserting CKPWRGD.

PWRDWN# Deassertion

The power up latency is less than 1.8 ms. This is the time from the deassertion of the PD# pin or the ramping of the power supply until the time that stable clocks are generated from the clock chip. All differential outputs stopped in a three-state condition, resulting from power down are driven high in less than 300 μs of PD# deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are enabled within a few clock cycles of

each clock. *Figure 4* is an example showing the relationship of clocks coming up.

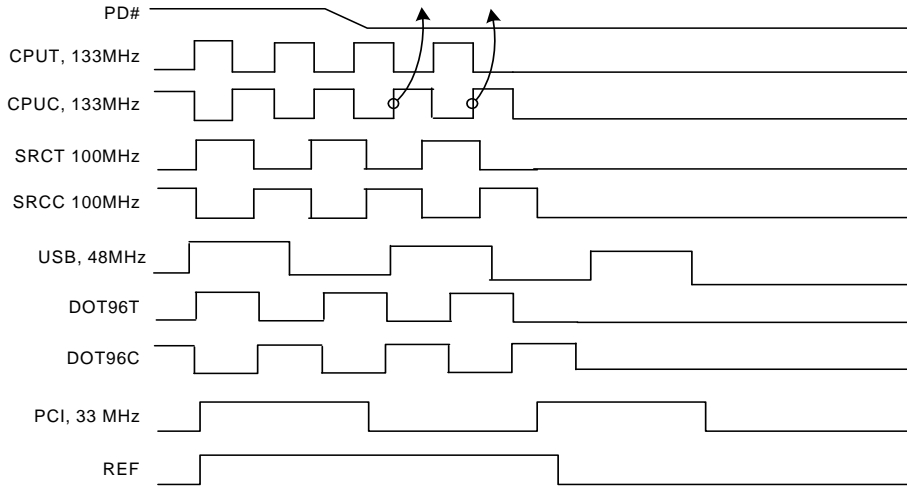


Figure 3. Power down Assertion Timing Waveform

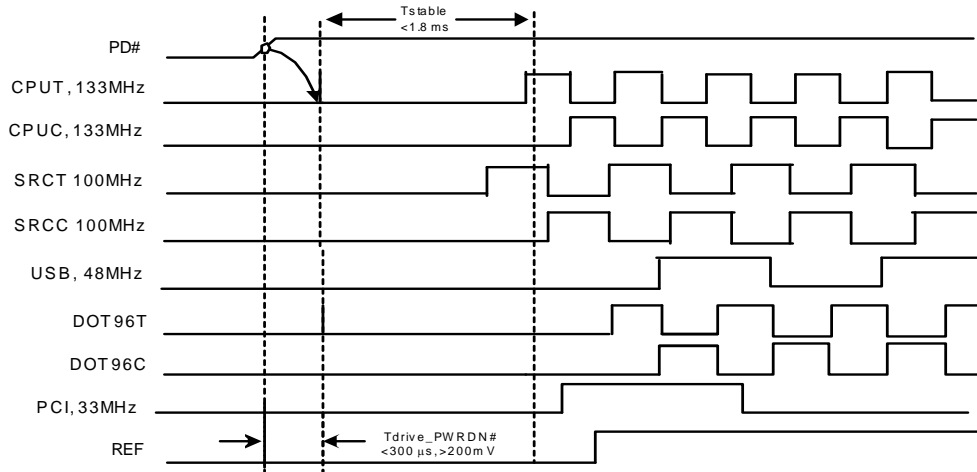


Figure 4. Power down Deassertion Timing Waveform

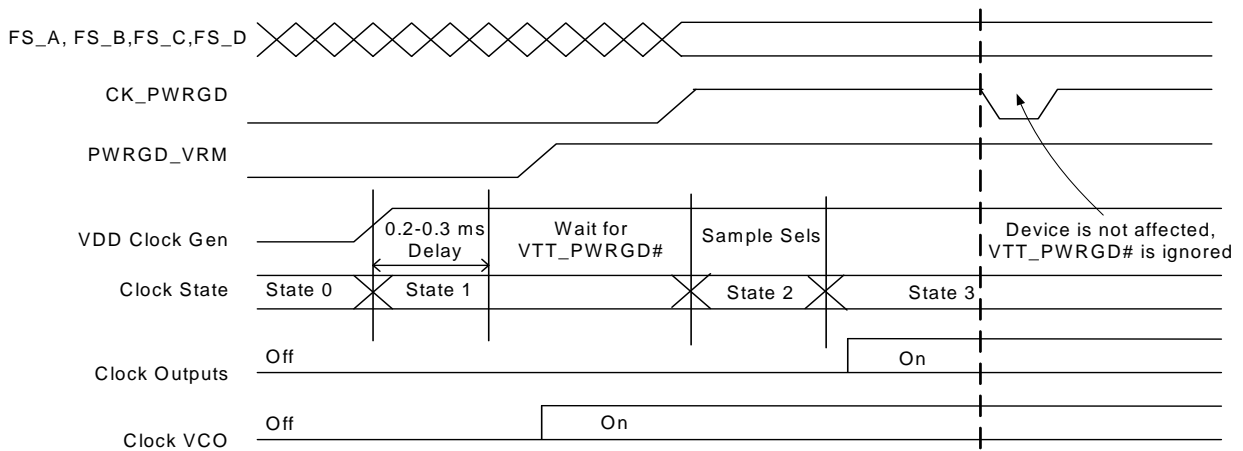


Figure 5. CK_PWRGD Timing Diagram

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable are stopped within two to six CPU clock periods after sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW.

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal causes all stopped CPU outputs to resume normal operation in a synchronous manner. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

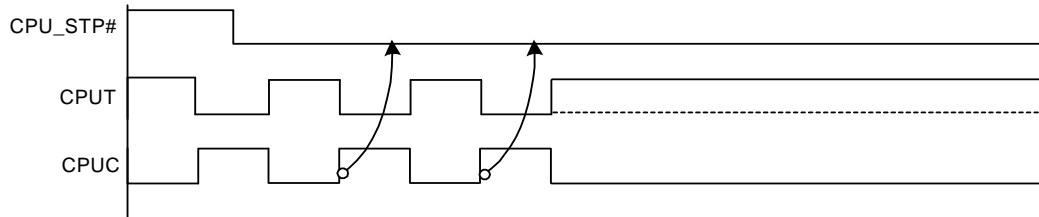


Figure 6. CPU_STP# Assertion Waveform

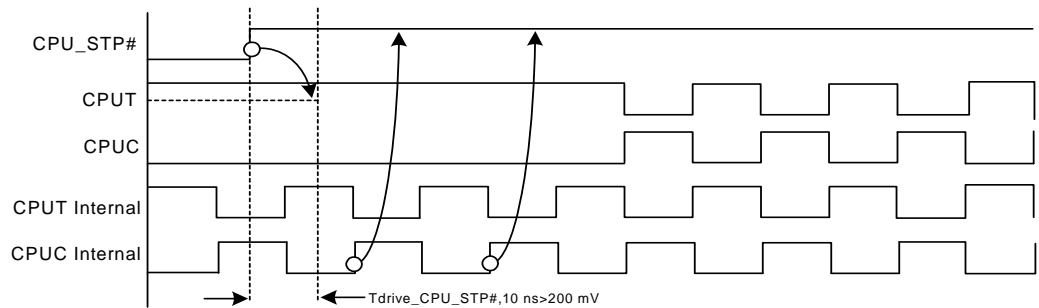


Figure 7. CPU_STP# Deassertion Waveform

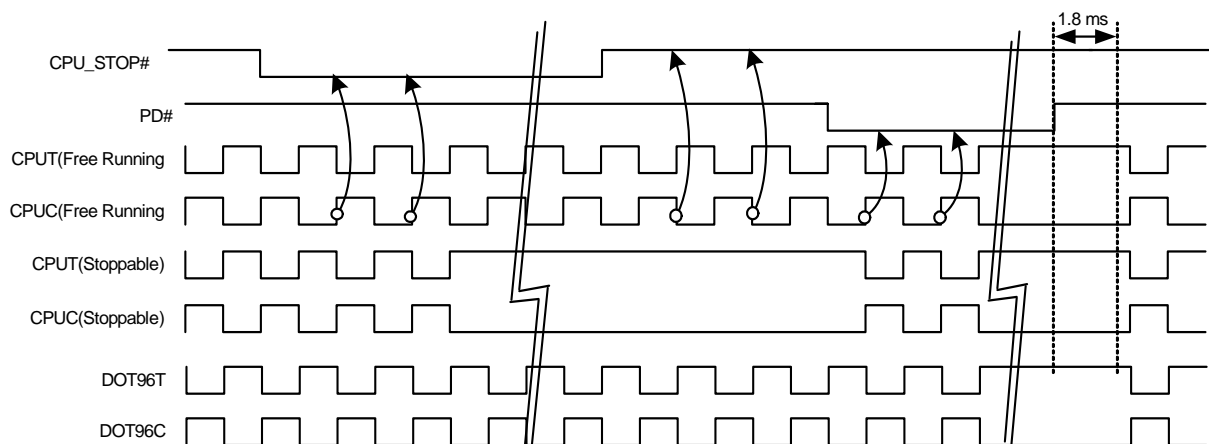


Figure 8. CPU_STP# = Driven, CPU_PD = Driven, DOT_PD = Driven

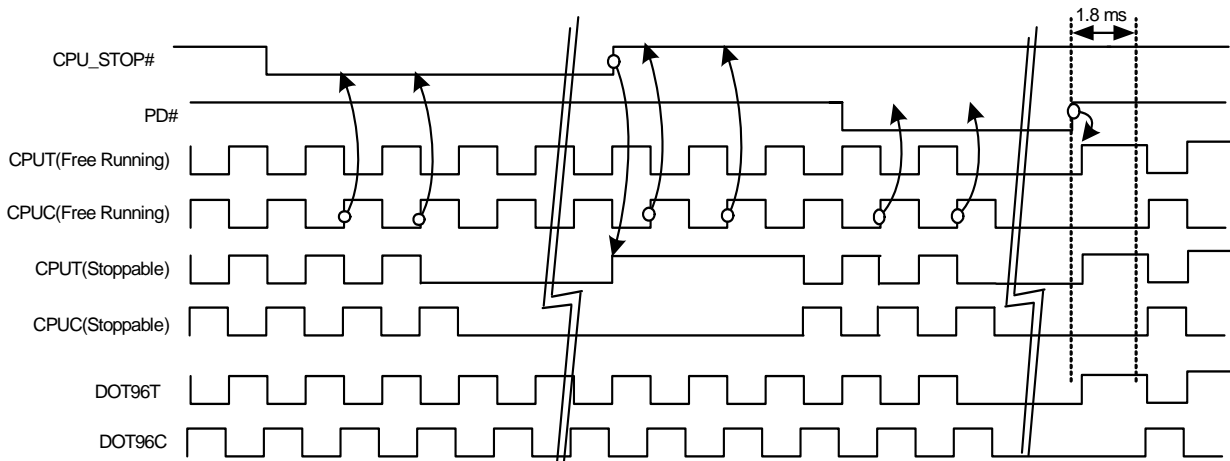


Figure 9. CPU_STP# = Tri-state, CPU_PD = Tri-state, DOT_PD = Tri-state

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronously stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{SU}). (See Figure 10.) The PCIF clocks are affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free running.

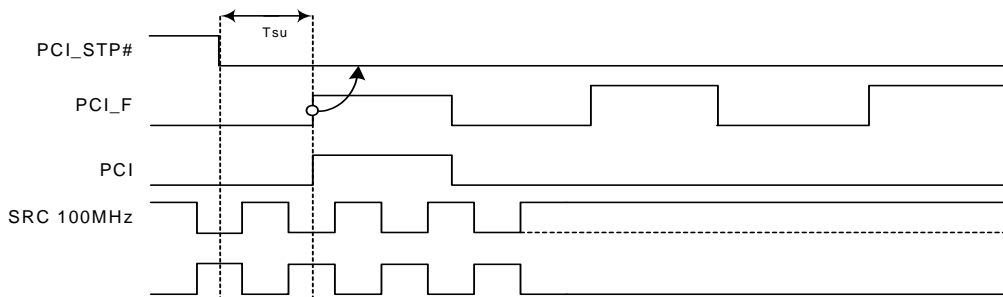


Figure 10. PCI_STP# Assertion Waveform

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal causes all PCI and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods, after PCI_STP# transitions to a HIGH level.

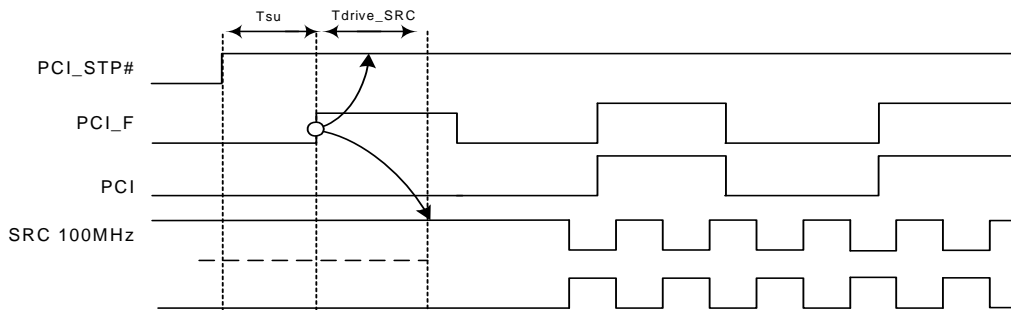


Figure 11. PCI_STP# Deassertion Waveform

Table 6. Output Driver Status during PCI-STOP# and CPU-STOP#

| | | PCI_STOP# Asserted | CPU_STOP# Asserted | SMBus OE Disabled |
|---------------------|---------------|--------------------|--------------------|----------------------------------|
| Single-ended Clocks | Stoppable | Driven low | Running | Driven low |
| | Non stoppable | Running | Running | |
| Differential Clocks | Stoppable | Clock driven high | Clock driven high | Clock driven Low or 20K pulldown |
| | | Clock# driven low | Clock# driven low | |
| | Non stoppable | Running | Running | |

Table 7. Output Driver Status

| | All Single-ended Clocks | | All Differential Clocks except CPU1 | | CPU1 | |
|--------------------|-------------------------|----------|-------------------------------------|--------|---------------------|---------|
| | w/o Strap | w/ Strap | Clock | Clock# | Clock | Clock# |
| Latches Open State | Low | Hi-z | Low or 20K pulldown | Low | Low or 20K pulldown | Low |
| Powerdown | Low | Hi-z | Low or 20K pulldown | Low | Low or 20K pulldown | Low |
| M1 | Low | Hi-z | Low or 20K pulldown | Low | Running | Running |

Table 8. PLL3/SE Configuration Table

| GCLK_SEL | B1b4 | B1b3 | B1b2 | B1b1 | Pin 27 (17) MHz | Pin 25 (18) MHz | Spread (%) | Comment |
|----------|------|------|------|------|-----------------|-----------------|------------|--------------------|
| 0 | 0 | 0 | 0 | 0 | PLL3 Disabled | | | |
| 0 | 0 | 0 | 0 | 1 | 100 | 100 | 0.5 | SRC1 from SRC_Main |
| 0 | 0 | 0 | 1 | 0 | 100 | 100 | 0.5 | LCD_100 from PLL3 |
| 0 | 0 | 0 | 1 | 1 | 100 | 100 | 1 | LCD_100 from PLL3 |
| 0 | 0 | 1 | 0 | 0 | 100 | 100 | 1.5 | LCD_100 from PLL3 |
| 0 | 0 | 1 | 0 | 1 | 100 | 100 | 2 | LCD_100 from PLL3 |
| 0 | 0 | 1 | 1 | 0 | N/A | N/A | N/A | N/A |
| 0 | 0 | 1 | 1 | 1 | N/A | N/A | N/A | N/A |
| 0 | 1 | 0 | 0 | 0 | N/A | N/A | N/A | N/A |
| 0 | 1 | 0 | 0 | 1 | N/A | N/A | N/A | N/A |
| 0 | 1 | 0 | 1 | 0 | N/A | N/A | N/A | N/A |
| 0 | 1 | 0 | 1 | 1 | N/A | N/A | N/A | N/A |
| 0 | 1 | 1 | 0 | 0 | N/A | N/A | none | N/A |
| 0 | 1 | 1 | 0 | 1 | N/A | N/A | N/A | N/A |
| 0 | 1 | 1 | 1 | 0 | N/A | N/A | N/A | N/A |
| 0 | 1 | 1 | 1 | 1 | N/A | N/A | N/A | N/A |
| 1 | 0 | 0 | 0 | 0 | N/A | N/A | N/A | |
| 1 | 0 | 0 | 0 | 1 | 27M_NSS | 27M_NSS | 0.5 | 27M_NSS from PLL3 |
| 1 | 0 | 0 | 1 | 0 | 27M_NSS | 27M_NSS | 0.5 | 27M_NSS from PLL3 |
| 1 | 0 | 0 | 1 | 1 | 27M_NSS | 27M_NSS | 1 | 27M_NSS from PLL3 |
| 1 | 0 | 1 | 0 | 0 | 27M_NSS | 27M_NSS | 1.5 | 27M_NSS from PLL3 |
| 1 | 0 | 1 | 0 | 1 | 27M_NSS | 27M_NSS | 2 | 27M_NSS from PLL3 |
| 1 | 0 | 1 | 1 | 0 | N/A | N/A | N/A | |
| 1 | 0 | 1 | 1 | 1 | N/A | N/A | N/A | |
| 1 | 1 | 0 | 0 | 0 | N/A | N/A | N/A | |
| 1 | 1 | 0 | 0 | 1 | N/A | N/A | N/A | |
| 1 | 1 | 0 | 1 | 0 | N/A | N/A | N/A | |
| 1 | 1 | 0 | 1 | 1 | N/A | N/A | N/A | |
| 1 | 1 | 1 | 0 | 0 | N/A | N/A | N/A | |

Table 8. PLL3/SE Configuration Table (continued)

| GCLK_SEL | B1b4 | B1b3 | B1b2 | B1b1 | Pin 27 (17) MHz | Pin 25 (18) MHz | Spread (%) | Comment |
|----------|------|------|------|------|-----------------|-----------------|------------|---------|
| 1 | 1 | 1 | 0 | 1 | N/A | N/A | N/A | |

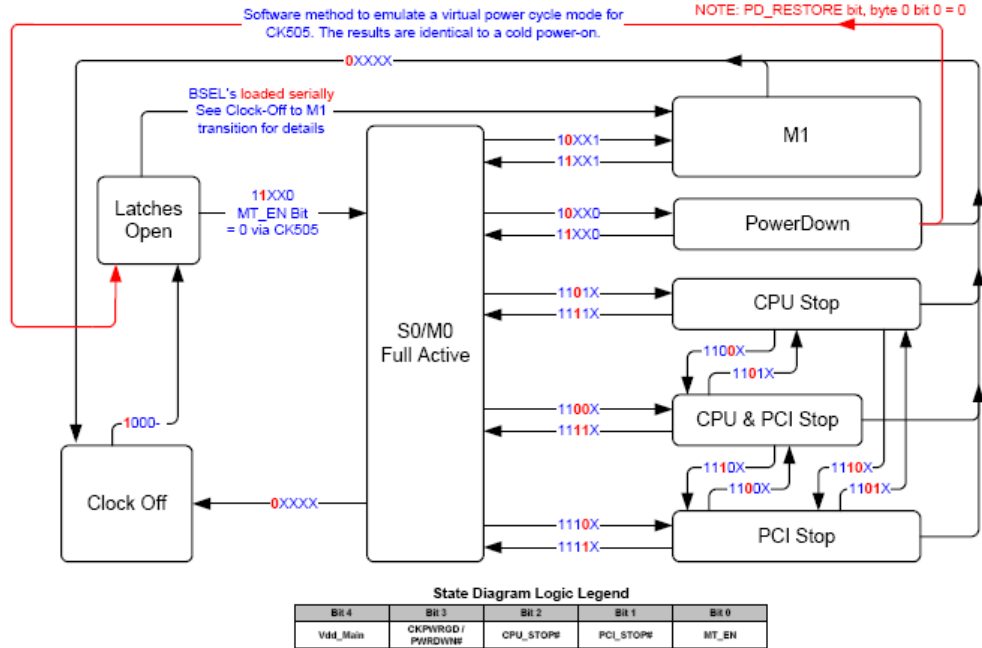


Figure 12. Clock Generator Power up/Run State Diagram

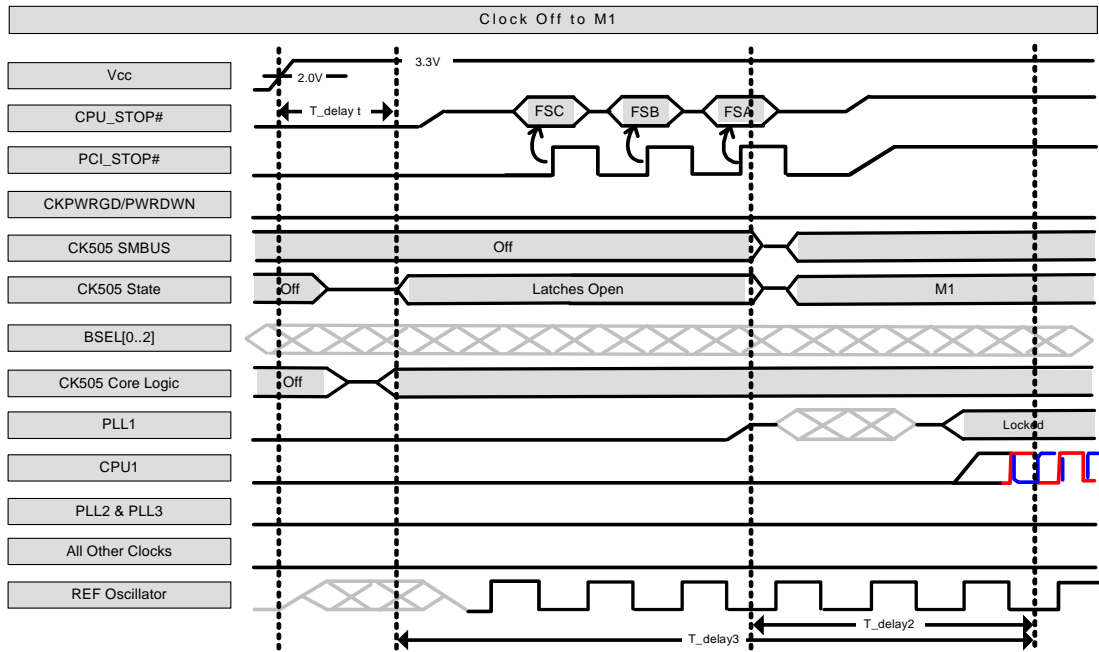


Figure 13. BSEL Serial Latching

Absolute Maximum Conditions

| Parameter | Description | Condition | Min. | Max. | Unit |
|--------------------|-----------------------------------|-----------------------------|------|------|-----------------|
| V _{DD} | Core Supply Voltage | | – | 4.6 | V |
| V _{DD_A} | Analog Supply Voltage | | – | 4.6 | V |
| V _{DD_IO} | IO Supply Voltage | | | 1.5 | V |
| V _{IN} | Input Voltage | Relative to V _{SS} | –0.5 | 4.6 | V _{DC} |
| T _S | Temperature, Storage | Non-functional | –65 | 150 | °C |
| T _A | Temperature, Operating Ambient | Functional | 0 | 85 | °C |
| T _J | Temperature, Junction | Functional | – | 150 | °C |
| ∅ _{JC} | Dissipation, Junction to Case | Mil-STD-883E Method 1012.1 | – | 20 | °C/W |
| ∅ _{JA} | Dissipation, Junction to Ambient | JEDEC (JESD 51) | – | 60 | °C/W |
| ESD _{HBM} | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | – | V |
| UL-94 | Flammability Rating | At 1/8 in. | V–0 | | |
| MSL | Moisture Sensitivity Level | | 1 | | |

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|----------------------------|--------------------------------|--|-----------------------|-----------------------|------|
| V _{DD core} | 3.3V Operating Voltage | 3.3 ± 5% | 3.135 | 3.465 | V |
| V _{IH} | 3.3V Input High Voltage (SE) | | 2.0 | V _{DD} + 0.3 | V |
| V _{IL} | 3.3V Input Low Voltage (SE) | | V _{SS} – 0.3 | 0.8 | V |
| V _{IHI2C} | Input High Voltage | SDATA, SCLK | 2.2 | – | V |
| V _{ILI2C} | Input Low Voltage | SDATA, SCLK | – | 1.0 | V |
| V _{IH_FS} | FS_[A,B] Input High Voltage | | 0.7 | 1.5 | V |
| V _{IL_FS} | FS_[A,B] Input Low Voltage | | V _{SS} – 0.3 | 0.35 | V |
| V _{IHFS_C_TEST} | FS_C Input High Voltage | | 2 | V _{DD} + 0.3 | V |
| V _{IMFS_C_NORMAL} | FS_C Input Middle Voltage | | 0.7 | 1.5 | V |
| V _{ILFS_C_NORMAL} | FS_C Input Low Voltage | | V _{SS} – 0.3 | 0.35 | V |
| I _{IH} | Input High Leakage Current | Except internal pull-down resistors, 0 < V _{IN} < V _{DD} | – | 5 | μA |
| I _{IL} | Input Low Leakage Current | Except internal pull-up resistors, 0 < V _{IN} < V _{DD} | –5 | – | μA |
| V _{OH} | 3.3V Output High Voltage (SE) | I _{OH} = –1 mA | 2.4 | – | V |
| V _{OL} | 3.3V Output Low Voltage (SE) | I _{OL} = 1 mA | – | 0.4 | V |
| V _{DD IO} | Low Voltage IO Supply Voltage | | 0.72 | 0.88 | |
| V _{OH} | 3.3V Input High Voltage (DIFF) | | 0.70 | 0.90 | V |
| V _{OL} | 3.3V Input Low Voltage (DIFF) | | | 0.40 | V |
| I _{OZ} | High-impedance Output Current | | –10 | 10 | μA |
| C _{IN} | Input Pin Capacitance | | 1.5 | 5 | pF |
| C _{OUT} | Output Pin Capacitance | | | 6 | pF |
| L _{IN} | Pin Inductance | | – | 7 | nH |
| V _{XIH} | Xin High Voltage | | 0.7V _{DD} | V _{DD} | V |
| V _{XIL} | Xin Low Voltage | | 0 | 0.3V _{DD} | V |
| I _{DD3.3V} | Dynamic Supply Current | | – | 250 | mA |

AC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|--------------------------------|--|---|----------|----------|------|
| Crystal | | | | | |
| T _{DC} | XIN Duty Cycle | The device operates reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification | 47.5 | 52.5 | % |
| T _{PERIOD} | XIN Period | When XIN is driven from an external clock source | 69.841 | 71.0 | ns |
| T _R /T _F | XIN Rise and Fall Times | Measured between 0.3V _{DD} and 0.7V _{DD} | – | 10.0 | ns |
| T _{CCJ} | XIN Cycle to Cycle Jitter | As an average over 1-μs duration | – | 500 | ps |
| L _{ACC} | Long-term Accuracy | | – | 300 | ppm |
| CPU at 0.7V | | | | | |
| T _{DC} | CPUT and CPUC Duty Cycle | Measured at 0V differential at 0.1s | 45 | 55 | % |
| T _{PERIOD} | 100 MHz CPUT and CPUC Period | Measured at 0V differential at 0.1s | 9.99900 | 10.0100 | ns |
| T _{PERIOD} | 133 MHz CPUT and CPUC Period | Measured at 0V differential at 0.1s | 7.49925 | 7.50075 | ns |
| T _{PERIOD} | 166 MHz CPUT and CPUC Period | Measured at 0V differential at 0.1s | 5.99940 | 6.00060 | ns |
| T _{PERIOD} | 200 MHz CPUT and CPUC Period | Measured at 0V differential at 0.1s | 4.99950 | 5.00050 | ns |
| T _{PERIOD} | 266 MHz CPUT and CPUC Period | Measured at 0V differential at 0.1s | 3.74963 | 3.75038 | ns |
| T _{PERIOD} | 333 MHz CPUT and CPUC Period | Measured at 0V differential at 0.1s | 2.99970 | 3.00030 | ns |
| T _{PERIOD} | 400 MHz CPUT and CPUC Period | Measured at 0V differential at 0.1s | 2.49975 | 2.50025 | ns |
| T _{PERIODSS} | 100 MHz CPUT and CPUC Period, SSC | Measured at 0V differential at 0.1s | 10.02406 | 10.02607 | ns |
| T _{PERIODSS} | 133 MHz CPUT and CPUC Period, SSC | Measured at 0V differential at 0.1s | 7.51804 | 7.51955 | ns |
| T _{PERIODSS} | 166 MHz CPUT and CPUC Period, SSC | Measured at 0V differential at 0.1s | 6.01444 | 6.01564 | ns |
| T _{PERIODSS} | 200 MHz CPUT and CPUC Period, SSC | Measured at 0V differential at 0.1s | 5.01203 | 5.01303 | ns |
| T _{PERIODSS} | 266 MHz CPUT and CPUC Period, SSC | Measured at 0V differential at 0.1s | 3.75902 | 3.75978 | ns |
| T _{PERIODSS} | 333 MHz CPUT and CPUC Period, SSC | Measured at 0V differential at 0.1s | 3.00722 | 3.00782 | ns |
| T _{PERIODSS} | 400 MHz CPUT and CPUC Period, SSC | Measured at 0V differential at 0.1s | 2.50601 | 2.50652 | ns |
| T _{PERIODAbs} | 100 MHz CPUT and CPUC Absolute period | Measured at 0V differential at 1 clock | 9.91400 | 10.0860 | ns |
| T _{PERIODAbs} | 133 MHz CPUT and CPUC Absolute period | Measured at 0V differential at 1 clock | 7.41425 | 7.58575 | ns |
| T _{PERIODAbs} | 166 MHz CPUT and CPUC Absolute period | Measured at 0V differential @ 1 clock | 5.91440 | 6.08560 | ns |
| T _{PERIODAbs} | 200 MHz CPUT and CPUC Absolute period | Measured at 0V differential @ 1 clock | 4.91450 | 5.08550 | ns |
| T _{PERIODAbs} | 266 MHz CPUT and CPUC Absolute period | Measured at 0V differential @ 1 clock | 3.66463 | 3.83538 | ns |
| T _{PERIODAbs} | 333 MHz CPUT and CPUC Absolute period | Measured at 0V differential @ 1 clock | 2.91470 | 3.08530 | ns |
| T _{PERIODAbs} | 400 MHz CPUT and CPUC Absolute period | Measured at 0V differential @ 1 clock | 2.41475 | 2.58525 | ns |
| T _{PERIODSSAbs} | 100 MHz CPUT and CPUC Absolute period, SSC | Measured at 0V differential @ 1 clock | 9.91406 | 10.1362 | ns |
| T _{PERIODSSAbs} | 133 MHz CPUT and CPUC Absolute period, SSC | Measured at 0V differential @ 1 clock | 7.41430 | 7.62340 | ns |
| T _{PERIODSSAbs} | 166 MHz CPUT and CPUC Absolute period, SSC | Measured at 0V differential @ 1 clock | 5.91444 | 6.11572 | ns |
| T _{PERIODSSAbs} | 200 MHz CPUT and CPUC Absolute period, SSC | Measured at 0V differential @ 1 clock | 4.91453 | 5.11060 | ns |

AC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|---------------------------------|--|--|----------|----------|------|
| T _{PERIODSSAbs} | 266 MHz CPUT and CPUC Absolute period, SSC | Measured at 0V differential @ 1 clock | 3.66465 | 3.85420 | ns |
| T _{PERIODSSAbs} | 333 MHz CPUT and CPUC Absolute period, SSC | Measured at 0V differential @ 1 clock | 2.91472 | 3.10036 | ns |
| T _{PERIODSSAbs} | 400 MHz CPUT and CPUC Absolute period, SSC | Measured at 0V differential @ 1 clock | 2.41477 | 2.59780 | ns |
| T _{CCJ} | CPU Cycle to Cycle Jitter | Measured at 0V differential | – | 85 | ps |
| T _{CCJ2} | CPU2_ITP Cycle to Cycle Jitter | Measured at 0V differential | – | 125 | ps |
| L _{ACC} | Long-term Accuracy | Measured at 0V differential | – | 100 | ppm |
| T _{SKEW} | CPU0 to CPU1 Clock Skew | Measured at 0V differential | – | 100 | ps |
| T _{SKEW2} | CPU2_ITP to CPU0 Clock Skew | Measured at 0V differential | – | 150 | ps |
| T _R / T _F | CPU Rising/Falling Slew rate | Measured differentially from ±150 mV | 2.5 | 8 | V/ns |
| T _{RFM} | Rise/Fall Matching | Measured single-endedly from ±75 mV | – | 20 | % |
| V _{HIGH} | Voltage High | | | 1.15 | V |
| V _{LOW} | Voltage Low | | –0.3 | – | V |
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 300 | 550 | mV |
| SRC at 0.7V | | | | | |
| T _{DC} | SRC Duty Cycle | Measured at 0V differential | 45 | 55 | % |
| T _{PERIOD} | 100 MHz SRC Period | Measured at 0V differential @ 0.1s | 9.99900 | 10.0010 | ns |
| T _{PERIODSS} | 100 MHz SRC Period, SSC | Measured at 0V differential @ 0.1s | 10.02406 | 10.02607 | ns |
| T _{PERIODAbs} | 100 MHz SRC Absolute Period | Measured at 0V differential @ 1 clock | 9.87400 | 10.1260 | ns |
| T _{PERIODSSAbs} | 100 MHz SRC Absolute Period, SSC | Measured at 0V differential @ 1 clock | 9.87406 | 10.1762 | ns |
| T _{SKEW(window)} | Any SRC Clock Skew from the earliest bank to the latest bank | Measured at 0V differential | – | 3.0 | ns |
| T _{CCJ} | SRC Cycle to Cycle Jitter | Measured at 0V differential | – | 125 | ps |
| L _{ACC} | SRC Long Term Accuracy | Measured at 0V differential | – | 100 | ppm |
| T _R / T _F | SRC Rising/Falling Slew Rate | Measured differentially from ±150 mV | 2.5 | 8 | V/ns |
| T _{RFM} | Rise/Fall Matching | Measured single-endedly from ±75 mV | – | 20 | % |
| V _{HIGH} | Voltage High | | | 1.15 | V |
| V _{LOW} | Voltage Low | | –0.3 | – | V |
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 300 | 550 | mV |
| DOT96 at 0.7V | | | | | |
| T _{DC} | DOT96 Duty Cycle | Measured at 0V differential | 45 | 55 | % |
| T _{PERIOD} | DOT96 Period | Measured at 0V differential at 0.1s | 10.4156 | 10.4177 | ns |
| T _{PERIODAbs} | DOT96 Absolute Period | Measured at 0V differential at 0.1s | 10.1656 | 10.6677 | ns |
| T _{CCJ} | DOT96 Cycle to Cycle Jitter | Measured at 0V differential at 1 clock | – | 250 | ps |
| L _{ACC} | DOT96 Long Term Accuracy | Measured at 0V differential at 1 clock | – | 100 | ppm |
| T _R / T _F | DOT96 Rising/Falling Slew Rate | Measured differentially from ±150 mV | 2.5 | 8 | V/ns |
| T _{RFM} | Rise/Fall Matching | Measured single-endedly from ±75 mV | – | 20 | % |
| V _{HIGH} | Voltage High | | | 1.15 | V |
| V _{LOW} | Voltage Low | | –0.3 | – | V |
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 300 | 550 | mV |
| LCD_100_SSC at 0.7V | | | | | |
| T _{DC} | LCD_100 Duty Cycle | Measured at 0V differential | 45 | 55 | % |
| T _{PERIOD} | 100 MHz LCD_100 Period | Measured at 0V differential at 0.1s | 9.99900 | 10.0010 | ns |

AC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|---------------------------------|--|--|----------|----------|------|
| T _{PERIODSS} | 100 MHz LCD_100 Period, SSC -0.5% | Measured at 0V differential at 0.1s | 10.02406 | 10.02607 | ns |
| T _{PERIODAbs} | 100 MHz LCD_100 Absolute Period | Measured at 0V differential at 1 clock | 9.74900 | 10.25100 | ns |
| T _{PERIODSSAbs} | 100 MHz LCD_100 Absolute Period, SSC | Measured at 0V differential @ 1 clock | 9.74906 | 10.3012 | ns |
| T _{CCJ} | LCD_100 Cycle to Cycle Jitter | Measured at 0V differential | – | 250 | ps |
| L _{ACC} | LCD_100 Long Term Accuracy | Measured at 0V differential | – | 100 | ppm |
| T _R / T _F | LCD_100 Rising/Falling Slew Rate | Measured differentially from ±150 mV | 2.5 | 8 | V/ns |
| T _{RFM} | Rise/Fall Matching | Measured single-endedly from ±75 mV | – | 20 | % |
| V _{HIGH} | Voltage High | | | 1.15 | V |
| V _{LOW} | Voltage Low | | –0.3 | – | V |
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 300 | 550 | mV |
| PCI/PCIF at 3.3V | | | | | |
| T _{DC} | PCI Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | Spread Disabled PCIF/PCI Period | Measurement at 1.5V | 29.99700 | 30.00300 | ns |
| T _{PERIODSS} | Spread Enabled PCIF/PCI Period | Measurement at 1.5V | 30.08421 | 30.23459 | ns |
| T _{PERIODAbs} | Spread Disabled PCIF/PCI Period | Measurement at 1.5V | 29.49700 | 30.50300 | ns |
| T _{PERIODSSAbs} | Spread Enabled PCIF/PCI Period | Measurement at 1.5V | 29.56617 | 30.58421 | ns |
| T _{HIGH} | Spread Enabled PCIF and PCI high time | Measurement at 2V | 12.27095 | 16.27995 | ns |
| T _{LOW} | Spread Enabled PCIF and PCI low time | Measurement at 0.8V | 11.87095 | 16.07995 | ns |
| T _{HIGH} | Spread Disabled PCIF and PCI high time | Measurement at 2.0V | 12.27365 | 16.27665 | ns |
| T _{LOW} | Spread Disabled PCIF and PCI low time | Measurement at 0.8V | 11.87365 | 16.07665 | ns |
| T _R / T _F | PCIF/PCI Rising/Falling Slew Rate | Measured between 0.8V and 2.0V | 1.0 | 4.0 | V/ns |
| T _{SKEW} | Any PCI clock to Any PCI clock Skew | Measurement at 1.5V | – | 1000 | ps |
| T _{CCJ} | PCIF and PCI Cycle to Cycle Jitter | Measurement at 1.5V | – | 500 | ps |
| L _{ACC} | PCIF/PCI Long Term Accuracy | Measurement at 1.5V | – | 100 | ppm |
| 48_M at 3.3V | | | | | |
| T _{DC} | Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | Period | Measurement at 1.5V | 20.83125 | 20.83542 | ns |
| T _{PERIODAbs} | Absolute Period | Measurement at 1.5V | 20.48125 | 21.18542 | ns |
| T _{HIGH} | 48_M High time | Measurement at 2V | 8.216563 | 11.15198 | ns |
| T _{LOW} | 48_M Low time | Measurement at 0.8V | 7.816563 | 10.95198 | ns |
| T _R / T _F | Rising and Falling Edge Rate | Measured between 0.8V and 2.0V | 1.0 | 2.0 | V/ns |
| T _{CCJ} | Cycle to Cycle Jitter | Measurement at 1.5V | – | 350 | ps |
| L _{ACC} | 48M Long Term Accuracy | Measurement at 1.5V | – | 100 | ppm |
| 27M_NSS/27M_SS at 3.3V | | | | | |
| T _{DC} | Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | Spread Disabled 27M Period | Measurement at 1.5V | 37.03594 | 37.03813 | ns |
| | Spread Enabled 27M Period | Measurement at 1.5V | 37.03594 | 37.03813 | ns |
| T _R / T _F | Rising and Falling Edge Rate | Measured between 0.4V and 2.0V | 1.0 | 4.0 | V/ns |
| T _{CCJ} | Cycle to Cycle Jitter | Measurement at 1.5V | – | 200 | ps |
| L _{ACC} | 27_M Long Term Accuracy | Measured at crossing point V _{OX} | – | 50 | ppm |
| REF | | | | | |
| T _{DC} | REF Duty Cycle | Measurement at 1.5V | 45 | 55 | % |

AC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|----------------------------------|-----------------------------------|--------------------------------|----------|----------|------|
| T _{PERIOD} | REF Period | Measurement at 1.5V | 69.82033 | 69.86224 | ns |
| T _{PERIODAbs} | REF Absolute Period | Measurement at 1.5V | 68.83429 | 70.84826 | ns |
| T _{HIGH} | REF High time | Measurement at 2V | 29.97543 | 38.46654 | ns |
| T _{LOW} | REF Low time | Measurement at 0.8V | 29.57543 | 38.26654 | ns |
| T _R / T _F | REF Rising and Falling Edge Rate | Measured between 0.8V and 2.0V | 1.0 | 4.0 | V/ns |
| T _{SKEW} | REF Clock to REF Clock | Measurement at 1.5V | – | 500 | ps |
| T _{CCJ} | REF Cycle to Cycle Jitter | Measurement at 1.5V | – | 1000 | ps |
| L _{ACC} | Long Term Accuracy | Measurement at 1.5V | – | 100 | ppm |
| ENABLE/DISABLE and SET-UP | | | | | |
| T _{STABLE} | Clock Stabilization from Power-up | | – | 1.8 | ms |
| T _{SS} | Stopclock Set-up Time | | 10.0 | – | ns |

Test and Measurement Set-up

For PCI Single-ended Signals and Reference

The following diagram shows the test load configurations for the single-ended PCI, USB, and REF output signals.

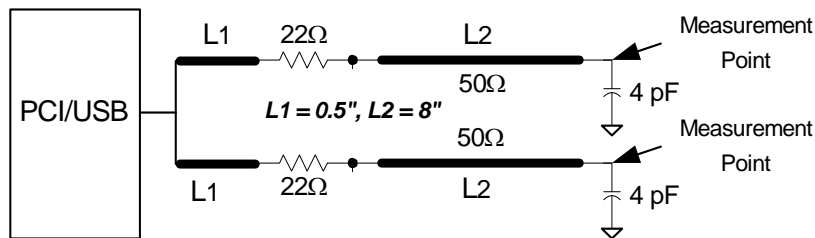


Figure 14. Single-ended PCI and USB Double Load Configuration

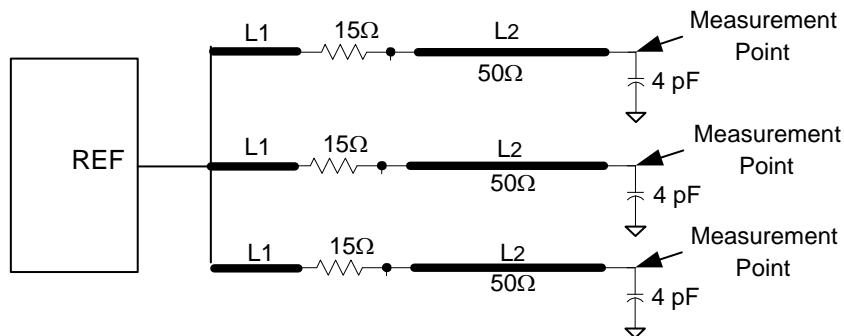


Figure 15. Single-ended REF Triple Load Configuration

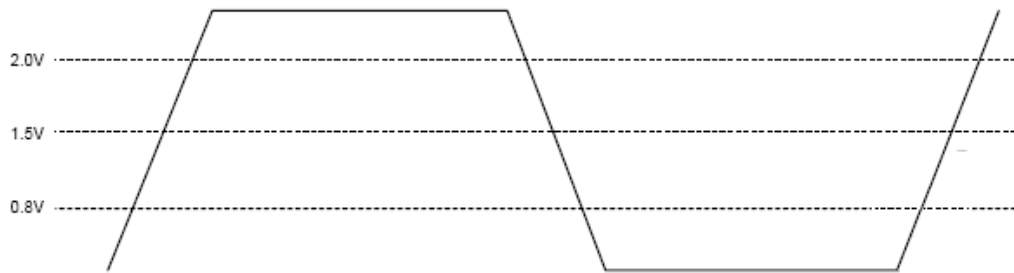


Figure 16. Single-ended Output Signals (for AC Parameters Measurement)

For CPU, SRC, and DOT96 Signals and Reference

This diagram shows the test load configuration for the differential CPU and SRC outputs

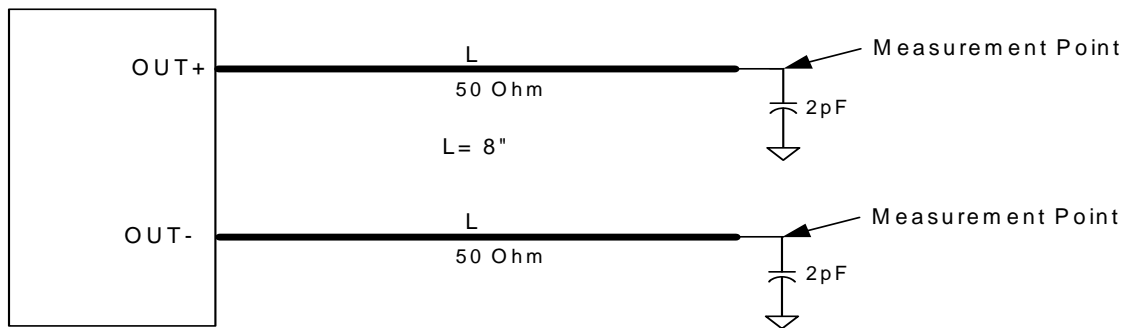


Figure 17. 0.7V Differential Load Configuration

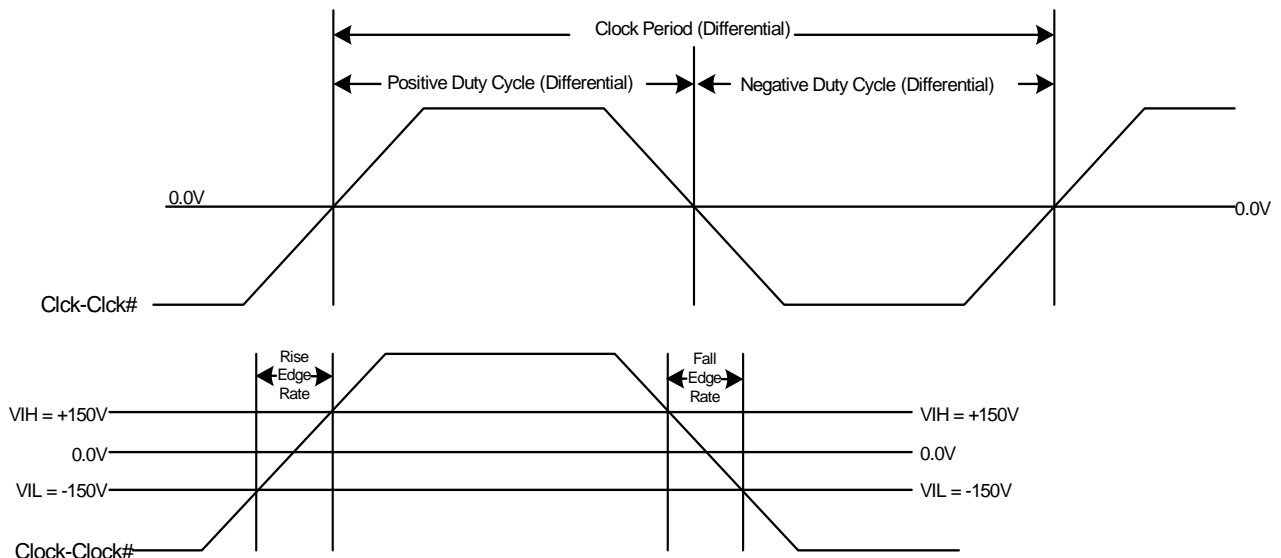


Figure 18. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

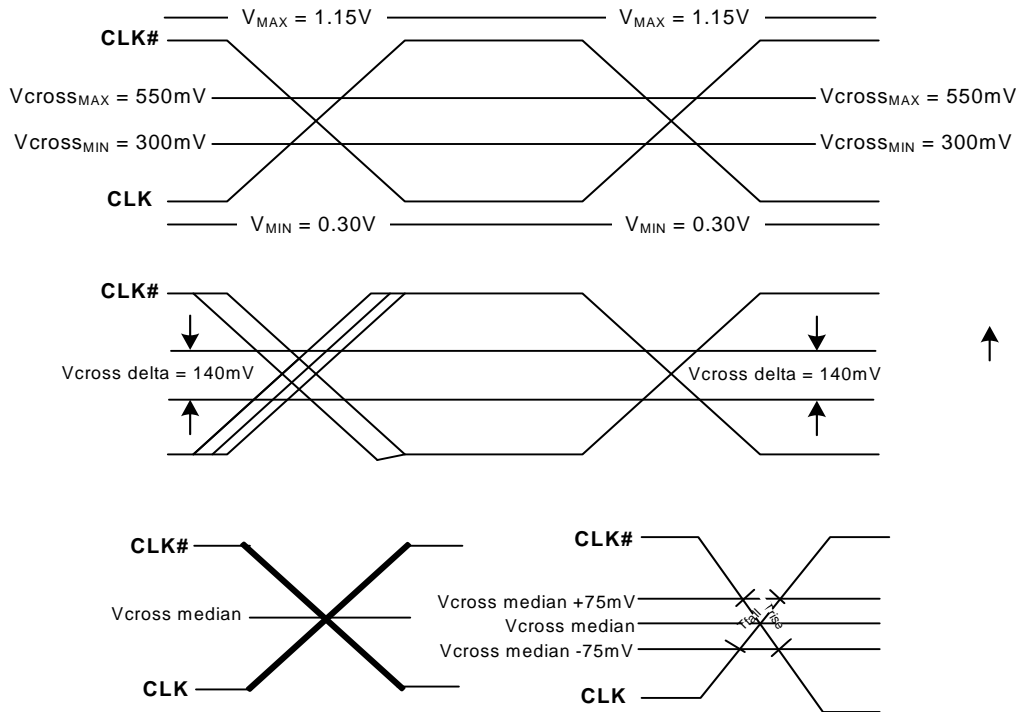


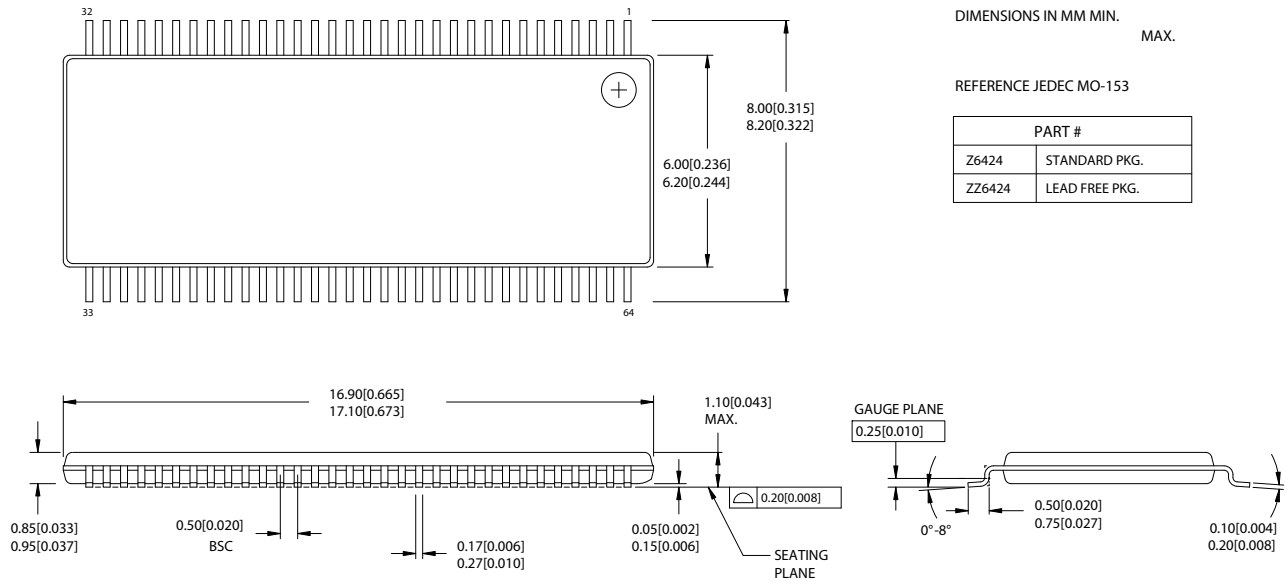
Figure 19. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

Ordering Information

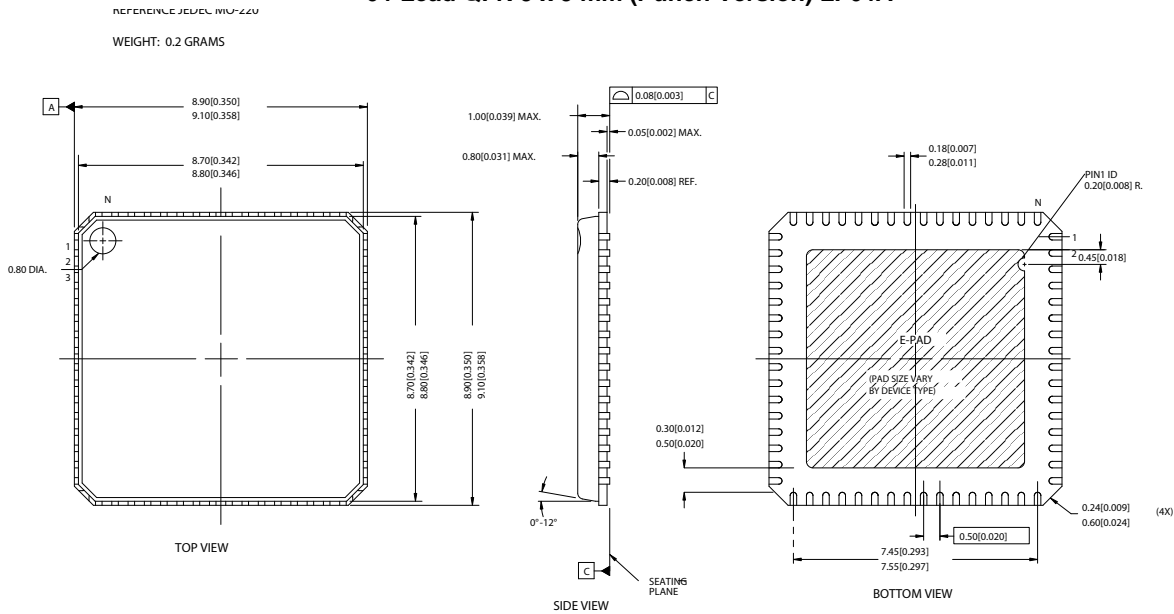
| Part Number | Package Type | Product Flow |
|------------------|----------------------------|------------------------|
| Lead-free | | |
| CY28548ZXC | 64-pin TSSOP | Commercial, 0° to 85°C |
| CY28548ZXCT | 64-pin TSSOP–Tape and Reel | Commercial, 0° to 85°C |
| CY28548LFXC | 64-pin QFN | Commercial, 0° to 85°C |
| CY28548LFXCT | 64-pin QFN–Tape and Reel | Commercial, 0° to 85°C |

Package Diagrams

64-Lead Thin Shrunken Small Outline Package (6 mm x 17 mm) Z64



64-Lead QFN 9 x 9 mm (Punch Version) LF64A





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