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W173

Tape Drive Frequency Timing Generator

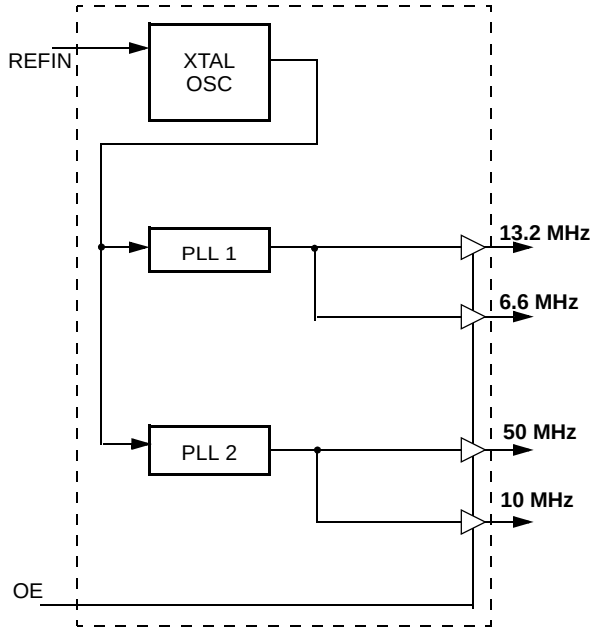
Features

- **Four derived outputs at frequencies specified by Hewlett Packard Computer Peripherals Bristol/Boise (CPB)**
- **Less than ±250 ps cycle-to-cycle jitter (13.2 MHz clock excluded derated to ±400 ps)**
- **Less than ±350 ps absolute jitter**
- **Supports 3.3V operation**
- **TTL compatible logic: V_{IL} = 0.8V max., V_{IH} = 2.0V min., V_{OL} = 0.4V max., and V_{OH} = 2.4V min.**
- **OE pin has internal pull-up**
- **45/55% duty cycle on all outputs**
- **15Ω output drivers**
- **Accepts 26.5625 MHz input reference**
- **Built-in crystal oscillator circuit. Capacitive load presented to the crystal is approximately 14 pF**
- **Outputs designed to drive 30 pF loads**
- **Available in 16-pin SOIC package**

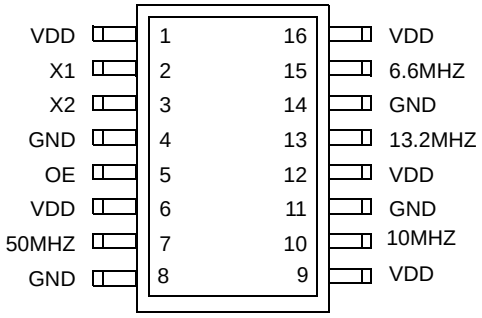
Functional Description

The W173 has been defined to meet the timing signal requirements for Hewlett Packard CPB tape drive system.

Block Diagram



Pin Configuration



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Pin Definitions [1]

Pin Name	Pin No.	Pin Type	Pin Description
OE	5	I	***Output Enable:*** When LOW, this input signal puts all outputs into a high-impedance state.
13.2MHZ	13	O	***Clock Output:*** Provides a TTL-level timing signal proportional in frequency to the input signal. For a 26.5625 MHz reference, the frequency will be 13.2 MHz.
6.6MHZ	15	O	***Clock Output:*** Provides a TTL-level timing signal proportional in frequency to the input signal. For a 26.5625 MHz reference, the frequency will be 6.6 MHz.
10MHZ	10	O	***Clock Output:*** Provides a TTL-level timing signal proportional in frequency to the input signal. For a 26.5625 MHz reference, the frequency will be 10.0 MHz.
50MHZ	7	O	***Clock Output:*** Provides a TTL-level timing signal proportional in frequency to the input signal. For a 26.5625 MHz reference, the frequency will be 50.0 MHz.
X1	2	I	***External Crystal Connection:*** This pin has dual functions. It can be used as an external 26.5625 MHz crystal connection or as an external reference frequency input.
X2	3	O	***External Crystal Connection:*** An input connection for an external 26.5625 MHz crystal. If using an external reference, this pin must be left unconnected.
VDD	1, 6, 9, 12, 16	P	***Power Supply Connections***: Connect both V_{DD} pins to the same voltage, either 3.3V or 5.0V. Each V_{DD} pin should have a decoupling capacitor (such as 0.1 µF) placed as close to the pin as possible.
GND	4, 8, 11, 14	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Note:
1. All inputs, except X1 or X2, have an internal pull-up resistor. Unconnected inputs will assume a logic HIGH condition.

Power Supply Connections

The recommended single voltage power supply configuration for the W173 is shown schematically in *Figure 1*. These recommendations should be followed to both ensure adequate device performance and to control EMI. The major considerations can be summarized as follows:

1. Decoupling Capacitor—A 0.1-µF decoupling capacitor should be used for each V_{DD} pin to minimize crosstalk between output frequencies. The trace to the V_{DD} pin and to the ground via should be as short as possible.
2. Ferrite Bead (FB)—A common supply connection should be used for all W173 V_{DD} pins. A ferrite bead should be used on this common supply as shown to remove high frequency system noise.
3. 22-µF Supply Filter Capacitor—The 22-µF capacitor filters low frequency supply noise that may produce clock output jitter. Depending on the particular application, this capacitor may not be required; its use should be considered optional. Mounting pads should be implemented in PCB layout. Use of this capacitor in production should be determined upon prototype evaluation.
4. PCB power supply traces should be at least 20 mils wide to assure adequate trade impedance recommend Power Supply Schematic–Single Voltage Supply Operation.

Ground Connections

All ground connections should be made to the main system ground plane. These connections should be as short as possible. No cuts should be made in the ground plane around the clock device since this can increase system EMI and reduce clock performance.

Clock Output Lines

1. The clock line width should be set to provide a 60Ω trace impedance. This width will vary depending on the PCB material; the PCB supplier can suggest what width to use for a 60Ω clock line. In general, an 8-mil trace will provide a 60Ω impedance on a multi-level board.
2. The series termination resistor (sometimes called “damping resistor”) must be placed in series with the clock line as close to the clock output as possible (within one inch).
3. Assume an output resistance from the W173 of 40Ω, choose series resistors appropriate to the number of driven traces.

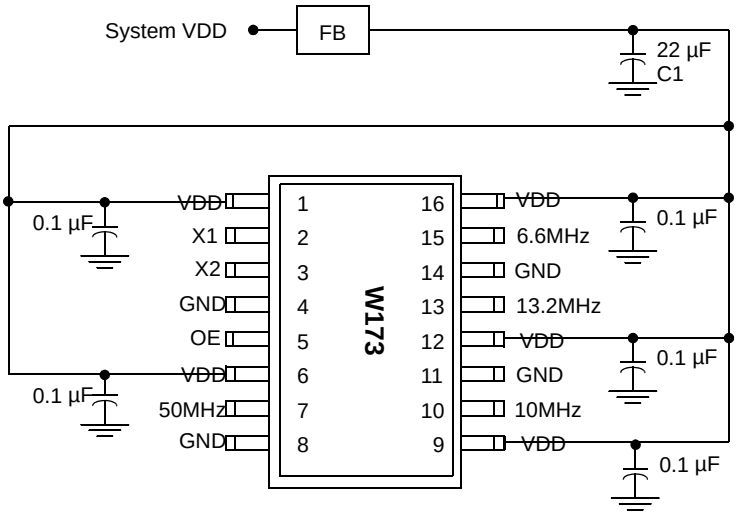

Figure 1. Test Circuit

Absolute Maximum Ratings[2]

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Table 1:

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on Any Pin with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V±5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current	Note: CLK output = 50.0 MHz output loaded			40	mA
V_{IL}	Input Low Voltage	V_{CC} = 5.0V			0.8	V
V_{IH}	Input High Voltage	V_{CC} = 5.0V	2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	3.1			V
I_{IL}	Input Low Current				10	µA
I_{IH}	Input High Current				10	µA
R_P	Input Pull-up Resistor	V_{IN} = 0V		500		kΩ
C_I	Input Capacitance	Except X1 and X2			6	pF
L_I	Input Inductance	Except X1 and X2			7	nH
C_L	XTAL Load Capacitance	Total load to crystal		12		pF

AC Electrical Characteristics: T_A = 0°C to +70°C, V_{CC} = 3.3V±5%[3]

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Clock Outputs						
t_{JC}	Output Clock Jitter, Cycle-to-Cycle	Excluding 13.2-MHz output		±175	±250	ps
Z_O	Output Buffer Impedance			40		W
d_T	Output Duty Cycle		45	50	55	%
t_R	Rise Time	Between 0.4V and 2.4V	0.8	1.5	4.0	V/ns
t_F	Fall Time	Between 2.4V and 0.4V	0.8	1.5	4.0	V/ns
t_{PU}	Stabilization Time from Power-Up	To within 0.1% of final frequency		1.5	3.0	ms
f_A	Long Term Output Frequency Stability	Over V_{CC} and T_A range			0.01	%

Note:
2. **Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. All AC tests are performed using the circuit shown in *Figure 1* to simulate typical system load conditions. Measurements are taken at the load. Threshold voltage for timing measurements is 1.5V.

Ordering Information

Ordering Code	Package Type
W173G	16-pin SOIC (150 mil)
W173GT	16-pin SOIC (150 mil) - Tape and Reel
Lead Free	
CYW173SXC	16-pin SOIC (150 mil)
CYW173SXCT	16-pin SOIC (150 mil) - Tape and Reel

Package Drawing and Dimensions

16-Lead (150-Mil) SOIC S16.15