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Low Voltage 2.5/3.3 V Differential ECL/PECL/HSTL Fanout Buffer

MC100ES6111

LOW-VOLTAGE 1:10 DIFFERENTIAL ECL/PECL/HSTL CLOCK FANOUT DRIVER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-04

AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-04

The MC100ES6111 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6111 supports various applications that require distribution of precisely aligned differential clock signals. Using SiGe:C technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:10 differential clock distribution
- 35 ps maximum device skew
- Fully differential architecture from input to all outputs
- SiGe:C technology supports near-zero output skew
- Supports DC to 2.7 GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL/HSTL compatible differential clock inputs
- Single 3.3 V, –3.3 V, 2.5 V or –2.5 V supply
- Standard 32-lead LQFP package
- 32-lead Pb-free package available
- Industrial temperature range
- Pin and function compatible to the MC100EP111

Functional Description

The MC100ES6111 is designed for low skew clock distribution systems and supports clock frequencies up to 2.7 GHz. The device accepts two clock sources. The CLKA input can be driven by ECL or PECL compatible signals, the CLKB input accepts HSTL compatible signals. The selected input signal is distributed to 10 identical, differential ECL/PECL outputs. If V_{BB} is connected to the CLKA input and bypassed to GND by a 10 nF capacitor, the MC100ES6111 can be driven by single-ended ECL/PECL signals utilizing the V_{BB} bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6111 can be operated from a single 3.3 V or 2.5 V supply. As most other ECL compatible devices, the MC100ES6111 supports positive (PECL) and negative (ECL) supplies. The MC100ES6111 is pin and function compatible to the MC100EP111.

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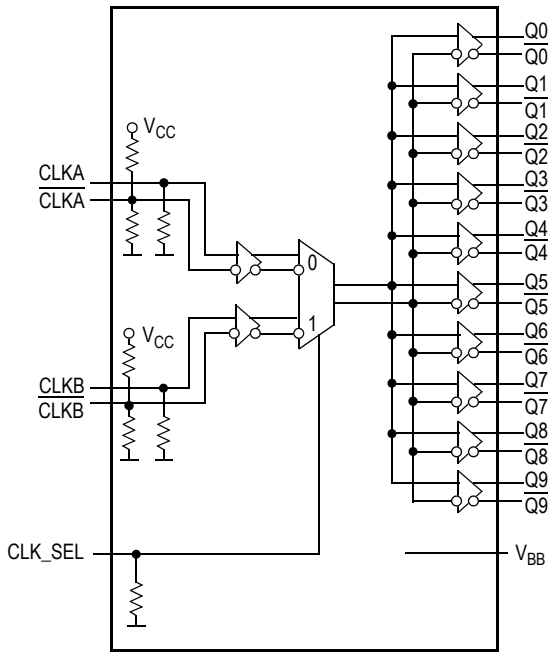


Figure 1. MC100ES6111 Logic Diagram

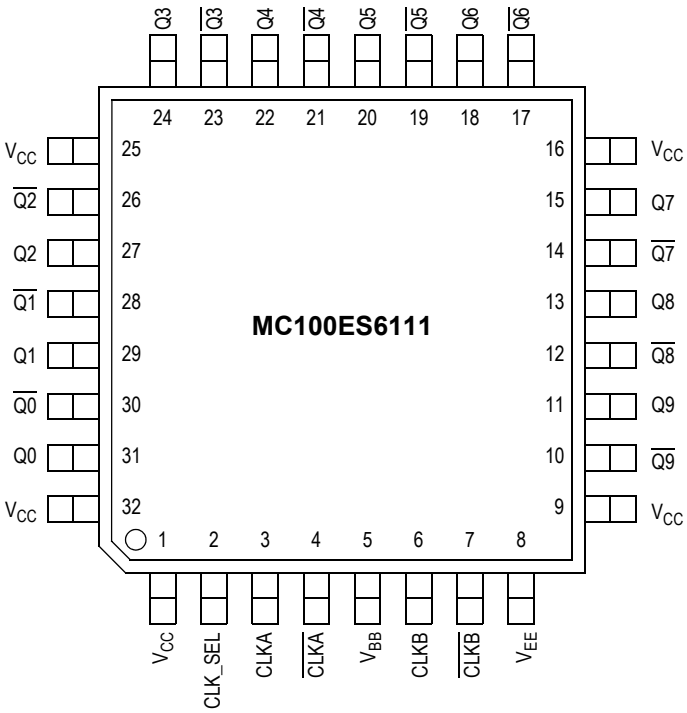


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLKA, $\overline{\text{CLKA}}$	Input	ECL/PECL	Differential reference clock signal input
CLKB, $\overline{\text{CLKB}}$	Input	HSTL	Alternative differential reference clock signal input
CLK_SEL	Input	ECL/PECL	Active clock input select
Q[0–9], $\overline{\text{Q[0–9]}}$	Output	ECL/PECL	Differential clock outputs
V_{EE}[1]	Supply		Negative power supply
V_{CC}	Supply		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
V_{BB}	Output	DC	Reference voltage output for single ended ECL or PECL operation

1. In ECL mode (negative power supply mode), V_{EE} is either –3.3 V or –2.5 V and V_{CC} is connected to GND (0 V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0 V) and V_{CC} is either +3.3 V or +2.5 V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}).

Table 2. Function Table

Control	Default	0	1
CLK_SEL	0	CLKA, $\overline{\text{CLKA}}$ input pair is active. CLKA can be driven by ECL or PECL compatible signals.	CLKB, $\overline{\text{CLKB}}$ input pair is active. CLKB can be driven by HSTL compatible signals.

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	
T_{Func}	Functional Temperature Range	T_A = –40	T_J = +110	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2[1]		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	4000			V	
CDM	ESD Protection (Charged Device Model)	2000			V	
LU	Latch-up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient					
	JESD 51–3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51–6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T_J	Operating Junction Temperature[2] (Continuous Operation) MTBF = 9.1 years			110	°C	

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase
2. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this data sheet for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6111 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6111 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. PECL/HSTL DC Characteristics (V_{CC} = 2.5 V ± 5% or V_{CC} = 3.3 V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Control Input CLK_SEL						
V_{IL}	Input Voltage Low	V_{CC} – 1.810		V_{CC} – 1.475	V	
V_{IH}	Input Voltage High	V_{CC} – 1.165		V_{CC} – 0.880	V	
I_{IN}	Input Current(1)			100	μA	V_{IN} = V_{IL} or V_{IN} = V_{IH}
Clock Input Pair CLKA, $\overline{\text{CLKA}}$ (PECL differential signals)						
V_{PP}	Differential Input Voltage(2)	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage(3)	1.0		V_{CC} – 0.3	V	Differential operation
I_{IN}	Input Current(1)			100	μA	V_{IN} = V_{IL} or V_{IN} = V_{IH}
Clock Input Pair CLKB, $\overline{\text{CLKB}}$ (HSTL differential signals)						
V_{DIF}	Differential Input Voltage(4) V_{CC} = 3.3 V V_{CC} = 2.5 V	 0.4 0.4			 V V	
V_X	Differential Cross Point Voltage(5)	0	0.68 – 0.9	V_{CC} – 1.1	V	
I_{IN}	Input Current			200	μA	V_{IN} = V_X ± 0.2 V
PECL Clock Outputs (Q0-9, $\overline{\text{Q0-9}}$)						
V_{OH}	Output High Voltage	V_{CC} – 1.2	V_{CC} – 1.005	V_{CC} – 0.7	V	I_{OH} = –30 mA(6)
V_{OL}	Output Low Voltage V_{CC} = 3.3 V±5% V_{CC} = 2.5 V±5%	V_{CC} – 1.9 V_{CC} – 1.9	V_{CC} – 1.705 V_{CC} – 1.705	V_{CC} – 1.5 V_{CC} – 1.3	V	I_{OL} = –5 mA(6)
Supply Current and V_{BB}						
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current(7)			100	mA	V_{EE} pin
V_{BB}	Output Reference Voltage	V_{CC} – 1.4		V_{CC} – 1.2	V	I_{BB} = 200 μA

1. Input have internal pullup/pulldown resistors which affect the input current.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
5. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
6. Equivalent to a termination of 50 Ω to V_{TT}.
7. I_{CC} calculation: I_{CC} = (number of differential output pairs used) x (I_{OH} + I_{OL}) + I_{EE}
   I_{CC} = (number of differential output pairs used) x (V_{OH} – V_{TT})/R_{load} + (V_{OL} – V_{TT})/R_{load} + I_{EE}

Table 6. ECL DC Characteristics (V_{EE} = –2.5 V ± 5% or V_{EE} = –3.3 V ± 5%, V_{CC} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Control Input CLK_SEL						
V_{IL}	Input Voltage Low	–1.810		–1.475	V	
V_{IH}	Input Voltage High	–1.165		–0.880	V	
I_{IN}	Input Current(1)			100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock Input Pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (ECL differential signals)						
V_{PP}	Differential Input Voltage(2)	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage(3)	V_{EE} + 1.0		–0.3	V	Differential operation
I_{IN}	Input Current(1)			100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL Clock Outputs (Q0-9, $\overline{\text{Q0-9}}$)						
V_{OH}	Output High Voltage	–1.2	–1.005	–0.7	V	I_{OH} = –30 mA(4)
V_{OL}	Output Low Voltage V_{EE} = –3.3 V ± 5% V_{EE} = –2.5 V ± 5%	–1.9 –1.9	–1.705 –1.705	–1.5 –1.3	V	I_{OL} = –5 mA(4)
Supply Current and V_{BB}						
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current(5)			100	mA	V_{EE} pin
V_{BB}	Output Reference Voltage	V_{CC} – 1.4		V_{CC} – 1.2	V	I_{BB} = 200 μA

1. Input have internal pullup/pulldown resistors which affect the input current.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. Equivalent to a termination of 50 Ω to V_{TT}.
5. I_{CC} calculation: I_{CC} = (number of differential output pairs used) x (I_{OH} + I_{OL}) + I_{EE}
   I_{CC} = (number of differential output pairs used) x ($V_{OH} – V_{TT}$)/R_{load} + ($V_{OL} – V_{TT}$)/R_{load} + I_{EE}

Table 7. AC Characteristics (ECL: V_{EE} = –3.3 V ± 5% or V_{EE} = –2.5 V ± 5%, V_{CC} = GND) or (HSTL/PECL: V_{CC} = 3.3 V ± 5% or V_{CC} = 2.5 V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock Input Pair CLKA, $\overline{CLKA}$ (PECL or ECL differential signals)						
V_{PP}	Differential Input Voltage[2] (peak-to-peak)	0.15		1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[3] PECL	V_{EE} + 1.0		V_{CC} – 0.3	V	
f_{CLK}	Input Frequency[4]			2.7	GHz	Differential
t_{PD}	Propagation Delay CLKA or CLKB to Q0–9	280	400	530	ps	Differential
Clock Input Pair CLKB, $\overline{CLKB}$ (HSTL differential signals)						
V_{DIF}	Differential Input Voltage (peak-to-peak)[5]	0.4		1.0	V	
V_X	Differential Input Crosspoint Voltage[6]	V_{EE} + 0.1	V_{EE} + 0.68 V_{EE} + 0.9	V_{EE} + 2.1	V	
f_{CLK}	Input Frequency			2.7	GHz	Differential
t_{PD}	Propagation Delay CLKB to Q0-9	280	400	530	ps	Differential
ECL Clock Outputs (Q0-9, $\overline{Q0\text{-}9}$)						
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak) f_O < 300 MHz f_O < 1.5 GHz f_O < 2.7 GHz	 0.45 0.3 0.18	 0.72 0.55 0.37	 0.95 0.95 0.95	 V V V	
$t_{sk(O)}$	Output-to-Output Skew			35	ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part) f_O < 1.5 GHz f_O > 1.5 GHz			150 250	ps ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter RMS (1σ)			1	ps	
$t_{sk(P)}$	Output Pulse Skew[7]			75	ps	
t_r, t_f	Output Rise/Fall Time	0.05		0.3	ns	20% to 80%

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
3. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
4. The MC100ES6111 is fully operational up to 3.0 GHz and is characterized up to 2.7 GHz.
5. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
6. V_X (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF} (AC) impacts the device propagation delay, device and part-to-part skew.
7. Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

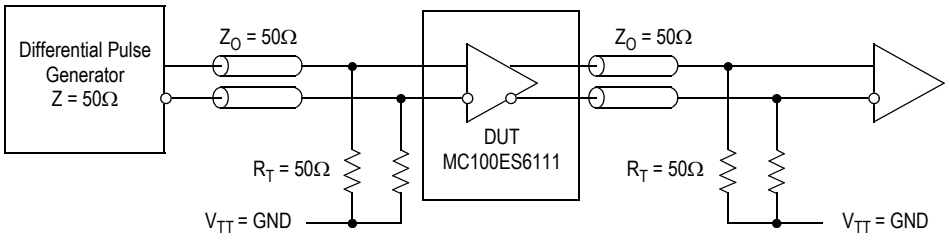


Figure 3. MC100ES6111 AC Test Reference

APPLICATIONS INFORMATION

Understanding the Junction Temperature Range of the MC100ES6111

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6111, the MC100ES6111 is specified, characterized and tested for the junction temperature range of T_J = 0°C to +110°C. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this data sheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 54.4°C/W (2s2p board, 200 ft/min airflow, see Table 4) and a typical power consumption of 610 mW (all outputs terminated 50 ohms to V_{TT}, V_{CC} = 3.3 V, frequency independent), the junction temperature of the MC100ES6111 is approximately T_A + 33°C, and the minimum ambient temperature in this example case calculates to –33°C (the maximum ambient temperature is 77°C, see Table 8). Exceeding the minimum junction temperature specification of the MC100ES6111 does not have a significant impact on the device functionality. However, the continuous use of the MC100ES6111 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the Freescale application note AN1545 for a power consumption calculation guideline.

Table 8 . Ambient Temperature Range (P_{tot} = 610 mW)

R_{thja} (2s2p board)		T_A, Min(1)	T_A, Max
Natural convection	59.0°C/W	–36°C	74°C
100 ft/min	54.4°C/W	–33°C	77°C
200 ft/min	52.5°C/W	–32°C	78°C
400 ft/min	50.4°C/W	–30°C	79°C
800 ft/min	47.8°C/W	–29°C	81°C

1. The MC100ES6111 device function is guaranteed from T_A = –40°C to T_J = 110°C

Maintaining Lowest Device Skew

The MC100ES6111 guarantees low output-to-output bank skew of 35 ps and a part-to-part skew of max. 250 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6111 is a mixed analog/digital product. The differential architecture of the MC100ES6111 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

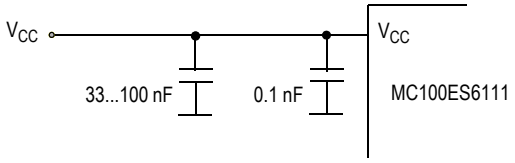
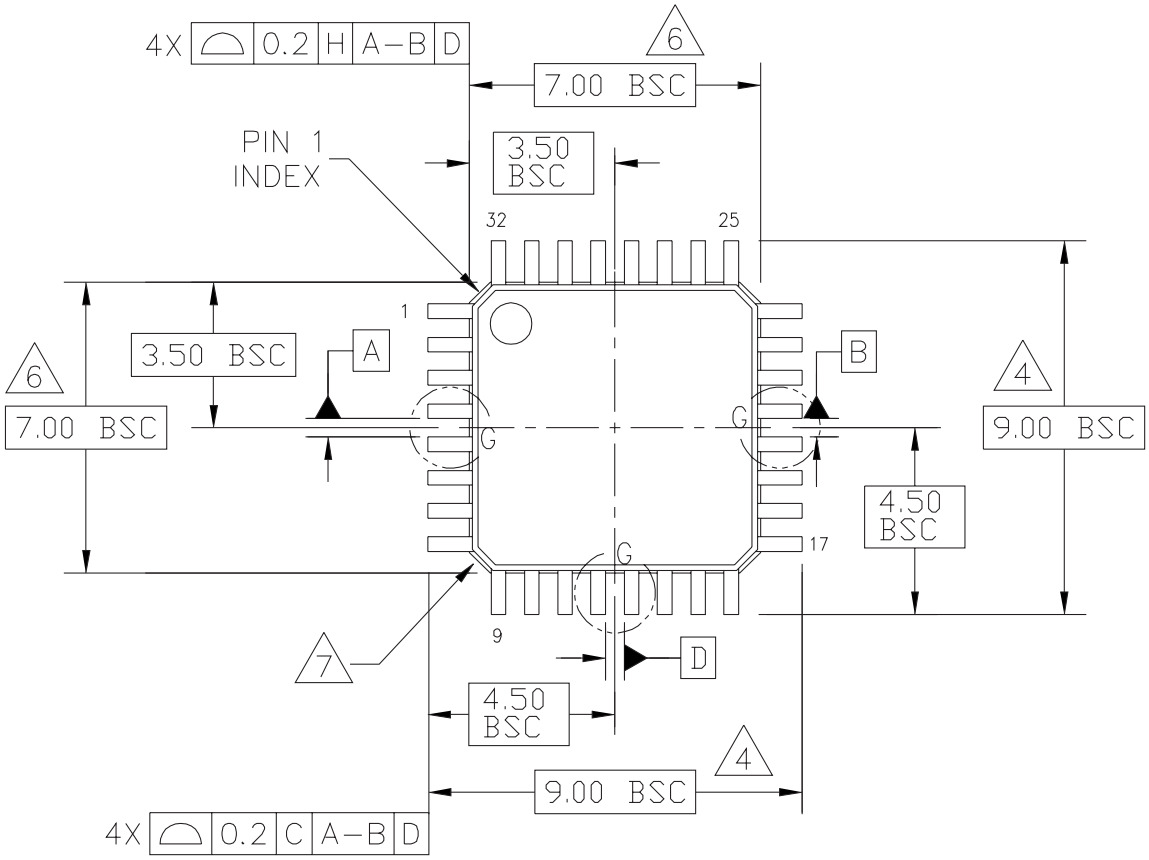
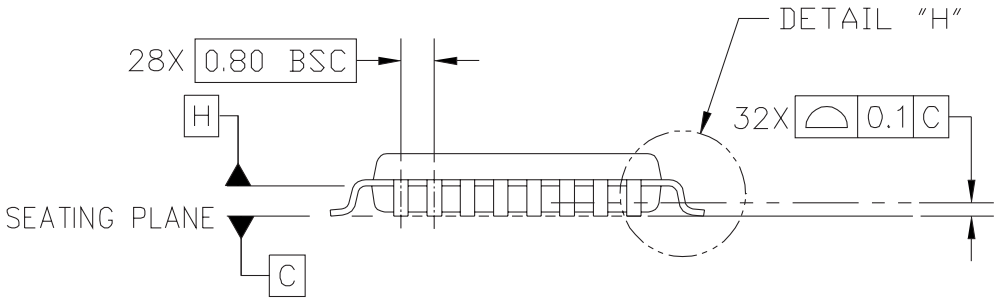


Figure 4. V_{CC} Power Supply Bypass

PACKAGE DIMENSIONS





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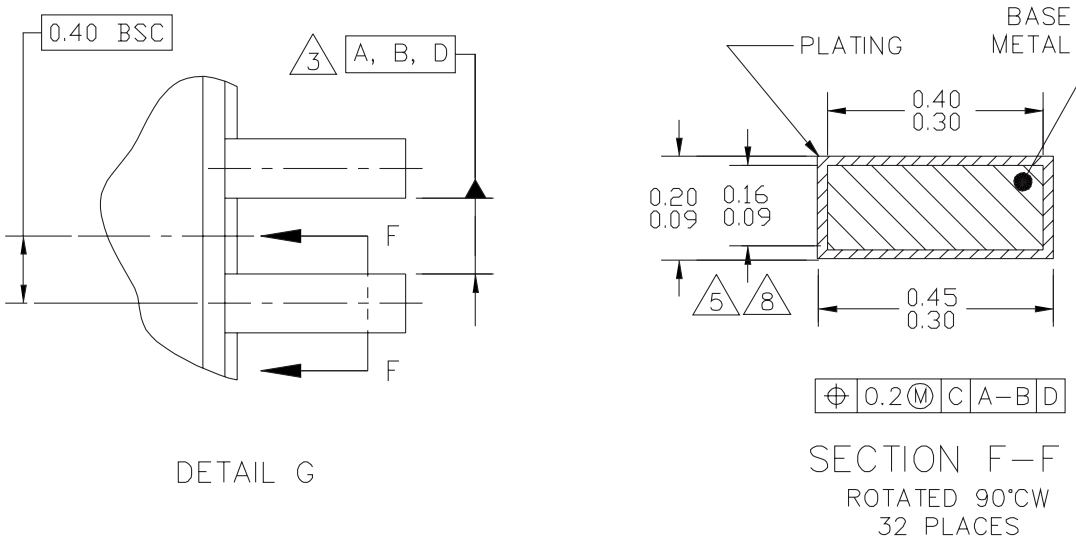
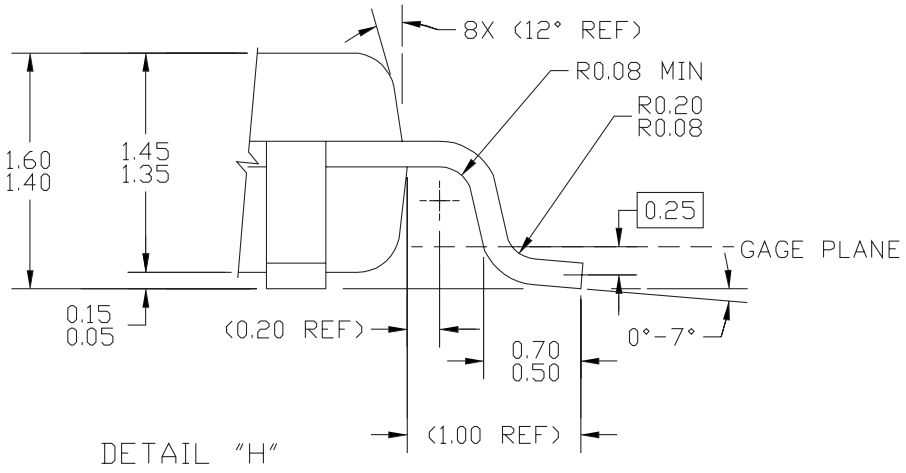
PACKAGE DIMENSIONS





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PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.

3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

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