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FAIRCHILD SEMICONDUCTOR®

January 2003
Revised January 2003

100EL11
5V ECL 1:2 Differential Fanout Buffer

General Description

The 100EL11 is a 5V 1:2 differential fanout buffer. One differential input signal is fanned out to two identical differential outputs. By supplying a constant reference level to one input pin a single ended input condition is created.

With inputs open or both inputs at V_{EE} the differential Q outputs default LOW and $\overline{Q}$ outputs default HIGH.

The 100 series is temperature compensated.

Features

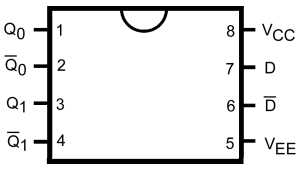
- Typical propagation delay of 265 ps
- Typical I_{EE} of 26 mA
- Typical Skew of 5 ps between outputs
- Internal pull-down resistors on inputs
- Fairchild MSOP-8 package is a drop-in replacement to ON TSSOP-8
- Meets or exceeds JEDEC specification EIA/JESD78 IC latch-up test
- Moisture Sensitivity Level 1
- ESD Performance:
  Human Body Model > 2000V
  Machine Model > 200V

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description
100EL11M	M08A	KEL11	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
100EL11M8 (Preliminary)	MA08D	KL11	8-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide

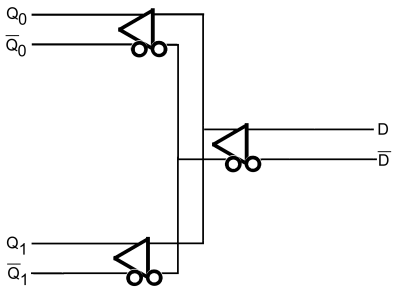
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Top View

Logic Diagram



Pin Descriptions

Pin Name	Description
Q_0, $\overline{Q}_0$, Q_1, $\overline{Q}_1$	ECL Data Outputs
D, $\overline{D}$	ECL Data Inputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

Absolute Maximum Ratings (Note 1)

PECL Supply Voltage (V_{CC}) V_{EE} = 0V	0.0V to +8.0V
NECL Supply Voltage (V_{EE}) V_{CC} = 0V	0.0V to −8.0V
PECL DC Input Voltage (V_I) V_{EE} = 0V	0.0V to +6.0V
NECL DC Input Voltage (V_I) V_{CC} = 0V	0.0V to −6.0V
DC Output Current (I_{OUT})	
Continuous	50 mA
Surge	100 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions

PECL Power Supply (V_{EE} = 0V)	V_{CC} = 4.2V to 5.5V
NECL Power Supply (V_{CC} = 0V)	V_{EE} = −4.2V to −5.5V
Free Air Operating Temperature (T_A)	−40°C to +85°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

100EL PECL DC Electrical Characteristics V_{CC} = 5.0V; V_{EE} = 0.0V (Note 2)

Symbol	Parameter	−40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		26	31		26	31		30	36	mA
V_{OH}	Output HIGH Voltage (Note 3)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 3)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current (Note 5)			150			150			150	µA
I_{IL}	Input LOW Current (Note 5)	0.5			0.5			0.5			µA

Note 2: Input and output parameters vary 1 to 1 with V_{CC}. V_{EE} can vary +0.8V/−0.5V.

Note 3: Outputs are terminated through a 50Ω Resistor to V_{CC} − 2.0V.

Note 4: V_{IHCMR} minimum varies 1 to 1 with V_{EE}. V_{IHCMR} maximum varies 1 to 1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPMIN} and 1V.

Note 5: Absolute value of the input HIGH and LOW current should not exceed the absolute value of the stated MIn or Max specification.

Note: Devices are designed to meet the DC specifications after thermal equilibrium has been established. Circuit is tested with air flow greater than 500LFPM maintained.

100EL NECL DC Electrical Characteristics V_{CC} = 0.0V; V_{EE} = –5.0V (Note 6)

Symbol	Parameter	–40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		26	31		26	31		30	36	mA
V_{OH}	Output HIGH Voltage (Note 7)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 7)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		-1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 8)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current (Note 9)			150			150			150	µA
I_{IL}	Input LOW Current (Note 9)	0.5			0.5			0.5			µA

Note 6: Input and output parameters vary 1 to 1 with V_{CC}. V_{EE} can vary +0.8V/–0.5V.

Note 7: Outputs are terminated through a 50Ω Resistor to V_{CC} – 2.0V.

Note 8: V_{IHCMR} minimum varies 1 to 1 with V_{EE}. V_{IHCMR} maximum varies 1 to 1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPMIN} and 1V.

Note 9: Absolute value of the input HIGH and LOW current should not exceed the absolute value of the stated Min or Max specification.

Note: Devices are designed to meet the DC specifications after thermal equilibrium has been established. Circuit is tested with air flow greater than 500LFPM maintained.

AC Electrical Characteristics V_{CC} = 5V; V_{EE} = 0.0V or V_{CC} = 0.0V; V_{EE} = –5V (Note 10)(Note 11)

Symbol	Parameter	–40°C			25°C			85°C			Units	Figure Number
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz	
t_{PLH}, t_{PHL}	Propagation Delay to Output	135	260	385	190	265	340	215	290	365	ps	Figure 1
t_{SKEW}	Within Device Skew (Note 12)		5			5	20		5	20	ps	
	Duty Cycle Skew (Note 13)		5			5	20		5	20		
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps	
V_{PP}	Input Swing	150		1000	150		100	150		1000	mV	Figure 1
t_r, t_f	Output Rise Times Q (20% to 80%)	100	225	350	100	225	350	100	225	350	ps	Figure 2

Note 10: V_{EE} can vary +0.8V / –0.5V.

Note 11: Measured using a 750 mV input swing centered at V_{CC} - 1.32V; 50% duty cycle clock source; $t_r = t_f$ = 250 ps (20% - 80%) at f_{IN} = 1 MHz. All loading with 50Ω to V_{CC} – 2.0V.

Note 12: Within-device skew defined as identical transitions on similar paths through a device.

Note 13: Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device under identical conditions.

Switching Waveforms

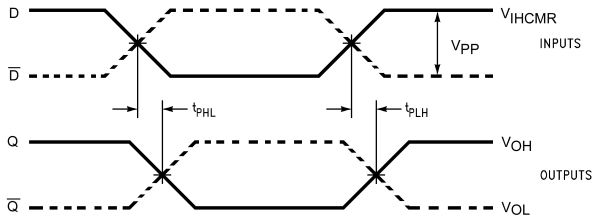


FIGURE 1. Differential to Differential Propagation Delay

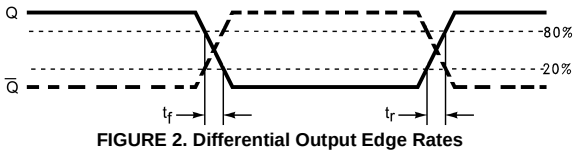
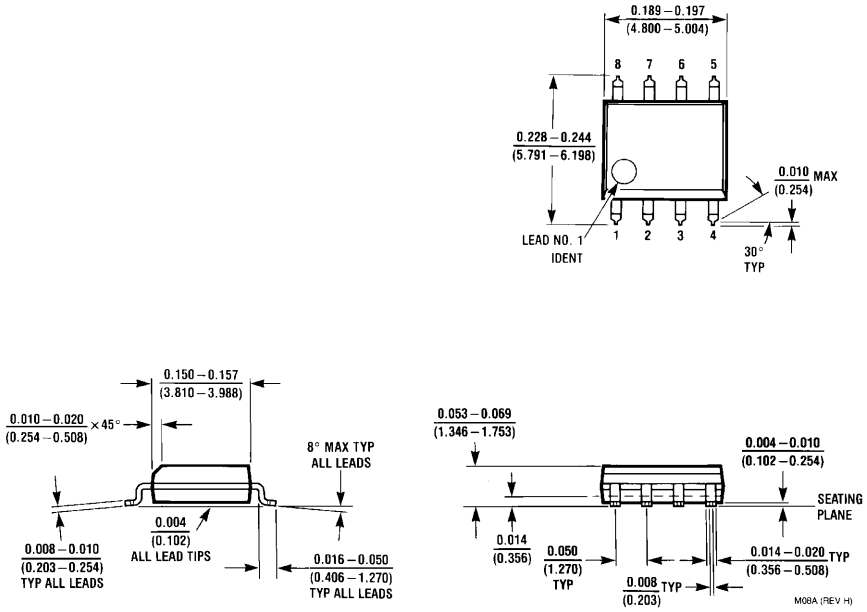


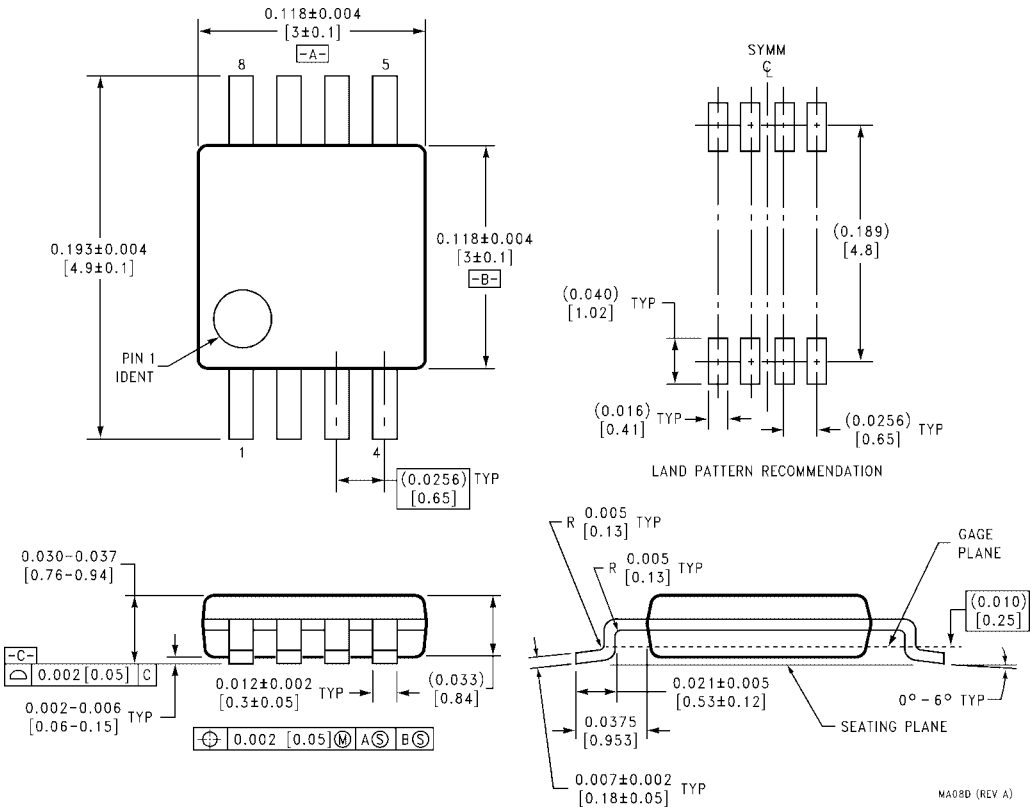
FIGURE 2. Differential Output Edge Rates

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide
Package Number MA08D