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2.5V or 3.3V, 200-MHz, 1:18 Clock Distribution Buffer

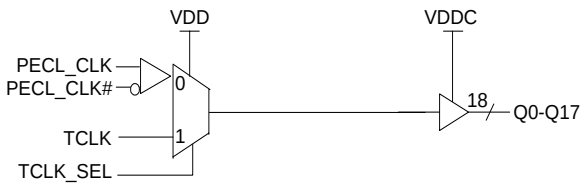
Features

- **200-MHz clock support**
- **LVPECL or LVCMOS/LVTTL clock input**
- **LVCMOS/LVTTL compatible inputs**
- **18 clock outputs: drive up to 36 clock lines**
- **60 ps typical output-to-output skew**
- **Dual or single supply operation:**
  - **3.3V core and 3.3V outputs**
  - **3.3V core and 2.5V outputs**
  - **2.5V core and 2.5V outputs**
- **Pin compatible with MPC940L, MPC9109**
- **Available in Commercial and Industrial temperature**
- **32-pin LQFP package**

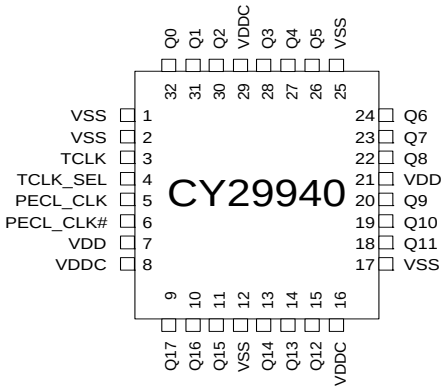
Description

The CY29940 is a low-voltage 200-MHz clock distribution buffer with the capability to select either a differential LVPECL or a LVCMOS/LVTTL compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The eighteen outputs are 2.5V or 3.3V LVCMOS/LVTTL compatible and can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:36. Low output-to-output skews make the CY29940 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	PWR	I/O	Description
5	PECL_CLK		I, PU	PECL Input Clock
6	PECL_CLK#		I, PD	PECL Input Clock
3	TCLK		I, PD	External Reference/Test Clock Input
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	VDDC	O	Clock Outputs
4	TCLK_SEL		I, PD	Clock Select Input. When LOW, PECL clock is selected and when HIGH TCLK is selected.
8, 16, 29	VDDC			3.3V or 2.5V Power Supply for Output Clock Buffers
7, 21	VDD			3.3V or 2.5V Power Supply
1, 2, 12, 17, 25	VSS			Common Ground

Note:
1. PD = Internal Pull-Down, PU = Internal Pull-up

Maximum Ratings[2]

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: .....–65°C to + 150°C

Operating Temperature: .....–40°C to +85°C

Maximum ESD Protection.....2 kV

Maximum Power Supply: 5.5V

Maximum Input Current: .....±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters[2]: V_{DD} = 3.3V ±5% or 2.5V ±5%, V_{DDC} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit.
V_{IL}	Input Low Voltage		V_{SS}	–	0.8	V
V_{IH}	Input High Voltage		2.0	–	V_{DD}	V
I_{IL}	Input Low Current[3]			–	–200	µA
I_{IH}	Input High Current[3]			–	200	µA
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK		500	–	1000	mV
V_{CMR}	Common Mode Range[4] PECL_CLK	V_{DD} = 3.3V	V_{DD} – 1.4	–	V_{DD} – 0.6	V
		V_{DD} = 2.5V	V_{DD} – 1.0	–	V_{DD} – 0.6	V
V_{OL}	Output Low Voltage[5, 6, 7]	I_{OL} = 20 mA	–	–	0.5	V
V_{OH}	Output High Voltage[5, 6, 7]	I_{OH} = –20 mA, V_{DDC} = 3.3V	2.4	–	–	V
		I_{OH} = –20 mA, V_{DDC} = 2.5V	1.8	–	–	V
I_{DDQ}	Quiescent Supply Current		–	5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3V, Outputs @ 150 MHz, CL = 15 pF	–	285	–	mA
		V_{DD} = 3.3V, Outputs @ 200 MHz, CL = 15 pF	–	335	–	
		V_{DD} = 2.5V, Outputs @ 150 MHz, CL = 15 pF	–	200	–	
		V_{DD} = 2.5V, Outputs @ 200 MHz, CL = 15 pF	–	240	–	
Z_{out}	Output Impedance	V_{DD} = 3.3V	8	12	16	Ω
		V_{DD} = 2.5V	10	15	20	
C_{in}	Input Capacitance		–	4	–	pF

Notes:

2. **Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the VCMR range and the input lies within the VPP specification. Driving series or parallel terminated 50Ω (or 50Ω to VDD/2) transmission lines
5. Outputs driving 50Ω transmission lines.
6. See *Figure 1 &2*.
7. 50% input duty cycle.

AC Parameters[8]: V_{DD} = 3.3V ±5% or 2.5V ±5%, V_{DDC} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit.
F_{max}	Input Frequency		–	–	–	200	MHz
t_{PD}	PECL_CLK to Q Delay[5, 6, 11] </=150 MHz	V_{DD} = 3.3V 85°C	t_{PHL}	2.0	–	3.2	ns
			t_{PLH}	2.1	–	3.4	
		V_{DD} = 3.3V 70°C	t_{PHL}	1.9	–	3.1	
			t_{PLH}	2.0	–	3.2	
		V_{DD} = 2.5V 85°C	t_{PHL}	2.5	–	5.2	
			t_{PLH}	2.6	–	5	
		V_{DD} = 2.5V 70°C	t_{PHL}	2.5	–	5	
			t_{PLH}	2.6	–	5	
t_{PD}	LVCMOS to Q Delay[5, 6, 11] </=150 MHz	V_{DD} = 3.3V 85°C	t_{PHL}	1.9	–	3	ns
			t_{PLH}	2.0	–	3.2	
		V_{DD} = 3.3V 70°C	t_{PHL}	1.8	–	2.9	
			t_{PLH}	1.8	–	3.1	
		V_{DD} = 2.5V 85°C	t_{PHL}	2.5	–	4	
			t_{PLH}	2.5	–	4	
		V_{DD} = 2.5V 70°C	t_{PHL}	2.3	–	3.8	
			t_{PLH}	2.3	–	3.8	
t_J	Total Jitter	V_{DD} = 3.3V @ 150MHz		–	–	10	ps
FoutDC	Output Duty Cycle[5, 6, 7]	FCLK < 134 MHz		–	–	55	%
		FCLK > 134 MHz		–	–	60	
T_{skew}	Output-to-Output Skew[5, 6]	V_{DD} = 3.3V		–	60	150	ps
		V_{DD} = 2.5V		–		200	
T_{skew}(pp)	Part-to-Part Skew[9]	PECL, V_{DDC} = 3.3V		–	–	1.4	ns
		PECL, V_{DDC} = 2.5V		–	–	2.2	
T_{skew}(pp)	Part-to-Part Skew[9]	TCLK, V_{DDC} = 3.3V		–	–	1.2	ns
		TCLK, V_{DDC} = 2.5V		–	–	1.7	
T_{skew}(pp)	Part to Part Skew[10]	PECL_CLK		–	–	850	ps
		TCLK		–	–	750	
t_R/t_F	Output Clocks Rise/Fall Time[5, 6]	0.7V to 2.0V, V_{DDC} = 3.3V		0.3	–	1.1	ns
		0.5V to 1.8V, V_{DDC} = 2.5V		0.3	–	1.2	

Notes:

8. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
9. Across temperature and voltage ranges, includes output skew.
10. For a specific temperature and voltage, includes output skew
11. Parameters tested @ 150 MHz.

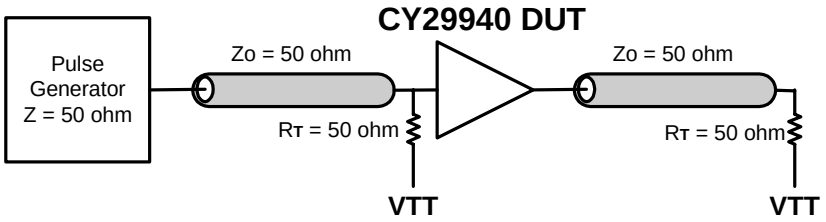


Figure 1. LVCMOS_CLK CY29940 Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

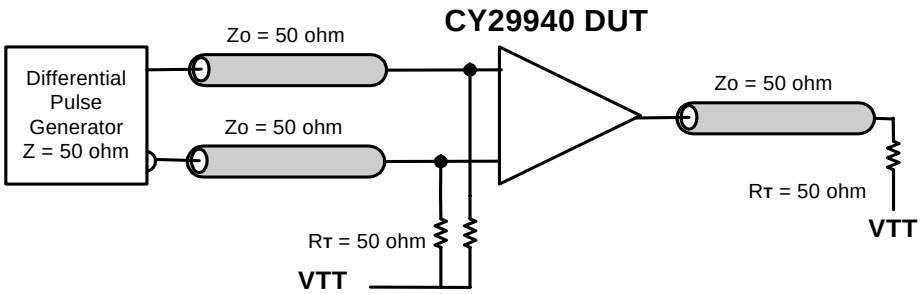


Figure 2. PECL_CLK CY29940 Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

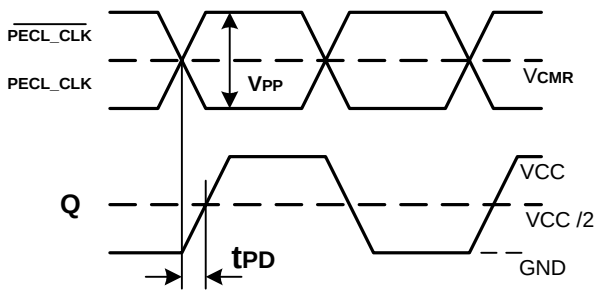


Figure 3. Propagation Delay (TPD) Test Reference

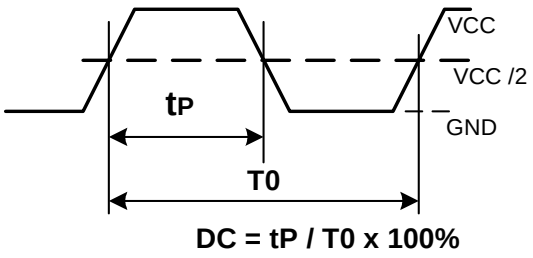


Figure 5. Output Duty Cycle (FoutDC)

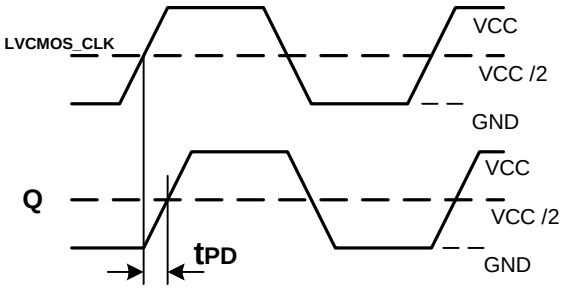


Figure 4. LVCMOS Propagation Delay (TPD) Test Reference

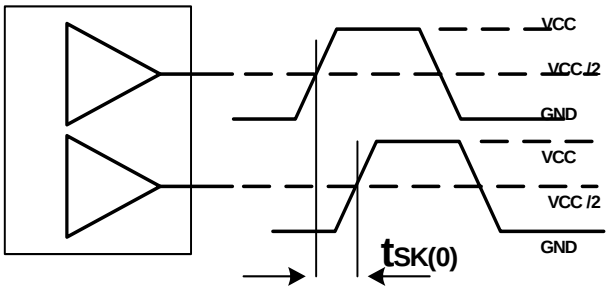


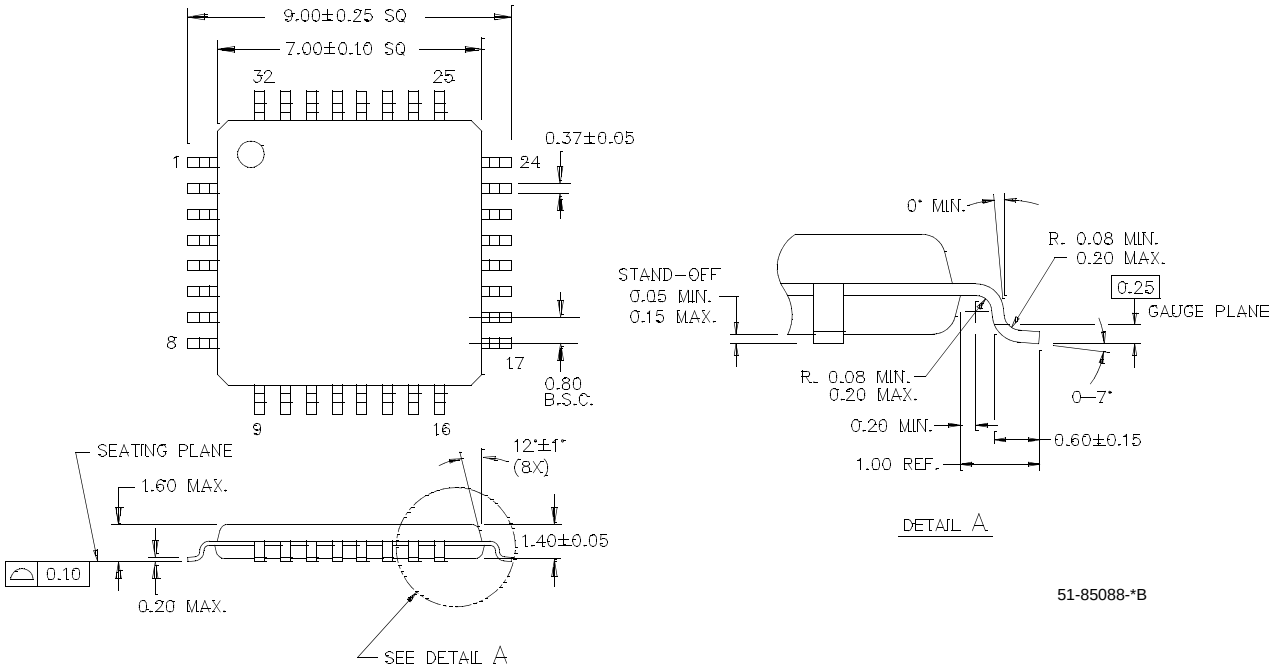
Figure 6. Output-to-Output Skew tsk(0)

Ordering Information

Part Number	Package Type	Production Flow
CY29940AI	32 Pin LQFP	Industrial, –40°C to +85°C
CY29940AIT	32 Pin LQFP – Tape and Reel	Industrial, –40°C to +85°C
CY29940AC	32 Pin LQFP	Commercial, 0°C to 70°C
CY29940ACT	32 Pin LQFP – Tape and Reel	Commercial, 0°C to 70°C
Lead-free		
CY29940AXI	32 Pin LQFP	Industrial, –40°C to +85°C
CY29940AXIT	32 Pin LQFP – Tape and Reel	Industrial, –40°C to +85°C
CY29940AXC	32 Pin LQFP	Commercial, 0°C to 70°C
CY29940AXCT	32 Pin LQFP – Tape and Reel	Commercial, 0°C to 70°C

Package Drawing and Dimensions

32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.4 mm A32.14



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Document History Page

Document Title: CY29940 2.5V or 3.3V, 200-MHz, 1:18 Clock Distribution Buffer Document Number: 38-07283				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111094	02/01/02	BRK	New data sheet
*A	116776	08/15/02	HWT	Incorporate results of final characterization using corporate methods, added output impedance on page 3 and added output duty cycle on page 4. Add commercial temperature range in the ordering information on page 6.
*B	122875	12/21/02	RBI	Add power up requirements to maximum rating information
*C	448379	See ECN	RGL	Add typical value for output-to-output skew Add Lead-free devices