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# MC10E411

## 5V ECL 1:9 Differential PECL/NECL RAMBus Clock Buffer

### Description

The MC10E411 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. The MC10E411's function and performance are similar to the popular MC10E111, with the added feature of 1.2 V output swings.

The output voltage swing of the E411 is larger than a standard ECL swing. The 1.2 V output swings provide a signal which can be AC coupled into RAMBus compatible input loads. The larger output swings are produced by lowering the  $V_{OL}$  of the device. With the exception of the lower  $V_{OL}$ , the E411 is identical to the MC10E111. Note that the larger output swings eliminate the possibility of temperature compensated outputs, thus the E411 is only available in the 10E style of ECL. In addition, because the  $V_{OL}$  is lower than standard ECL, the outputs cannot be terminated to  $-2.0$  V. This data sheet provides a few termination alternatives.

The device TPD is affected by the quantity of output pairs terminated with minimum occurring with only one output pair and increasing about 10 – 20 ps for all output pairs. Relative skew distribution is not affected as more pairs are terminated, but the increased TPD does shift the entire distribution. Unused output pairs should be left unterminated (open) to reduce power and switching noise.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

### Features

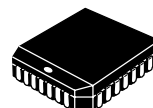
- 200 ps Part-to-Part Skew
- 50 ps Output-to-Output Skew
- Differential Design
- $V_{BB}$  Output
- Voltage Compensated Outputs
- PECL Mode Operating Range:  
 $V_{CC} = 4.5$  V to 5.5 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  
 $V_{CC} = 0$  V with  $V_{EE} = -4.5$  V to  $-5.5$  V
- Internal Input 50 k $\Omega$  Pulldown Resistors
- ESD Protection: Human Body Model; > 2 kV, Machine Model; > 200 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level: Pb = 1; Pb-Free = 3  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 1.125 in, Oxygen Index: 28 to 34
- Transistor Count = 180 devices
- Pb-Free Packages are Available\*

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



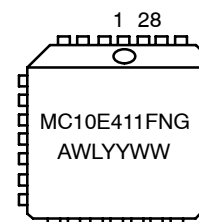
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PLCC-28  
FN SUFFIX  
CASE 776

### MARKING DIAGRAM\*



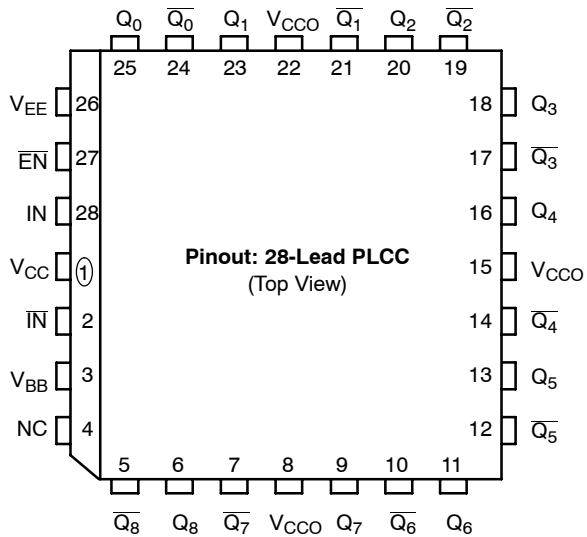
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

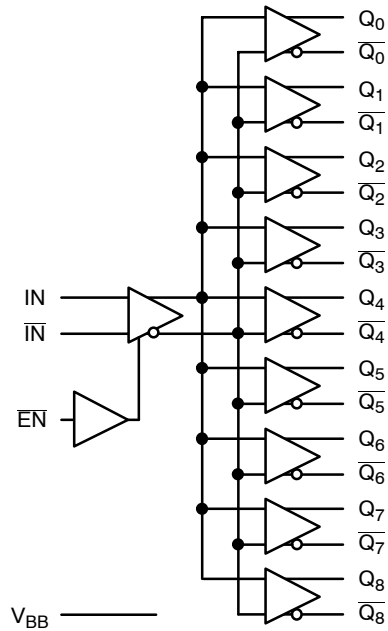
See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# MC10E411



All  $V_{CC}$  and  $V_{CCO}$  pins are tied together on the die  
 Warning: All  $V_{CC}$ ,  $V_{CCO}$ , and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

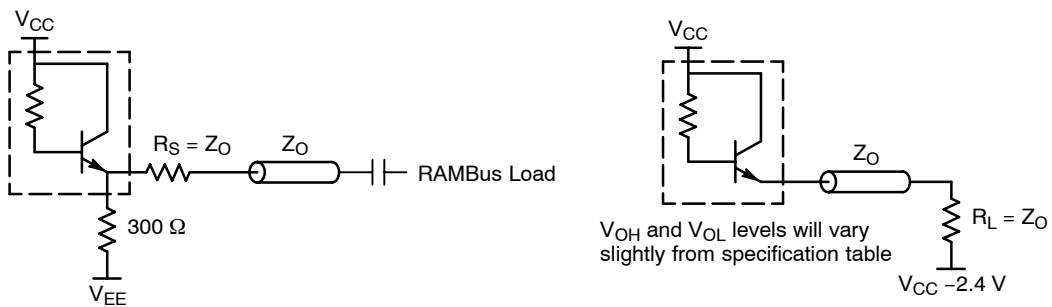
**Figure 1. 28-Lead Pinout Assignment**



**Figure 2. Logic Diagram**

**Table 1. PIN DESCRIPTION**

PIN	FUNCTION
IN, $\overline{IN}$	ECL Differential Input Pair
EN	ECL Enable
$Q_0, \overline{Q_0}$ – $Q_8, \overline{Q_8}$	ECL Differential Outputs
$V_{BB}$	Reference Voltage Output
$V_{CC}, V_{CCO}$	Positive Supply
$V_{EE}$	Negative Supply
NC	No Connect



**Figure 3. Termination Alternatives**

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**Table 2. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8	V
$V_I$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V V
$I_{out}$	Output Current	Continuous Surge		50 100	mA mA
$I_{BB}$	$V_{BB}$ Sink/Source			$\pm 0.5$	mA
$T_A$	Operating Temperature Range			0 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	PLCC-28 PLCC-28	63.5 43.5	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	PLCC-28	22 to 26	$^{\circ}\text{C}/\text{W}$
$T_{sol}$	Wave Solder Pb Pb-Free			265 265	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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**Table 3. 10E SERIES PECL DC CHARACTERISTICS**  $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		55	65		55	65		55	65	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
$V_{OL}$	Output LOW Voltage (Note 2)	2580	2750	2920	2620	2785	2950	2690	2865	3040	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
$V_{BB}$	Output Voltage Reference	3.62		3.73	3.65		3.75	3.69		3.81	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	3.4		4.6	3.4		4.6	3.4		4.6	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.5 V / -0.5 V.
2. Outputs are terminated through a 300  $\Omega$  resistor to  $V_{EE}$ .
3.  $V_{IHCMR}$  min and max vary 1:1 with  $V_{CC}$ .

**Table 4. 10E SERIES NECL DC CHARACTERISTICS**  $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 4)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		130	156		130	156		130	156	mA
$I_{EE}$	Power Supply Current		55	65		55	65		55	65	mA
$V_{OH}$	Output HIGH Voltage (Note 5)	-1020	-930	-840	-980	-895	-810	-910	-815	-720	mV
$V_{OL}$	Output LOW Voltage (Note 5)	-2420	-2250	-2080	-2380	-2215	-2050	-2310	-2135	-1960	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1170	-1005	-840	-1130	-970	-810	-1060	-890	-720	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.27	-1.35		-1.25	-1.31		-1.19	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6)	-1.6		-2.4	-1.6		-0.4	-1.6		-0.4	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.5 V / -0.5 V.
5. Outputs are terminated through a 300  $\Omega$  resistor to  $V_{EE}$ .
6.  $V_{IHCMR}$  min and max vary 1:1 with  $V_{CC}$ .

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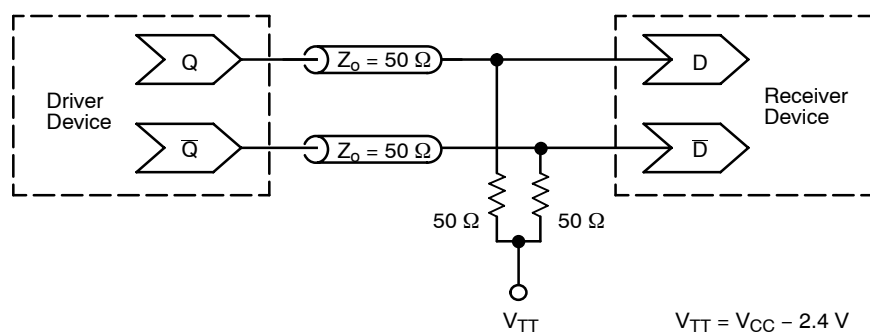
**Table 5. AC CHARACTERISTICS**  $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 7)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency		700			700			700		MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output IN (Differential) (Note 8) IN (Single-Ended) (Note 9) $\overline{EN}$ to Q	400 350 450		600 650 850	430 380 450		630 680 850	500 450 450		700 750 850	ps
$t_s$	Setup Time (Note 10) $\overline{EN}$ to IN	200	0		200	0		200	0		ps
$t_H$	Hold Time (Note 11) IN to $\overline{EN}$	0	-200		0	-200		0	-200		ps
$t_R$	Release Time (Note 12) $\overline{EN}$ to IN	300	100		300	100		300	100		ps
$t_{skew}$	Within-Device Skew (Note 13) Part-to-Part Skew (Diff)			50 200			50 200			50 200	ps
$t_{JITTER}$	Random Clock Jitter (RMS)		< 1			< 1			< 1		ps
$V_{PP}$	Input Voltage Swing (Differential Configuration)	250		1000	250		1000	250		1000	mV
$t_r/t_f$	Output Rise/Fall Time (20%–80%)	275		600	275		600	275		600	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7.  $V_{EE}$  can vary +0.5 V / -0.5 V.
8. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
9. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
10. The setup time is the minimum time that  $\overline{EN}$  must be asserted prior to the next transition of IN/ $\overline{IN}$  to prevent an output response greater than  $\pm 75$  mV to that IN/ $\overline{IN}$  transition.
11. The hold time is the minimum time that  $\overline{EN}$  must remain asserted after a negative going IN or a positive going  $\overline{IN}$  to prevent an output response greater than  $\pm 75$  mV to that IN/ $\overline{IN}$  transition.
12. The release time is the minimum time that  $\overline{EN}$  must be deasserted prior to the next IN/ $\overline{IN}$  transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times.
13. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.

## MC10E411



**Figure 4. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC10E411FN	PLCC-28	37 Units / Rail
MC10E411FNG	PLCC-28 (Pb-Free)	37 Units / Rail
MC10E411FNR2	PLCC-28	500 / Tape & Reel
MC10E411FNR2G	PLCC-28 (Pb-Free)	500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

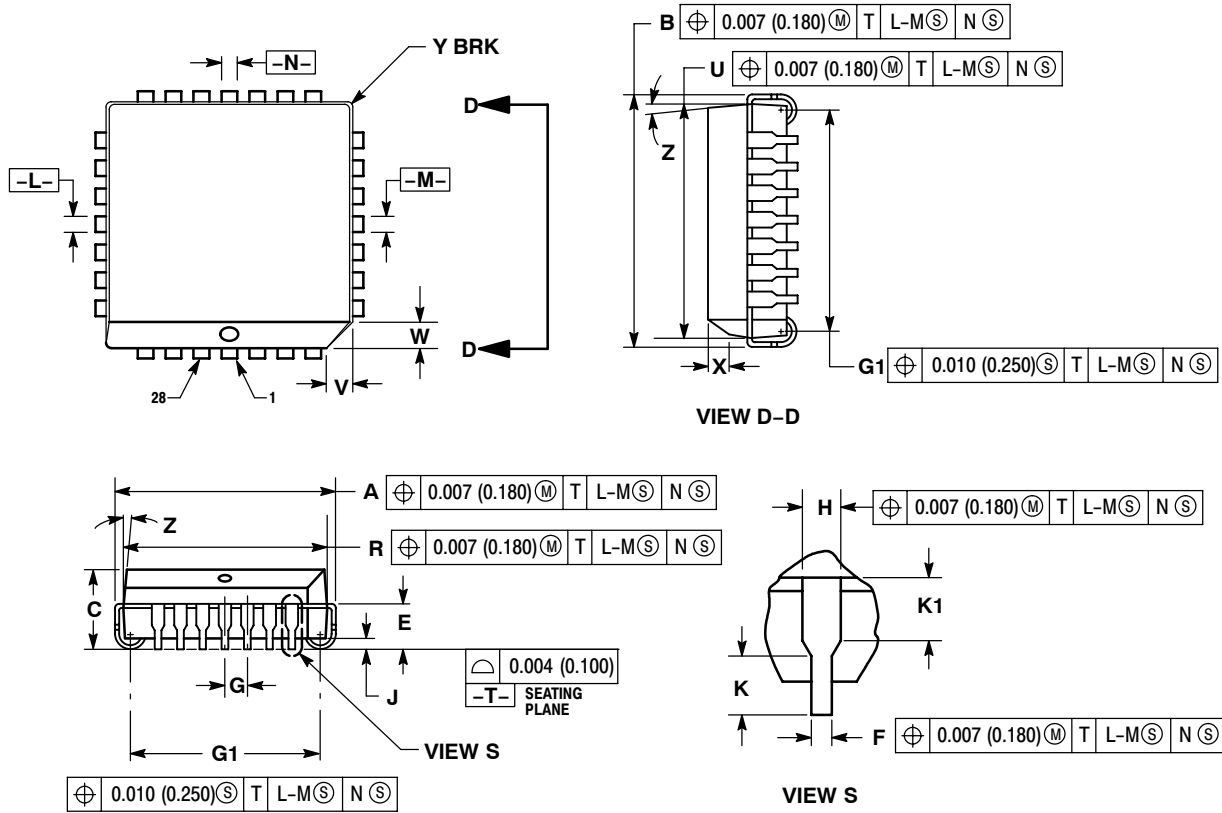
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC10E411

## PACKAGE DIMENSIONS

PLCC-28  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 776-02  
ISSUE E



### NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE BOTTOM MAY BE SMALLER THAN THE PACKAGE TOP BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2° 10°		2° 10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---



# MC10E411

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