阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

Integrated Circuit Systems, Inc.

ICS853310

LOW SKEW, 1-TO-8 DIFFERENTIAL-TO-3.3V LVPECL/ECL FANOUT BUFFER

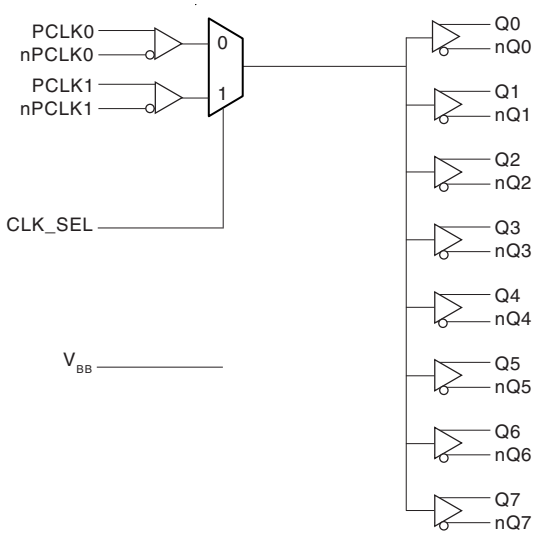
GENERAL DESCRIPTION

The ICS853310 is a low skew, high performance 1-to-8 Differential-to-3.3V LVPECL/ECL Fanout Buffer and a member of the HiPerClockS™family of High Performance Clock Solutions from ICS. The PCLKx, nPCLKx pairs can accept LVPECL, LVDS, CML and SSTL differential input levels. The ICS853310 is characterized to operate from a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS853310 ideal for those clock distribution applications demanding well defined performance and repeatability.

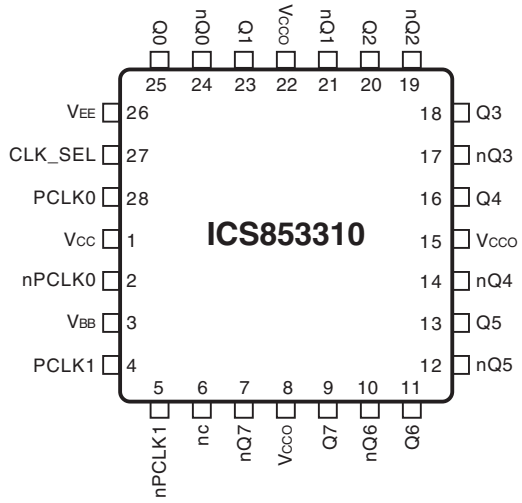
FEATURES

- Eight differential 3.3V LVPECL / ECL outputs
- Two selectable differential LVPECL input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: >2GHz (typical)
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nPCLKx input
- Output skew: 50ps (maximum)
- Part-to-part skew: 200ps (maximum)
- Propagation delay: 900ps (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 3V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3V to -3.8V
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



28-Lead PLCC
11.6mm x 11.4mm x 4.1mm package body
V Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{CC}	Power		Core supply pin.
2	nPCLK0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$.
3	V_{BB}	Output		Bias voltage.
4	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
5	nPCLK1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$.
6	nc	Unused		No connect.
7, 9	nQ7, Q7	Output		Differential output pair. LVPECL interface levels.
8, 15, 22	V_{CCO}	Power		Output supply pins.
10, 11	nQ6, Q6	Output		Differential output pair. LVPECL interface levels.
12, 13	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
14, 16	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
17, 18	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
19, 20	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
21, 23	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
24, 25	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.
26	V_{EE}	Power		Negative supply pin.
27	CLK_SEL	Input	Pulldown	Clock Select input. When HIGH, selects PCLK1, nPCLK1 inputs. When LOW, selects PCLK0, nPCLK0 inputs. LVCMOS / LVTTL interface levels.
28	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-4.6V (LVECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5 V
Inputs, V_I (LVECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
V_{BB} Sink/Source, I_{BB}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Wave Solder, T_{SOL}	265°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 2A. LVPECL POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3V TO 3.8V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.0	3.3	3.8	V
V_{CCO}	Output Supply Voltage		3.0	3.3	3.8	V
I_{EE}	Power Supply Current				70	mA

Table 2B. LVPECL DC Characteristics, V_{CC} = 3.3V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		2.175	2.275	2.38	2.225	2.295	2.37	2.295	2.22	2.365	V
V_{OL}	Output Low Voltage; NOTE 1		1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
V_{IH}	Input High Voltage (Single-Ended)		2.075		2.36	2.075		2.36	2.075			V
V_{IL}	Input Low Voltage (Single-Ended)		1.43		1.765	1.43		1.765	1.43		1.765	V
V_{BB}	Output Voltage Reference; NOTE 2		1.86		1.98	1.86		1.98	1.86		1.98	mV
V_{PP}	Peak-to-Peak Input Voltage		500		1000	500		1000	500		1000	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3		1.8		2.9	1.8		2.9	1.8		2.9	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1 CLK_SEL			150			150			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1, nPCLK0, nPCLK1 CLK_SEL	-150			-150			-150			µA

NOTE 1: Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3V.
Please refer to Parameter Measurement Information, "Output Load AC Test Circuit".
NOTE 2: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 3: V_{CMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1V and greater than or equal to V_{PP}(min).

TABLE 2C. LVECL POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.3V ± 0.3V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{EE}	Supply Voltage		-3.0	-3.3	-3.8	V
I_{EE}	Power Supply Current				70	mA

Table 2D. ECL DC Characteristics, V_{CC} = 0V; V_{EE} = -3.3V ± 0.3V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage		-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.005	-1.08	-0.935	V
V_{OL}	Output Low Voltage		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{IH}	Input High Voltage (Single-Ended)		-1.225		-0.94	-1.225		-0.94	-1.225			V
V_{IL}	Input Low Voltage (Single-Ended)		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{BB}	Output Voltage Reference; NOTE 1		-1.44		-1.32	-1.44		-1.32	-1.44		-1.32	mV
V_{PP}	Peak-to-Peak Input Voltage		500		1000	500		1000	500		1000	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2		1.5		-0.4	1.5		-0.4	1.5		-0.4	V
I_{IH}	Input High Current	PCLK0, PCLK1, nPCLK0, nPCLK1 CLK_SEL			150			150			150	µA
IIL	Input Low Current	PCLK0, PCLK1, nPCLK0, nPCLK1 CLK_SEL	-150			-150			-150			µA

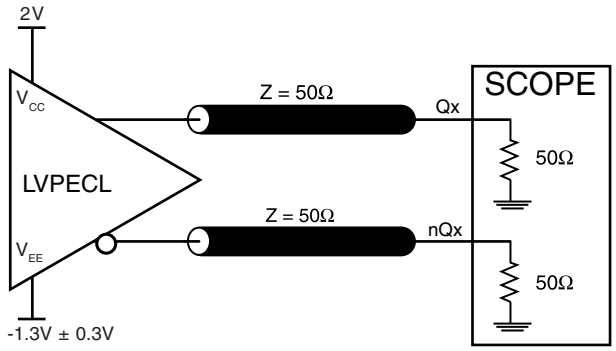
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: V_{CMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1V and greater than or equal to V_{PP}(min).

TABLE 3. AC CHARACTERISTICS, V_{CC} = 3.3V; V_{EE} = 0V OR V_{CC} = 0V; V_{EE} = -3.3V

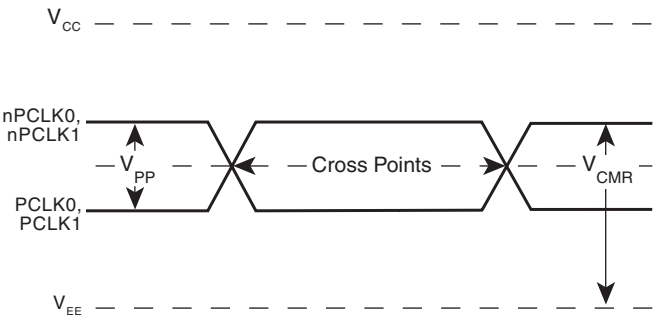
Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency			>2			>2			>2		GHz
t_{PD}	Propagation Delay; NOTE 1		700		900	750		950	775		975	ps
*t*sk(o)	Output Skew; NOTE 2, 4				75			50			50	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				250			200			200	ps
t_R/t_F	Output Rise/Fall Time	20% to 80%	100		400	100		400	100		400	ps

V_{EE} can very ± 0.3V.
All parameters measured at $f \leq$ 1.2GHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

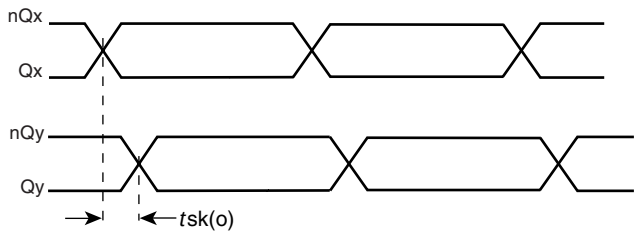
PARAMETER MEASUREMENT INFORMATION



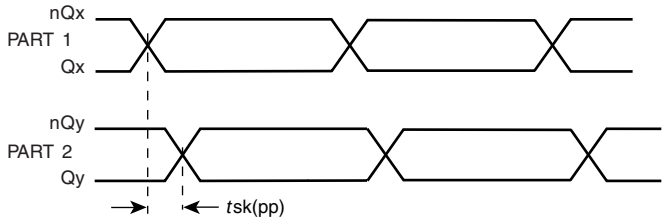
OUTPUT LOAD AC TEST CIRCUIT



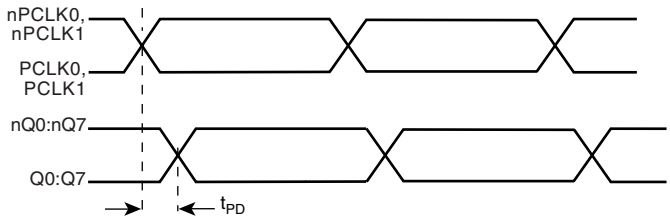
DIFFERENTIAL INPUT LEVEL



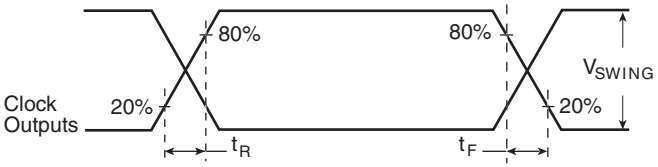
OUTPUT SKEW



PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVCMOS LEVELS

Figure 1A shows an example of the differential input that can be wired to accept single ended LVCMOS levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

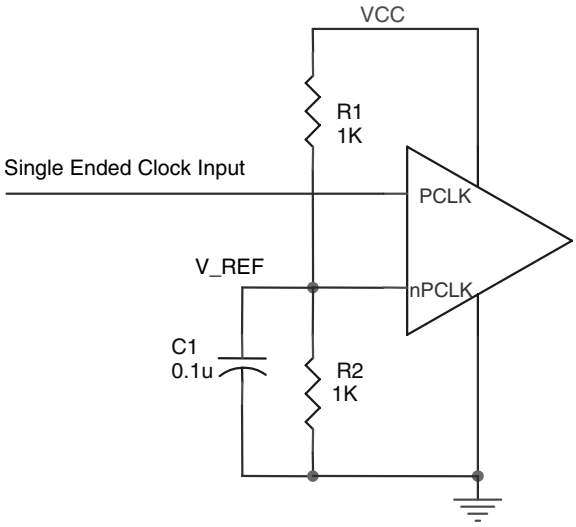


FIGURE 1A. SINGLE ENDED LVCMOS SIGNAL DRIVING DIFFERENTIAL INPUT

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVPECL LEVELS

Figure 1B shows an example of the differential input that can be wired to accept single ended LVPECL levels. The reference voltage level V_{BB} generated from the device is connected to the negative input.

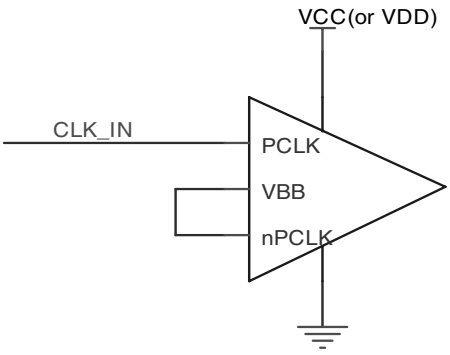


FIGURE 1B. SINGLE ENDED LVPECL SIGNAL DRIVING DIFFERENTIAL INPUT

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

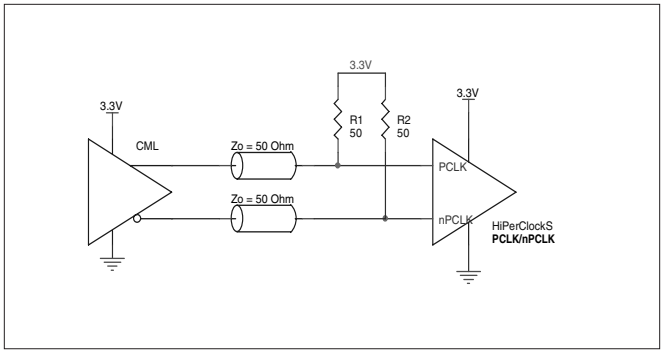


FIGURE 2A. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER

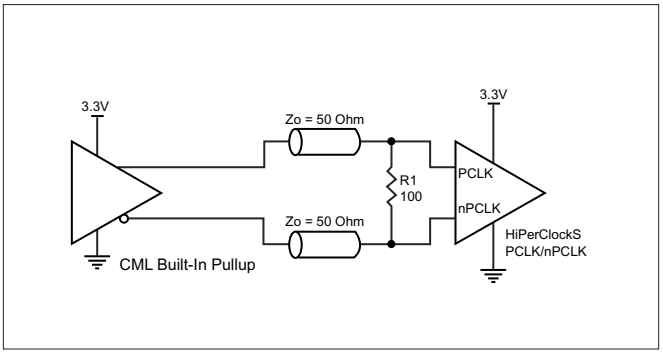


FIGURE 2B. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER

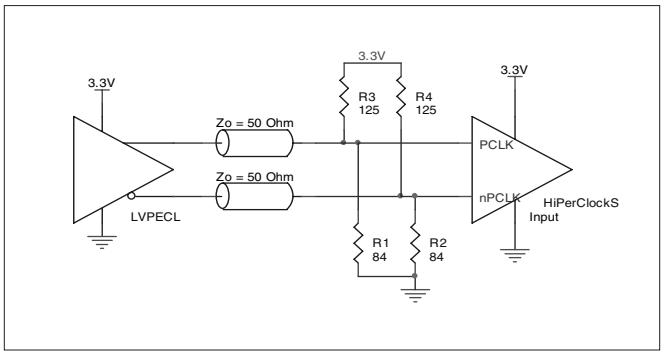


FIGURE 2C. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

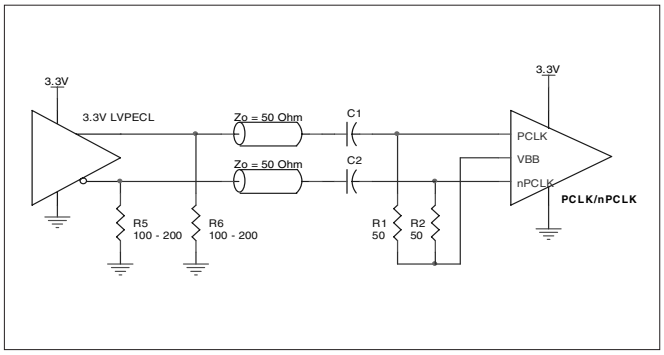


FIGURE 2D. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

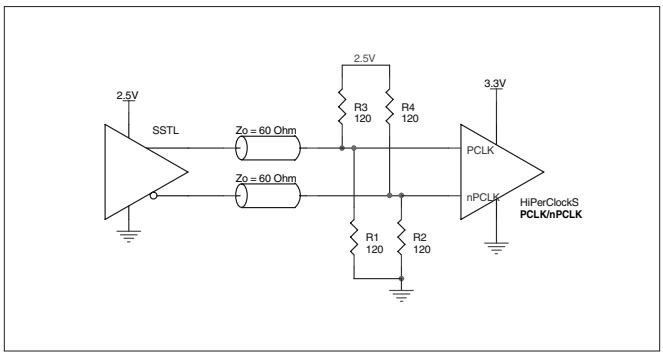


FIGURE 2E. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN SSTL DRIVER

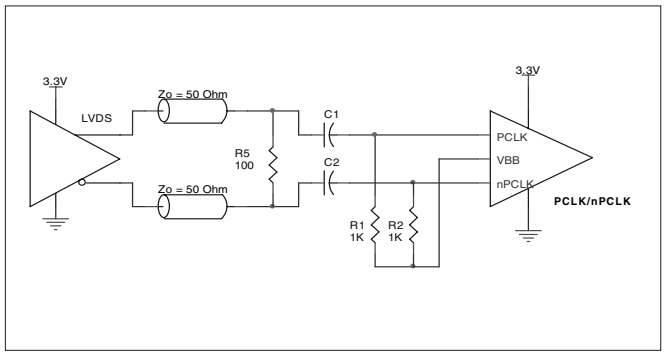


FIGURE 2F. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

PCLK/nPCLK INPUT:
For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

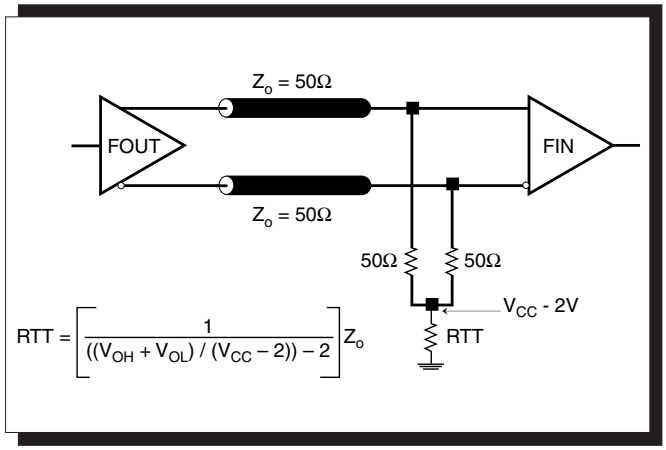


FIGURE 3A. LVPECL OUTPUT TERMINATION

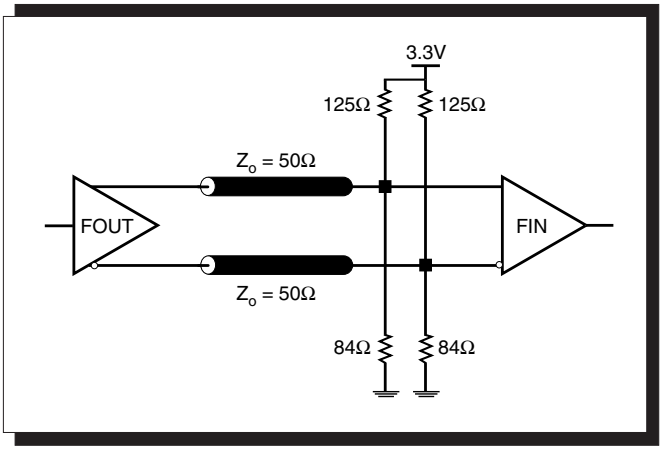


FIGURE 3B. LVPECL OUTPUT TERMINATION

SCHEMATIC EXAMPLE

Figure 4A shows a schematic example of the ICS853310. In this example, the PCLK0/nPCLK0 input is selected. The decoupling capacitors should be physically located near the power pin. For ICS853310, the unused outputs can be left floating.

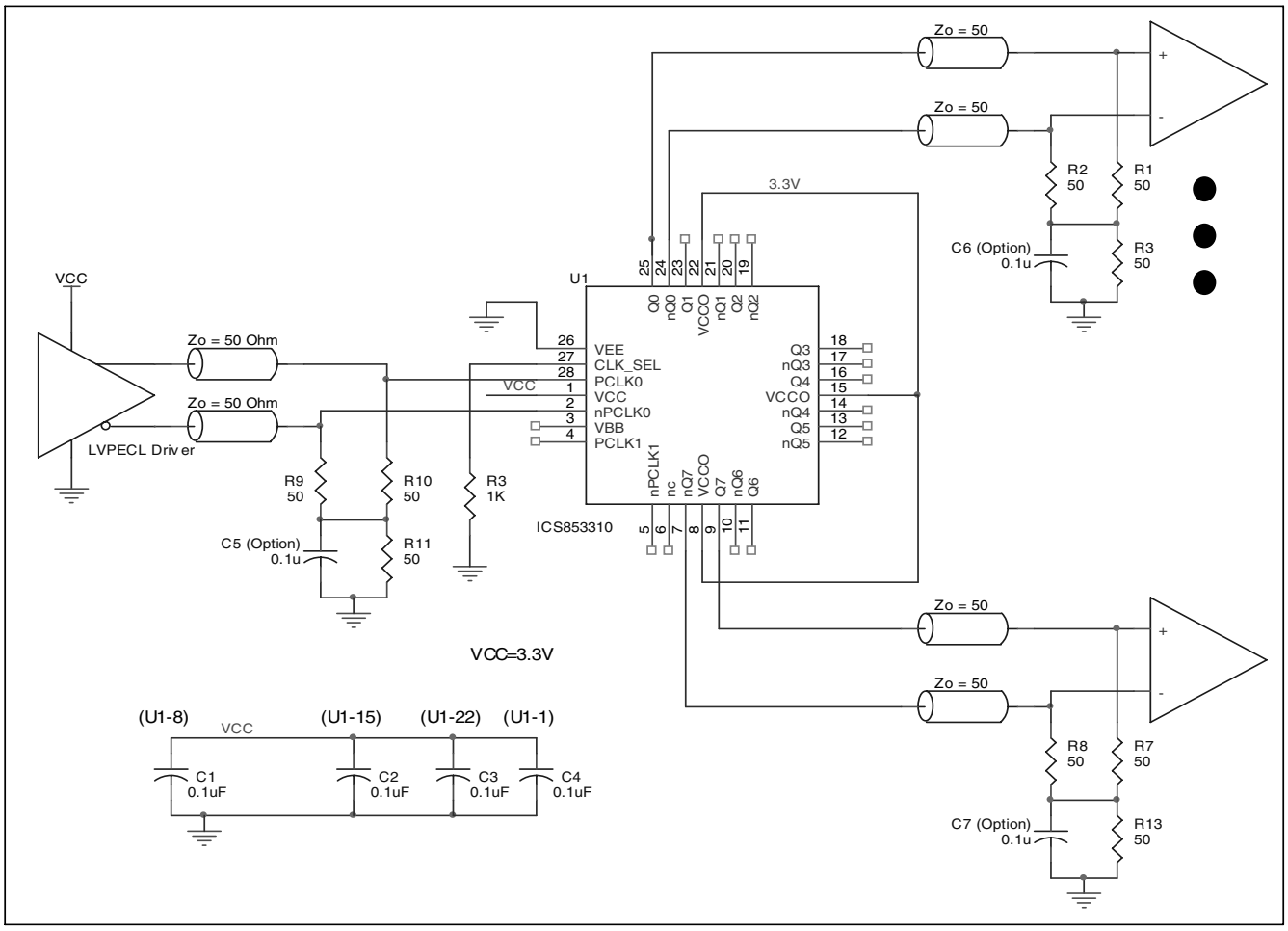


FIGURE 4A. ICS853310 LVPECL CLOCK OUTPUT BUFFER SCHEMATIC EXAMPLE

POWER, GROUND AND BYPASS CAPACITOR

This section provides a layout guide related to power, ground and placement of bypass capacitors for a high-speed digital IC. This layout guide is a general recommendation. The actual board design will depend on the component types being used, the board density and cost constraints. This description assumes that the board has clean power and ground planes. The goal is to minimize the ESR between the clean power/ground plane and the IC power/ground pin.

A low ESR bypass capacitor should be used on each power pin. The value of bypass capacitors ranges from 0.01uF to 0.1uF. The bypass capacitors should be located as close to the power pin as possible. It is preferable to locate the bypass capacitor on the same side as the IC. *Figure 4B* shows suggested capacitor placement. Placing the bypass capacitor on the same side as the IC allows the capacitor to have direct contact with the IC power pin. This can avoid any vias between the bypass capacitor and the IC power pins.

The vias should be placed at the Power/Ground pads. There should be a minimum of one via per pin. Increasing the number of vias from the Power/Ground pads to Power/Ground planes can improve the conductivity.

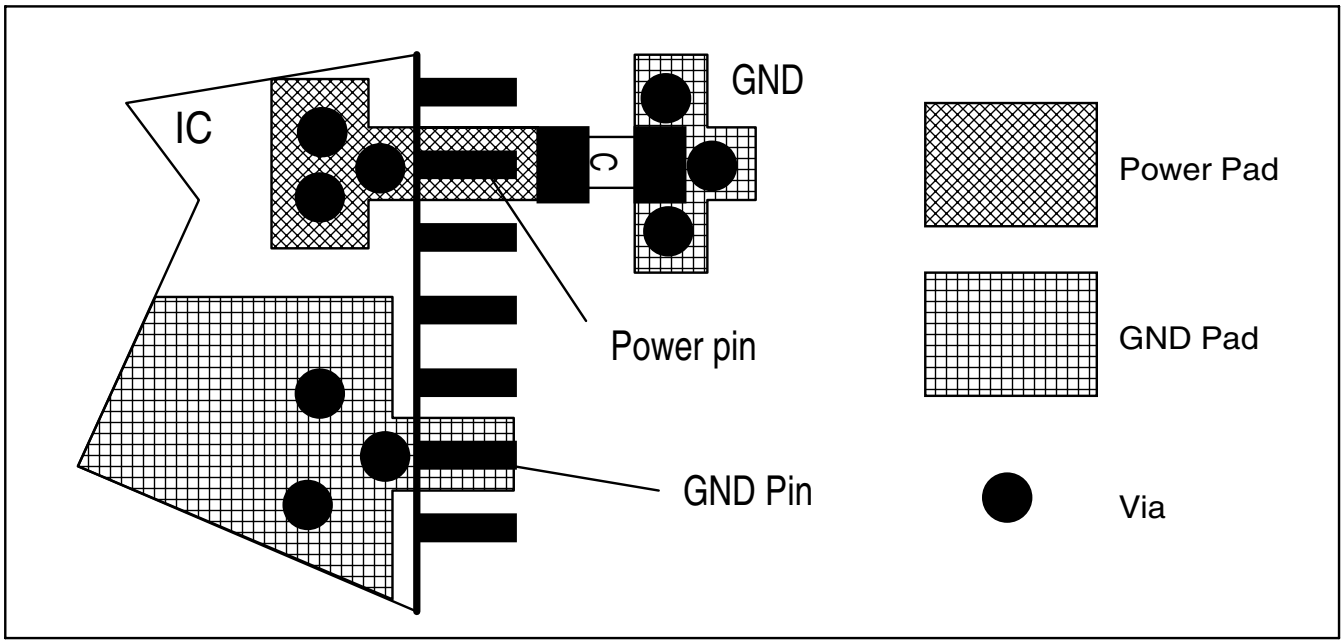


FIGURE 4B. RECOMMENDED LAYOUT OF BYPASS CAPACITOR PLACEMENT

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853310.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS853310 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.8V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.8V * 70mA = **266mW**
- Power $(outputs)_{MAX}$ = **30.94mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 30.94mW = **247.5mW**

Total Power$_{_MAX}$ (3.8V, with all outputs switching) = 266mW + 247.5mW = **513.5mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 31.1°C/W per Table 4 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.514W * 31.1°C/W = 101°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 4. THERMAL RESISTANCE θ_{JA} FOR 28-PIN PLCC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	37.8°C/W	31.1°C/W	28.3°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 5.

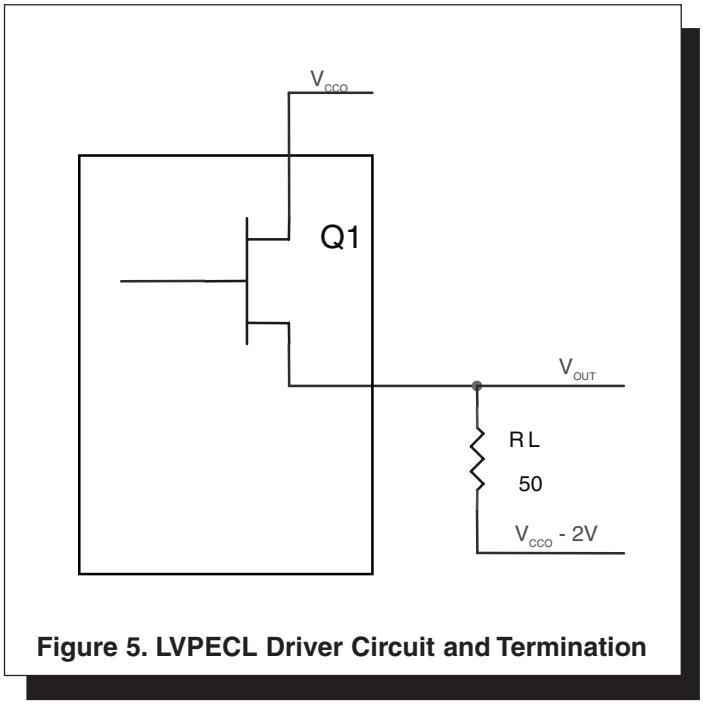


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} – 0.935V$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.935V$

- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} – 1.67V$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.67V$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50\Omega] * 1.67V = 11.02mW$

Total Power Dissipation per output pair = Pd_H + Pd_L = 30.94mW

RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE FOR 28 LEAD PLCC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	37.8°C/W	31.1°C/W	28.3°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS853310 is: 462

Pin compatible with MC100LVE310

PACKAGE OUTLINE - V SUFFIX FOR 28 LEAD PLCC

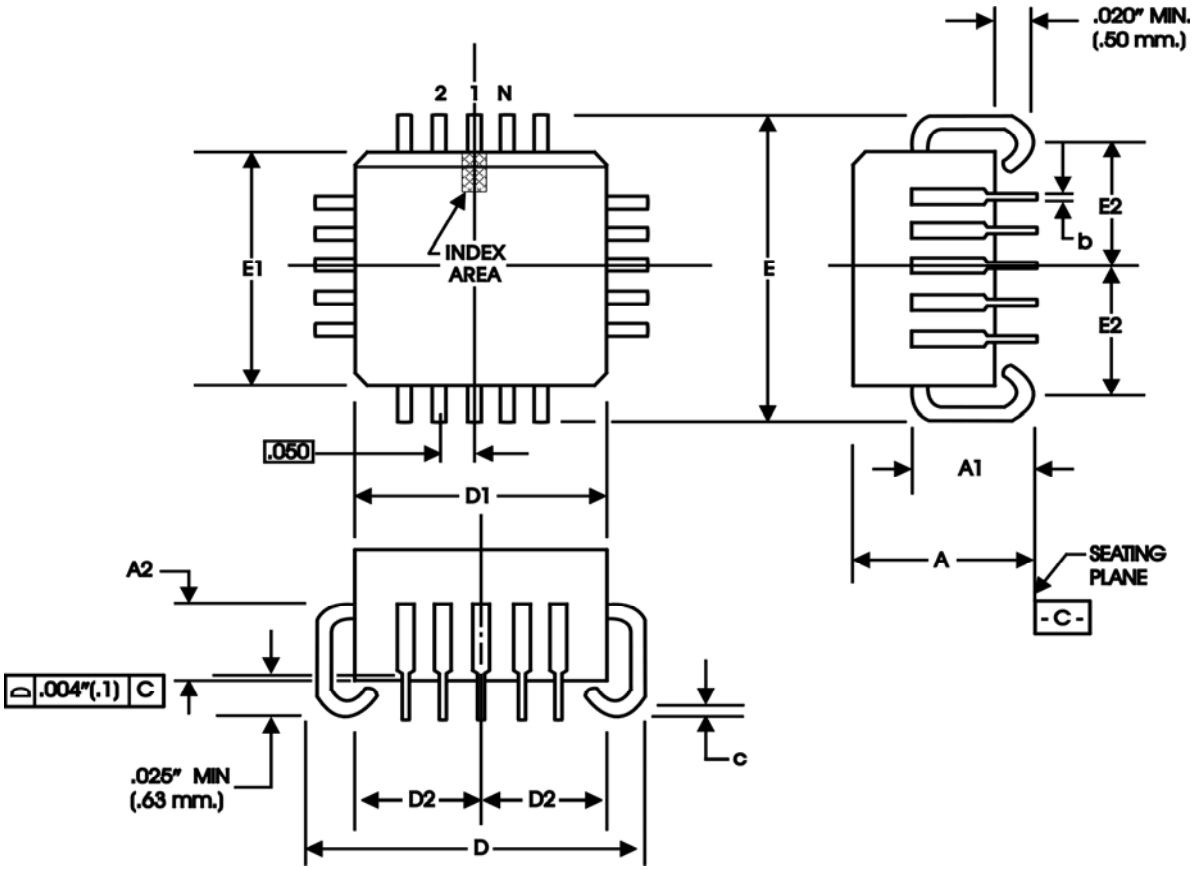


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	28	
A	4.19	4.57
A1	2.29	3.05
A2	1.57	2.11
b	0.33	0.53
c	0.19	0.32
D	12.32	12.57
D1	11.43	11.58
D2	4.85	5.56
E	12.32	12.57
E1	11.43	11.58
E2	4.85	5.56

Reference Document: JEDEC Publication 95, MS-018

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853310AV	ICS853310AV	28 Lead PLCC	Tube	-40°C to 85°C
853310AVT	ICS853310AV	28 Lead PLCC on Tape and Reel	500 Tape & Reel	-40°C to 85°C
853310AVLF	ICS853310AVL	28 Lead "Lead-Free" PLCC	Tube	-40°C to 85°C
853310AVLFT	ICS853310AVL	28 Lead "Lead-Free" PLCC	500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		1	Add Lead-Free bullet. Corrected Pin Assignment pin number spacing.	9/14/05
		8	Added *Recommendations for Unused Input and Output Pins.*	
	T7	15	Ordering Information Table - added Lead-Free Part Number.	
A	T7	15	Ordering Information Table - added Lead-Free marking.	11/22/05