

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

Features

- High-speed, low-noise non-inverting 1-5 buffer
- Switching speed up to 140 MHz
- Supports up to two SODIMMs
- Low skew (<250ps) between any two output clocks
- I²C Serial Configuration interface
- Multiple V_{DD}, V_{SS} pins for noise reduction
- 3.3V power supply voltage
- Packaging (Pb-free & Green available):
 - 16-pin TSSOP(L)
 - 16-pin QSOP(Q)

Description

The PI6C185-01 is a high-speed low-noise 1-5 non-inverting buffer designed for SDRAM clock buffer applications.

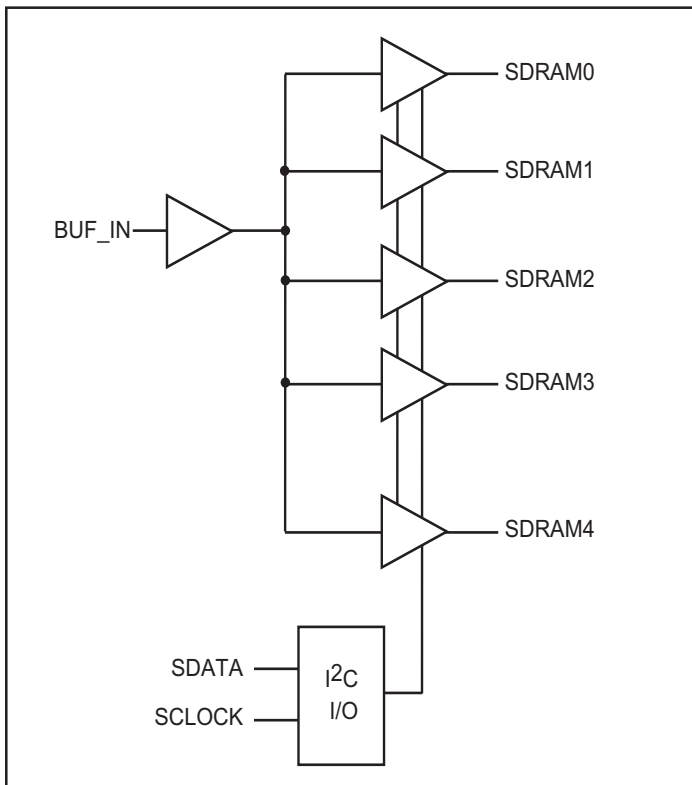
This buffer is intended to be used with the PI6C10X clock generator for Intel Architecture-based Mobile systems.

At power-up, all SDRAM outputs are enabled and active. The I²C Serial control may be used to individually activate/deactivate any of the 5 output drivers.

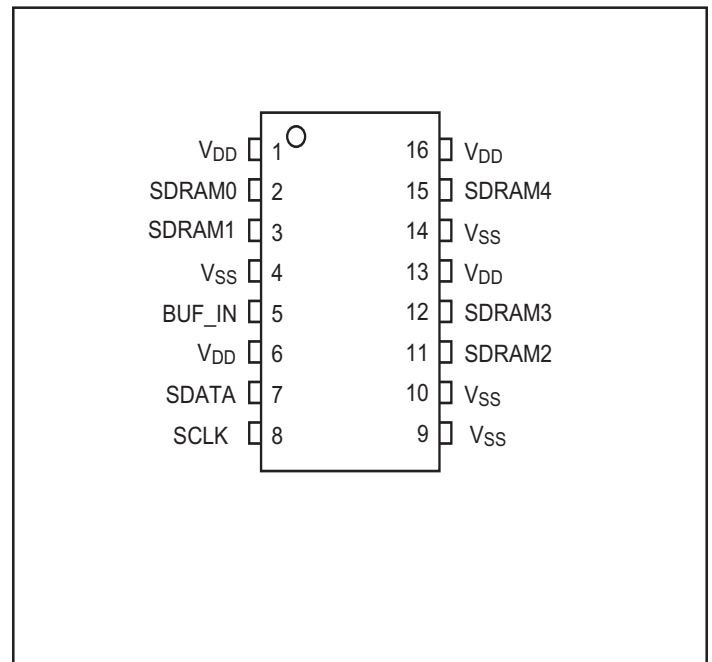
Note:

Purchase of I²C components from Pericom conveys a license to use them in an I²C system as defined by Philips®.

Block Diagram



Pin Configuration



Pin Description

Pin	Signal	Type	Qty	Description
2,3,11,12,15	SDRAM [0.4]	I	5	Buffered Clock Outputs
5	BUF_IN	I	1	Clock Buffer Input
7	SDATA	I/O	1	Serial Data for I ² C interface, internal pull-up
8	SCLK	I	1	Serial Clock for I ² C interface, internal pull-up
1,6,13,16	V _{DD}	Power	4	3.3V Power Supply
4,9,10,14	V _{SS}	Ground	4	Ground

I²C Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	0

Serial Configuration Map

Byte0: SDRAM Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	Description
Bit 7	12	SDRAM3 (Active/Inactive)
Bit 6	11	SDRAM2 (Active/Inactive)
Bit 5	-	NC (Initialize to 0)
Bit 4	-	NC (Initialize to 0)
Bit 3	-	NC (Initialize to 0)
Bit 2	-	NC (Initialize to 0)
Bit 1	3	SDRAM1 (Active/Inactive)
Bit 0	2	SDRAM0 (Active/Inactive)

Byte1: SDRAM Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin#	Description
Bit 7	-	NC (Initialize to 0)
Bit 6	-	NC (Initialize to 0)
Bit 5	-	NC (Initialize to 0)
Bit 4	-	NC (Initialize to 0)
Bit 3	-	NC (Initialize to 0)
Bit 2	-	NC (Initialize to 0)
Bit 1	-	NC (Initialize to 0)
Bit 0	15	SDRAM4 (Active/Inactive)

Note:

Inactive means outputs are held LOW and are disabled from switching

2-Wire I²C Control

The I²C interface permits individual enable/disable of each clock output and test mode enable.

The PI6C185-01 is a slave receiver device. It can not be read back. Sub-addressing is not supported. All preceding bytes must be sent in order to change one of the control bytes.

Every bite put on the SDATA line must be 8-bits long (MSB first), followed by an acknowledge bit generated by the receiving device.

During normal data transfers SDATA changes only when SCLK is LOW. Exceptions: A HIGH-to-LOW transition on SDATA while SCLK is HIGH indicates a “start” condition. A LOW-to-HIGH transition on SDATA while SCLK is HIGH is a “stop” condition and indicates the end of a data transfer cycle.

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always a 7-bit address byte followed by a read/write bit. (HIGH = read from addressed device, LOW = write to addressed device). If the device’s own address is detected, PI6C185-01 generates an acknowledge by pulling SDATA line LOW during ninth clock pulse, then accepts the following data bytes until another start or stop condition is detected.

Following acknowledgement of the address byte (0D2H), two more bytes must be sent:

1. “Command Code” byte, and
2. “Byte Count” byte.

Although the data bits on these two bytes are “don’t care,” they must be sent and acknowledged.

Maximum Ratings

(Above which the useful life may be impaired.
For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
3.3V Supply Voltage to Ground Potential	-0.5V to +4.6V
DC Input Voltage	-0.5V to +4.6V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Supply Current (V_{DD} = +3.465V, C_{LOAD} = Max.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I _{DD}	Supply Current	BUF_IN = 0 MHz			3	
I _{DD}	Supply Current	BUF_IN = 66.66 MHz		70		
I _{DD}	Supply Current	BUF_IN = 100.0 MHz		120		
I _{DD}	Supply Current	BUF_IN = 133.3 MHz		200		mA

DC Operating Specifications ($V_{DD} = +3.3V \pm 5\%$, $T_A = 0^\circ C - 70^\circ C$)

Symbol	Parameter	Condition	Min.	Max.	Units
Input Voltage					
V_{IH}	Input High Voltage	V_{DD}	2.0	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{SS} - 0.3$	0.8	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{DD}$	-5	+5	μA
$V_{DD} = 3.3V \pm 5\%$					
V_{OH}	Output High Voltage	$I_{OH} = -1mA$	2.4		V
V_{OL}	Output Low Voltage	$I_{OL} = 1mA$		0.4	
C_{IN}	Input Pin Capacitance			5	pF
C_{OUT}	Output pins Capacitance			6	
L_{PIN}	Pin Inductance			7	nH
T_A	Ambient Temperature	No Airflow	0	70	$^\circ C$

SDRAM Clock Buffer Operating Specification

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	$V_{OUT} = 2.0V$	-54			mA
I_{OHMAX}	Pull-up current	$V_{OUT} = 3.135V$			-46	
I_{OLMIN}	Pull-down current	$V_{OUT} = 1.0V$	54			
I_{OLMAX}	Pull-down current	$V_{OUT} = 0.4V$			53	
$t_{RHSDRAM}$	Output rise edge rate SDRAM only	$3.3V \pm 5\%$ @0.4V-2.4V	1.5		4	V/ns
$t_{FHSDRAM}$	Output fall edge rate SDRAM only	$3.3V \pm 5\%$ @2.4V-0.4V	1.5		4	

AC Timing

Symbol	Parameter	66 MHz		100 MHz		133 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{DSKP}	SDRAMCLK period	15.0	15.5	10.0	10.5	7.5	8.0	ns
T_{SDKH}	SDRAMCLK high time	5.6		3.3		2.2		ns
T_{SDKL}	SDRAMCLK low time	5.3		3.1		2.0		ns
T_{SDRISE}	SDRAMCLK rise time	1.5	4.0	1.5	4.0	1.4	4.0	V/ns
T_{SDFALL}	SDRAMCLK fall time	1.5	4.0	1.5	4.0	1.4	4.0	V/ns
t_{PLH}	SDRAM Buffer LH prop delay	1.0	5.5	1.0	5.0	1.0	5.0	ns
t_{PHL}	SDRAM Buffer HL prop delay	1.0	5.5	1.0	5.0	1.0	5.0	ns
DutyCycle	Measured at 1.5V	45	55	45	55	45	55	%
t_{SDSKW}	SDRAM Output to Output Skew		250		250		250	ps

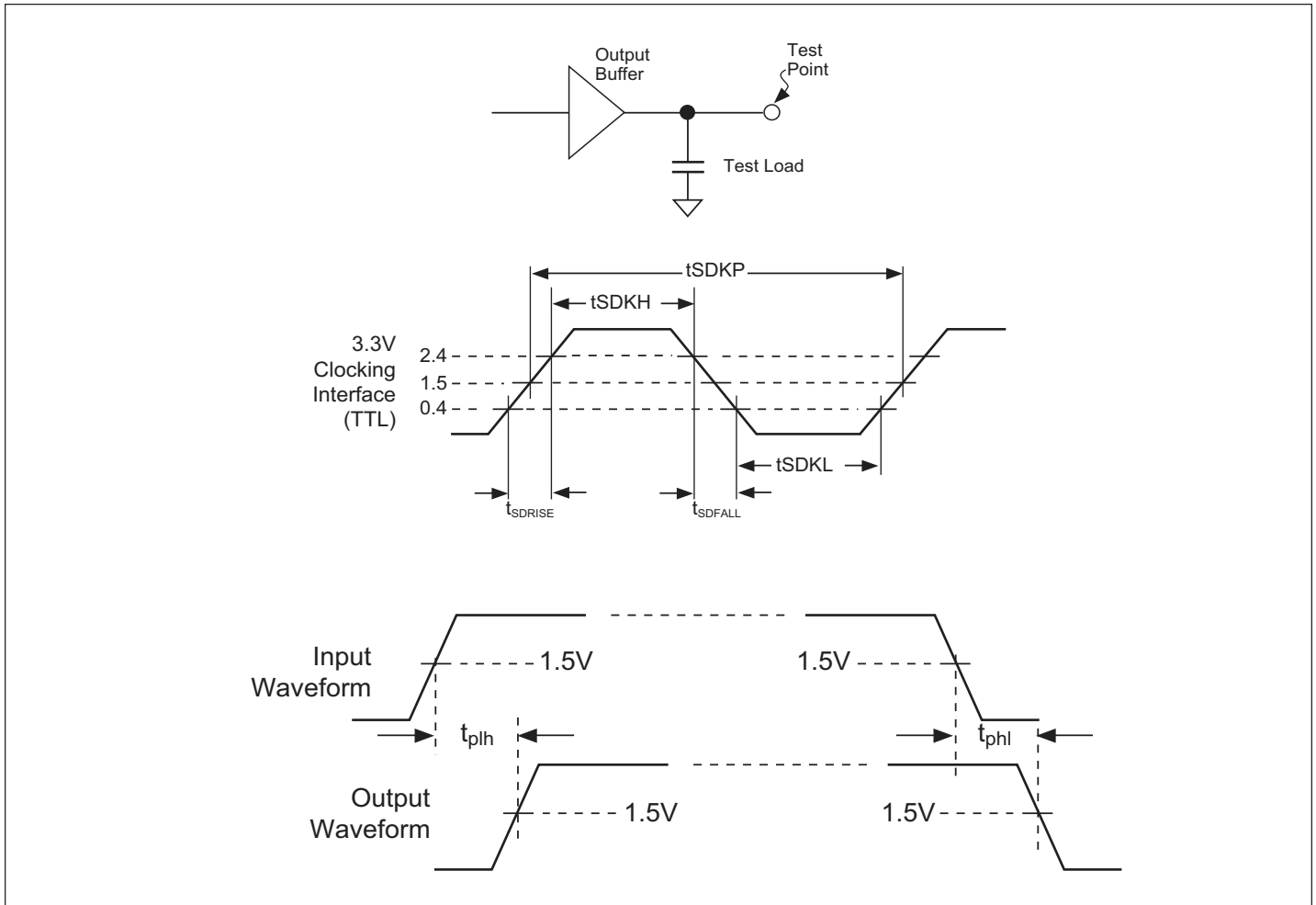


Figure 1. Clock Waveforms

Minimum and Maximum Expected Capacitive Loads

Clock	Min Load	Max Load	Units	Notes
SDRAM	20	30	pF	SDRAM DIMM Specification

Notes:

1. Maximum rise/fall times are guaranteed at maximum specified load.
2. Minimum rise/fall times are guaranteed at minimum specified load.
3. Rise/fall times are specified with pure capacitive load as shown.
Testing is done with an additional 500Ω resistor in parallel.

Design Guidelines to Reduce EMI

1. Place R_s series resistors and CI capacitors as close as possible to the respective clock pins. Typical value for CI is 10 pF. R_s Series resistor value can be increased to reduce EMI provided that the rise and fall time are still within the specified values.
2. Minimize the number of “vias” of the clock traces.
3. Route clock traces over a continuous ground plane or over a continuous power plane. Avoid routing clock traces from plane to plane (refer to rule #2).
4. Position clock signals away from signals that go to any cables or any external connectors.

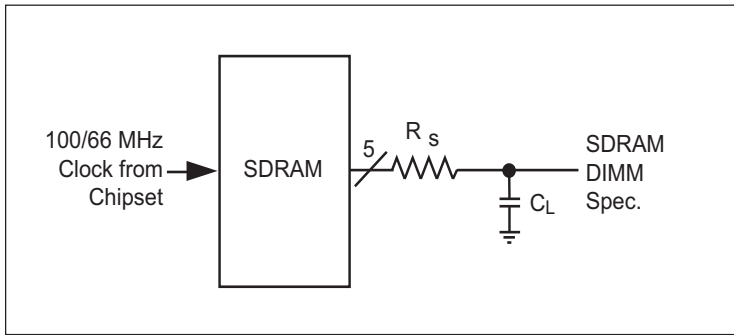
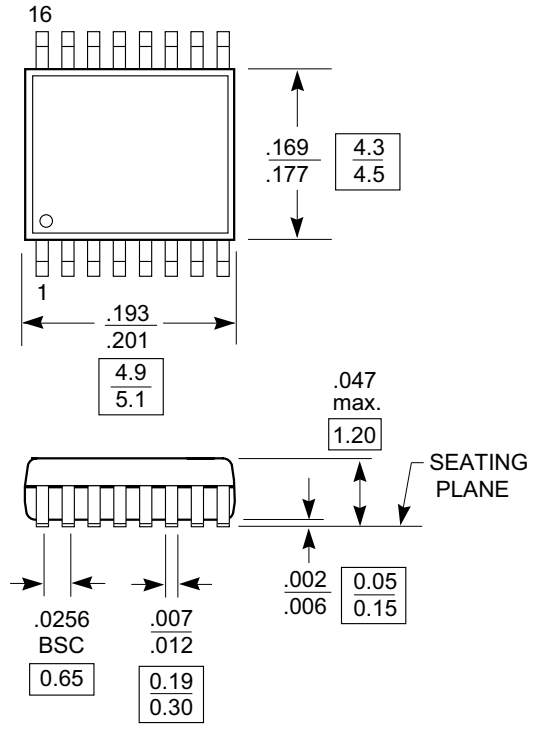
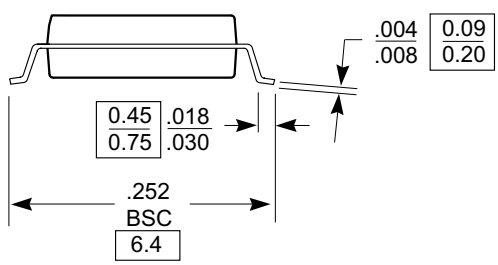



Figure 2. Design Guidelines

Packaging Mechanical: 16-Pin TSSOP (L)

DOCUMENT CONTROL NO. PD - 1310
REVISION: E DATE: 03/09/05







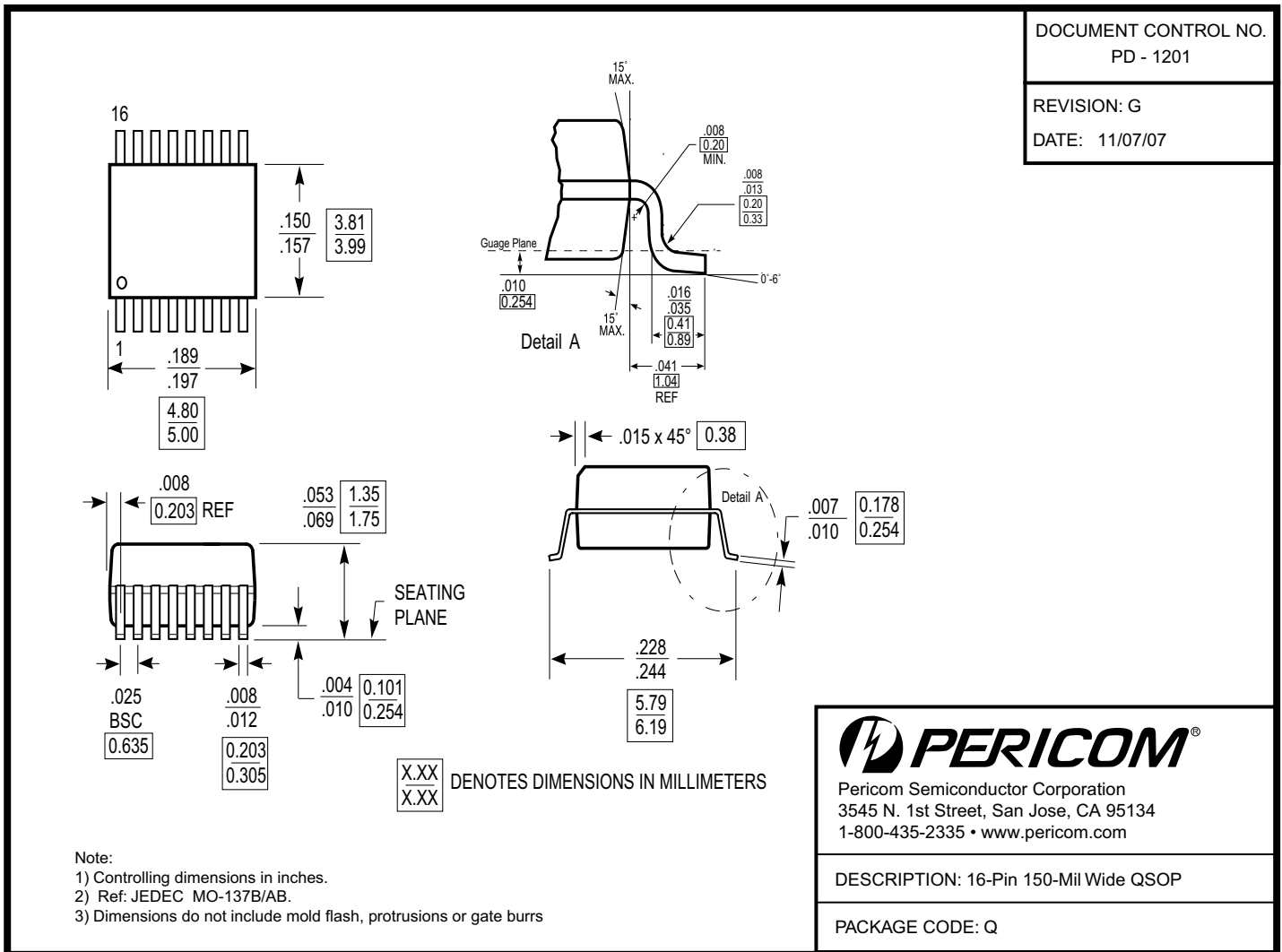
DESCRIPTION: 16-Pin, 173-Mil Wide, TSSOP

PACKAGE CODE: L

Note:

1. Package Outline Exclusive of Mold Flash and Metal Burr
2. Controlling dimensions in millimeters
3. Ref: JEDEC MO-153F/AB

Packaging Mechanical: 16-Pin QSOP (Q)



Ordering Information

Ordering Code	Packaging Code	Package Description	Operating Temperature
PI6C185-01L	L	16-Pin TSSOP	Commercial
PI6C185-01LE	L	Pb-free & Green, 16-Pin TSSOP	Commercial
PI6C185-01QE	Q	Pb-free & Green, 16-Pin QSOP	Commercial
PI6C185-01QIE	Q	Pb-free & Green, 16-Pin QSOP	Industrial

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/