

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

312.5 MHz LVPECL Clock Generator

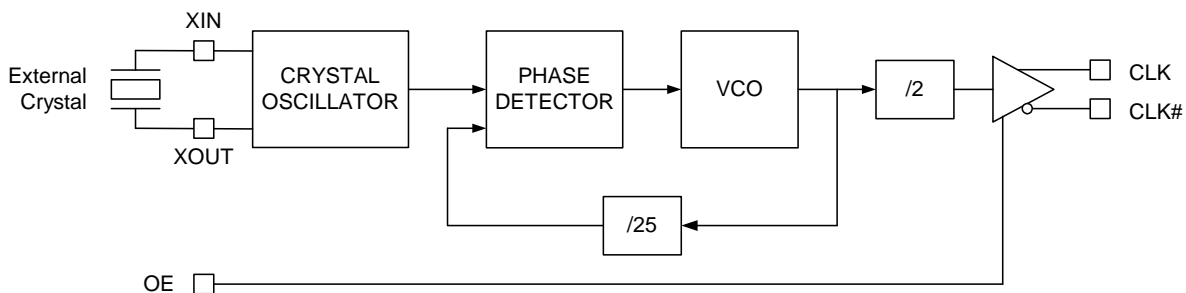
Features

- One LVPECL output pair
- Output frequency: 312.5 MHz
- External crystal frequency: 25 MHz
- Low RMS phase jitter at 312.5 MHz, using 25 MHz crystal (1.875 MHz to 20 MHz): 0.3 ps (typical)
- Pb-free 8-Pin TSSOP package
- Supply voltage: 3.3 V or 2.5 V
- Commercial and industrial temperature ranges

Functional Description

The CY2XP31 is a PLL (Phase Locked Loop) based high performance clock generator. It is optimized to generate 10 Gb Ethernet, SONET, and other high performance clock frequencies. It also produces an output frequency that is 12.5 times the crystal frequency. It uses Cypress's low noise VCO technology to achieve less than 1 ps typical RMS phase jitter, which meets both 10 Gb Ethernet and SONET jitter requirements. The CY2XP31 has a crystal oscillator interface input and one LVPECL output pair.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram – 8-Pin TSSOP



Table 1. Pin Definition – 8-Pin TSSOP

Pin Number	Pin Name	I/O Type	Description
1, 8	VDD	Power	3.3 V or 2.5 V power supply. All supply current flows through pin 1
2	VSS	Power	Ground
3, 4	XOUT, XIN	XTAL Output and Input	Parallel resonant crystal interface
5	OE	CMOS Input	Output enable. When HIGH, the output is enabled. When LOW, the output is high impedance
6,7	CLK#, CLK	LVPECL Output	Differential clock output

Frequency Table

Inputs		Output Frequency (MHz)
Crystal Frequency (MHz)	PLL Multiplier Value	
25	12.5	312.5

Absolute Maximum Conditions

Parameter	Description	Conditions	Min	Max	Unit
V _{DD}	Supply Voltage		-0.5	4.4	V
V _{IN} ^[1]	Input Voltage, DC	Relative to V _{SS}	-0.5	V _{DD} + 0.5	V
T _S	Temperature, Storage	Non operating	-65	150	°C
T _J	Temperature, Junction		-	135	°C
ESD _{HBM}	ESD Protection, Human Body Model	JEDEC STD 22-A114-B	2000	-	V
UL-94	Flammability Rating	At 1/8 in.	V-0		
Θ _{JA} ^[2]	Thermal Resistance, Junction to Ambient	0 m/s airflow	100		°C/W
		1 m/s airflow	91		
		2.5 m/s airflow	87		

Operating Conditions

Parameter	Description	Min	Max	Unit
V _{DD}	3.3 V Supply Voltage	3.135	3.465	V
	2.5 V Supply Voltage	2.375	2.625	V
T _A	Ambient Temperature, Commercial	0	70	°C
	Ambient Temperature, Industrial	-40	85	°C
T _{PU}	Power-up time for all V _{DD} to reach minimum specified voltage (ensure power ramps is monotonic)	0.05	500	ms

Notes

1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I _{DD}	Operating Supply Current with Output Unterminated	V _{DD} = 3.465 V, OE = V _{DD} , output unterminated	–	–	125	mA
		V _{DD} = 2.625 V, OE = V _{DD} , output unterminated	–	–	120	mA
I _{DDT}	Operating Supply Current with Output Terminated	V _{DD} = 3.465 V, OE = V _{DD} , output terminated	–	–	150	mA
		V _{DD} = 2.625 V, OE = V _{DD} , output terminated	–	–	145	mA
V _{OH}	LVPECL Output High Voltage	V _{DD} = 3.3 V or 2.5 V, R _{TERM} = 50Ω to V _{DD} – 2.0 V	V _{DD} – 1.15	–	V _{DD} – 0.75	V
V _{OL}	LVPECL Output Low Voltage	V _{DD} = 3.3 V or 2.5 V, R _{TERM} = 50Ω to V _{DD} – 2.0 V	V _{DD} – 2.0	–	V _{DD} – 1.625	V
V _{OD1}	LVPECL Peak-to-Peak Output Voltage Swing	V _{DD} = 3.3 V or 2.5 V, R _{TERM} = 50Ω to V _{DD} – 2.0 V	600	–	1000	mV
V _{OD2}	LVPECL Output Voltage Swing (V _{OH} – V _{OL})	V _{DD} = 2.5 V, R _{TERM} = 50Ω to V _{DD} – 1.5 V	500	–	1000	mV
V _{OCM}	LVPECL Output Common Mode Voltage (V _{OH} + V _{OL})/2	V _{DD} = 2.5 V, R _{TERM} = 50Ω to V _{DD} – 1.5 V	1.2	–	–	V
I _{OZ}	LVPECL Output Leakage Current	Output off, OE = V _{SS}	–35	–	35	μA
V _{IH}	Input High Voltage, OE Pin		0.7*V _{DD}	–	V _{DD} +0.3	V
V _{IL}	Input Low Voltage, OE Pin		–0.3	–	0.3*V _{DD}	V
I _{IH}	Input High Current, OE Pin	OE = V _{DD}	–	–	115	μA
I _{IL}	Input Low Current, OE Pin	OE = V _{SS}	–50	–	–	μA
C _{IN} ^[5]	Input Capacitance, OE Pin		–	15	–	pF
C _{INX} ^[5]	Pin Capacitance, XIN & XOUT		–	4.5	–	pF

AC Electrical Characteristics^[5]

Parameter	Description	Conditions	Min	Typ	Max	Unit
F _{OUT}	Output Frequency		–	312.5	–	MHz
T _R , T _F ^[3]	Output Rise or Fall Time	20% to 80% of full output swing	–	0.5	1.0	ns
T _{Jitter(φ)} ^[6]	RMS Phase Jitter (Random)	312.5 MHz, (1.875 to 20 MHz)	–	0.3	–	ps
T _{DC} ^[7]	Output Duty Cycle	Measured at zero crossing point	45	–	55	%
T _{OHZ}	Output Disable Time	Time from falling edge on OE to stopped outputs (Asynchronous)	–	–	100	ns
T _{OE}	Output Enable Time	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	–	100	ns
T _{LOCK}	Startup Time	Time for CLK to reach valid frequency measured from the time V _{DD} = V _{DD} (min.)	–	–	5	ms

Recommended Crystal Specifications^[4]

Parameter	Description	Min	Max	Unit
Mode	Mode of Oscillation	Fundamental		
F	Frequency	25	25	MHz
ESR	Equivalent Series Resistance	–	50	Ω
C _S	Shunt Capacitance	–	7	pF

Parameter Measurements

Figure 2. 3.3 V Output Load AC Test Circuit

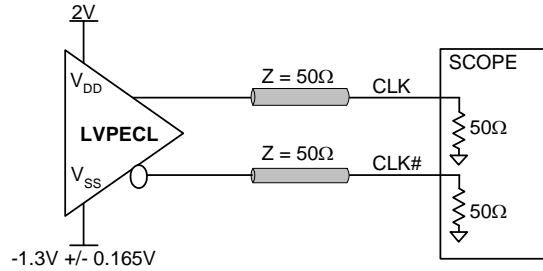


Figure 3. 2.5 V Output Load AC Test Circuit

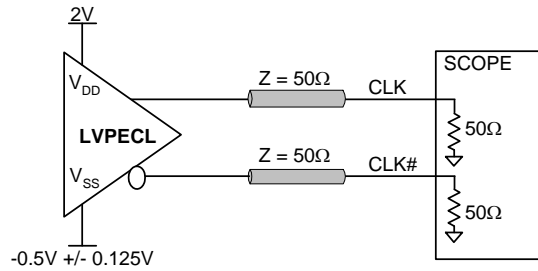


Figure 4. Output DC Parameters

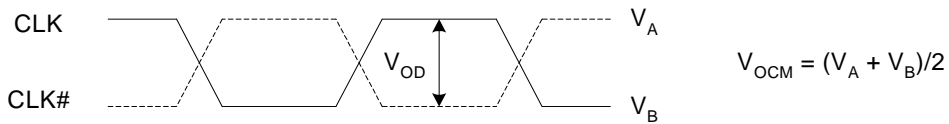
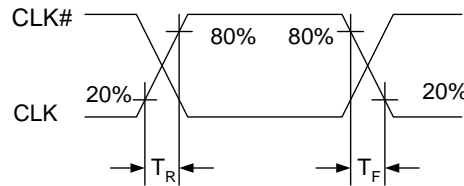


Figure 5. Output Rise and Fall Time



Notes

- 3. Refer to Figure 5 on page 4.
- 4. Characterized using an 18 pF parallel resonant crystal.
- 5. Not 100% tested, guaranteed by design and characterization.
- 6. Refer to Figure 6 on page 5.
- 7. Refer to Figure 7 on page 5.

Figure 6. RMS Phase Jitter

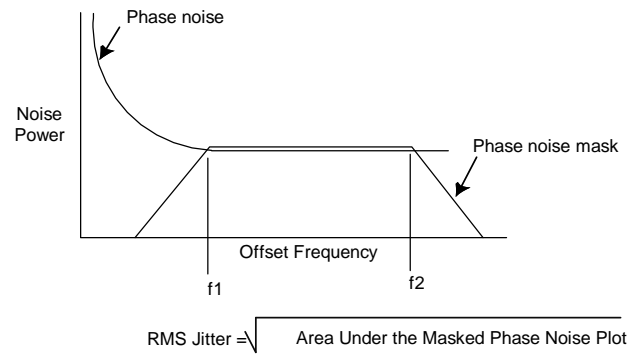


Figure 7. Output Duty Cycle

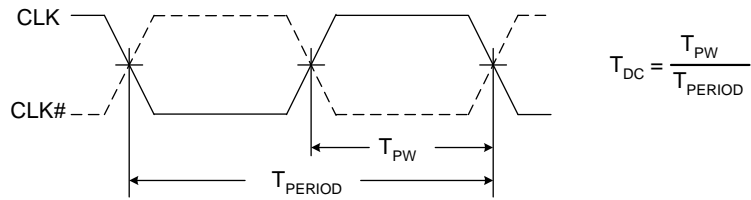
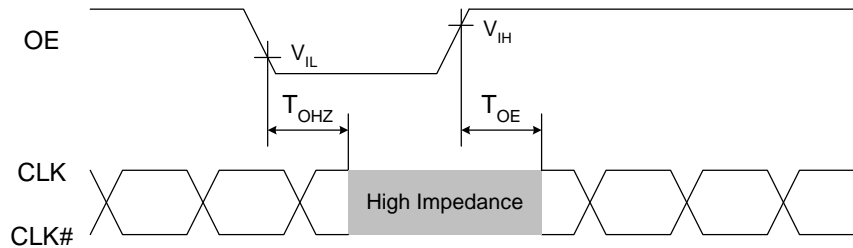


Figure 8. Output Enable Timing

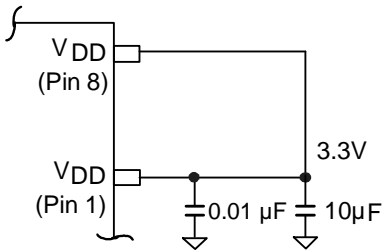


Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, noise at the power supply pins can degrade performance. To achieve optimum jitter performance, use good power supply isolation practices. Figure 9 illustrates a typical filtering scheme. Because all of the current flows through pin 1, the resistance and inductance between this pin and the supply is minimized. A 0.01 or 0.1 μF ceramic chip capacitor is also located close to this pin to provide a short and low impedance AC path to ground. A 1 to 10 μF ceramic or tantalum capacitor is located in the general vicinity of this device and may be shared with other devices.

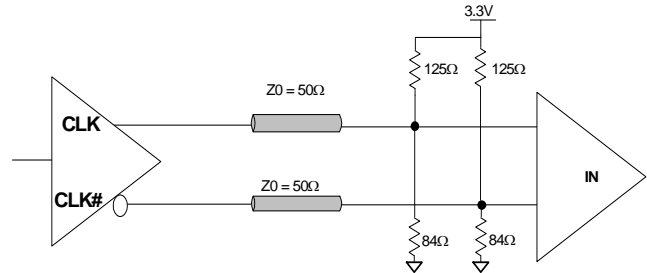
Figure 9. Power Supply Filtering



Termination for LVPECL Output

The CY2XP31 implements its LVPECL driver with a current steering design. For proper operation, it requires a 50 ohm dc termination on each of the two output signals. For 3.3 V operation, this data sheet specifies output levels for termination to $V_{DD}-2.0\text{ V}$. This same termination voltage can also be used for $V_{DD} = 2.5\text{ V}$ operation, or it can be terminated to $V_{DD}-1.5\text{ V}$. Note that it is also possible to terminate with 50 ohms to ground (V_{SS}), but the high and low signal levels differ from the data sheet values. Termination resistors are best located close to the destination device. To avoid reflections, trace characteristic impedance (Z_0) should match the termination impedance. Figure 10 shows a standard termination scheme.

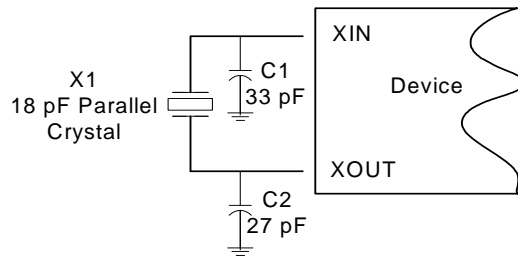
Figure 10. LVPECL Output Termination



Crystal Input Interface

The CY2XP31 is characterized with 18 pF parallel resonant crystals. The capacitor values shown in Figure 11 are determined using a 25 MHz 18 pF parallel resonant crystal and are chosen to minimize the ppm error. Note that the optimal values for C1 and C2 depend on the parasitic trace capacitance and are therefore layout dependent.

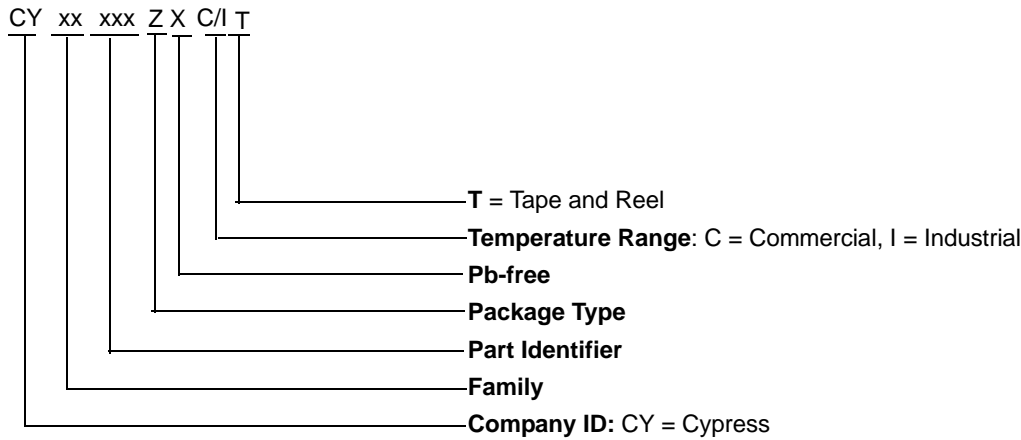
Figure 11. Crystal Input Interface



Ordering Information

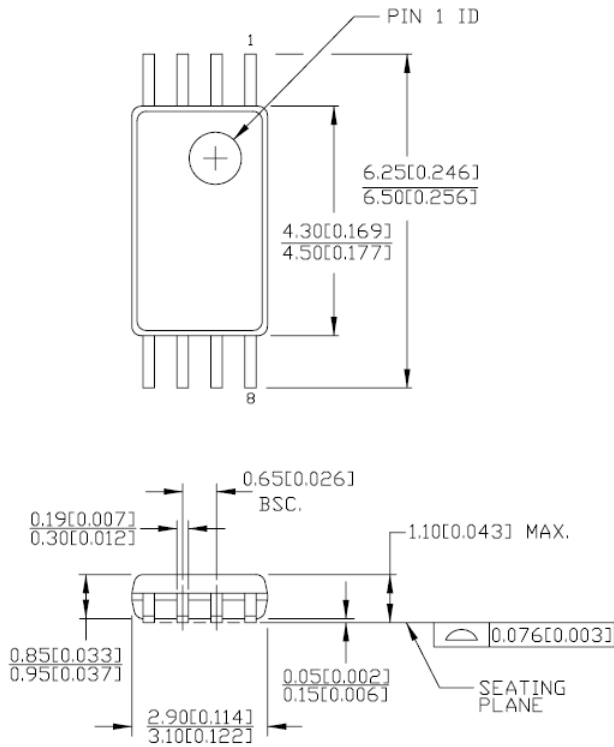
Part Number	Package Type	Product Flow
CY2XP31ZXC	8-Pin TSSOP	Commercial, 0°C to 70°C
CY2XP31ZXCT	8-Pin TSSOP – Tape and Reel	Commercial, 0°C to 70°C
CY2XP31ZXI	8-Pin TSSOP	Industrial, -40°C to 85°C
CY2XP31ZXIT	8-Pin TSSOP – Tape and Reel	Industrial, -40°C to 85°C

Ordering Code Definitions



Package Drawing and Dimensions

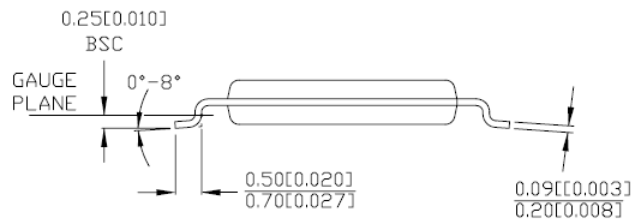
Figure 12. 8-Pin Thin Shrunken Small Outline Package (4.40 MM Body) Z8



DIMENSIONS IN MM [INCHES] MIN. MAX.

REFERENCE JEDEC MO-153

PART #	
Z08.173	STANDARD PKG.
ZZ08.173	LEAD FREE PKG.



51-85093 °C

Acronyms

Table 2. Acronyms Used

Acronym	Description
CLKOUT	Clock output
CMOS	Complementary metal oxide semiconductor
DPM	Die pick map
EPROM	Erasable programmable read only memory
LVDS	Low-voltage differential signaling
LVPECL	Low voltage positive emitter coupled logic
NTSC	National television system committee
OE	Output enable
PAL	Phase alternate line
PD	Power-down
PLL	Phase locked loop
PPM	Parts per million
TTL	Transistor transistor logic

Document Conventions

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
kHz	kilohertz
kΩ	kilohms
MHz	megahertz
MΩ	megaohms
μA	microamperes
μs	microseconds
μV	microvolts
μVrms	microvolts root-mean-square
mA	milliamperes
mm	millimeters
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms

Document History Page

Document Title: CY2XP31 312.5 MHz LVPECL Clock Generator				
Document Number: 001-06385				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	422680	RGL	See ECN	New data sheet
*A	506198	RGL	See ECN	Supplied values in TBDs, Change status from Advance Information to Preliminary
B	1337067	JWK / KVM /ARI	See ECN	Changed VCC to VDD*, VEE to VSS, Gave pins 1 and 8 the same name (VDD), Added MSL and CIN specifications, Removed pull up from pin 5, Changed V _{IL} , V _{IH} , I _{IH} , I _{DD} , I _{DDA} , V _{OH} , V _{OL} , t _R and t _F specifications, Added commercial temperature, Changed supply filtering recommendations Removed alternate termination figure, Cleaned up several drawings Fixed cross references and edited data sheet for template compliance, Title change
*C	2669117	KVM/ AESA	03/05/2009	Changed crystal frequency to 25 MHz only; removed other frequencies; output frequencies adjusted accordingly, Changed phase jitter value, Removed MSL spec Changed IIL and IIH values, Changed rise / fall time value from 350 ps to 500 ps Changed max junction temp from 125°C to 135°C, Added thermal resistance Clarified that IDD is with outputs loaded, Changed Data Sheet Status to Final.
*D	2700242	KVM/PYRS	04/30/2009	Typos: changed VCC to VDD OE pin capacitance changed from 7pF to 15pF Changed IDD footnote Reformatted AC & DC tables Added specs CINX and IOZ Added OE timing, and startup timing Added OE waveforms Added IDD for 2.5 V Changed footnote about external power dissipation
*E	2718433	WWZ/HMT	06/12/2009	No change. Submit to ECN for product launch.
*F	2767308	KVM	09/22/2009	Add I _{DD} spec for unterminated outputs Change parameter name for I _{DD} (terminated outputs) from I _{DD} to I _{DDT} Remove I _{DD} footnote about externally dissipated current Add footnote reference to C _{IN} and C _{INX} :not 100% tested Add max limit for T _R , T _F : 1.0 ns Change T _{LOCK} max from 10 ms to 5 ms
*G	2896121	KVM	03/19/2010	Updated Package Diagram (Figure 12)
*H	3219081	BASH	04/07/2011	Template and style updates as per current Cypress standards. Added ordering code definitions, acronyms, and units of measure. Updated package diagram to *C.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/Rf	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2006-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.