Dual PLL frequency synthesizer

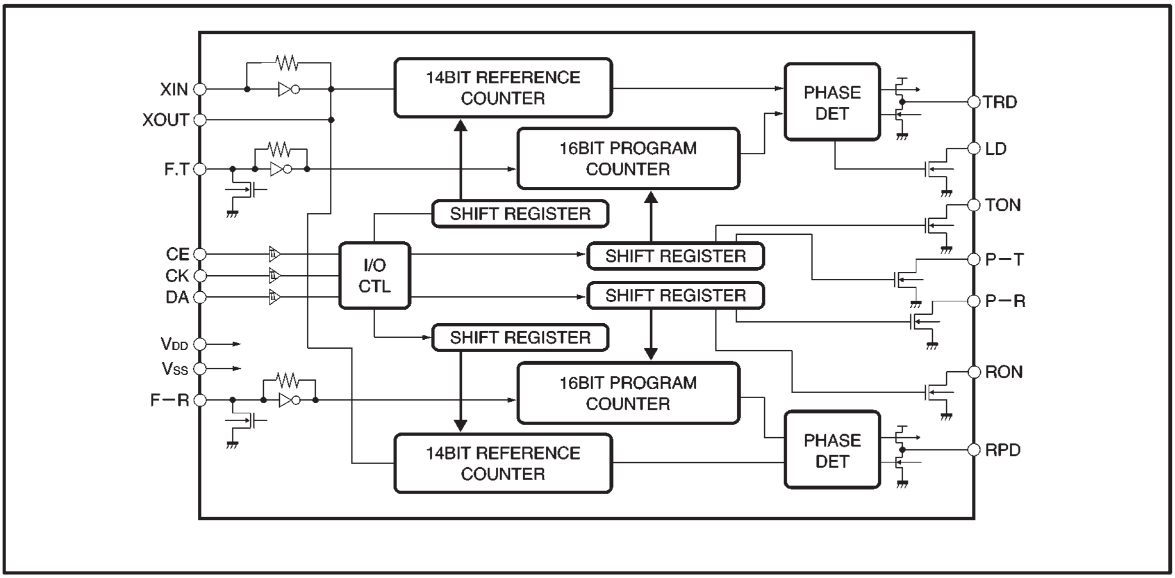
BU2630F / BU2630FV

The BU2630F / BU2630FV are a CMOS LSI with an internal dual PLL synthesizer.
VCOs for transmission and reception can be controlled independently, and the reference frequency and main counter settings can also be programmed separately. This product is designed for applications involving cordless telephones and communications equipment worldwide.

●Applications
Cordless telephones, amateur short wave radios, industrial transceivers, VHF / UHF frequency generators, and others

●Features
1) Operation possible at up to 80MHz (V_{DD} = 2.5).
2) Low current dissipation
   Dual-system operation : 2.2mA (typ), V_{DD} = 3V
   Single-system operation : 1.2mA (typ), V_{DD} = 3V
   Non-operating state : 0.2mA (typ), V_{DD} = 3V
3) 16-bit main counter.
4) Internal 14-bit reference frequency counter.
5) Unlock detection possible.
6) Four output ports. (open drain)
7) Control possible using 3-wire serial input.

●Block diagram



● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Power supply voltage		V_{DD}	−0.3～+7.0	V
Power dissipation	BU2630F	Pd	500*1	mW
	BU2630FV		350*2	
Operating temperature		Topr	−40～+85	℃
Storage temperature		Tstg	−55～+125	℃

*1 Reduced by 5.0mW for each increase in Ta of 1℃ over 25℃.
*2 Reduced by 3.5mW for each increase in Ta of 1℃ over 25℃.

● Recommended operating conditions (Ta = 25°C)

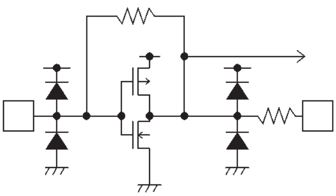
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	2.5	3.0	5.5	V

● Pin descriptions

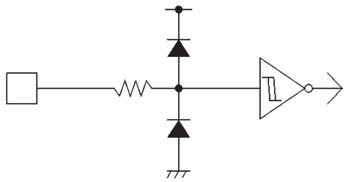
Pin No.	Pin name	Name	Function	I/O cuircuit
16	XOUT	Crystal resonator	For reference frequency	TYPE A
1	XIN			
2	V_{SS}			
3	RPD	Phase comparator output	This is LO if the locally divided value is higher than the reference frequency, HI if it is lower, and Z if it matches.	TYPE E
4	P−R	Output port	This is controlled by the input data.	TYPE D
5	RON			
6	F−R	VCO input	Local input for reception	TYPE F
7	CE	Chip enable	When CE is HIGH, the DA synchronized to the rise of CK is read into the internal shift register, and is latched at the timing of the CE fall.	TYPE B
8	CK	clock signal		
9	DA	serial data		
10	LD	Unlock output	This goes ON when the PLL is unlocked on the transmission side	TYPE D
11	F−T	VCO input	Local input for transmission	TYPE F
12	TON	Output port	This is controlled by the input data	TYPE D
13	P−T			
14	TPD	Phase comparator output	This is LO if the locally divided value is higher than the reference frequency, HI if it is lower, and Z if it matches.	TYPE E
15	V_{DD}	Power supply	2.5～5.5V	

●Input / output circuits

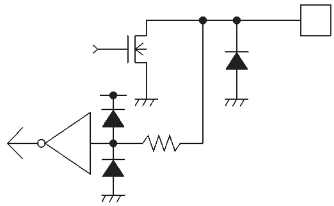
TYPE A



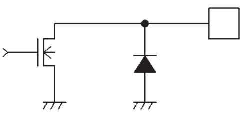
TYPE B



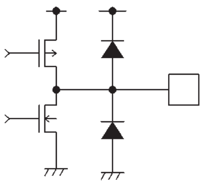
TYPE C



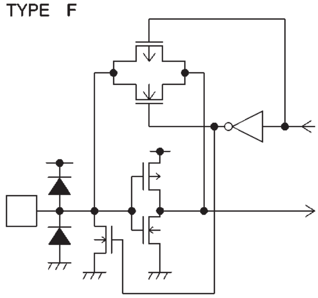
TYPE D



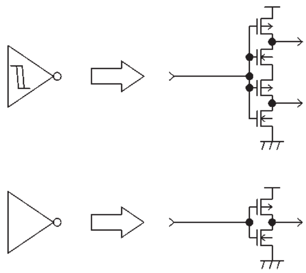
TYPE E



TYPE F



TYPE I



● Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 3.0V, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Power supply current 1	I_{DD1}	−	2.2	3.0	mA	Dual-system operation	F−T F−R=80MHz, 100mVrms XTAL=10.24MHz
Power supply current 2	I_{DD2}	−	1.2	2.0	mA	Single-system operation	
Power supply current 3	I_{DD3}	−	0.2	0.3	mA	With operation stopped: XTAL = 10.24 MHz	
Input high level voltage 1	V_{IH1}	0.8V_{DD}	−	−	V	CE CK DA	
Input low level voltage 1	V_{IL1}	−	−	0.2V_{DD}	V	CE CK DA	
Input high level current 1	I_{IH1}	−	−	1.0	μA	CE CK DA $V_{IN}=V_{DD}$	
Input high level current 2	I_{IH2}	−	0.3	−	μA	XIN $V_{IN}=V_{DD}$	
Input high level current 3	I_{IH3}	−	5.0	−	μA	F−T F−R $V_{IN}=V_{DD}$	
Input low level current 1	I_{IL1}	−1.0	−	−	μA	CE CK DA $V_{IN}=V_{SS}$	
Input low level current 2	I_{IL2}	−	−0.3	−	μA	XIN $V_{IN}=V_{SS}$	
Input low level current 3	I_{IL3}	−	−5.0	−	μA	F−T F−R $V_{IN}=V_{SS}$	
Output low level voltage 1	V_{OL1}	−	0.3	0.5	V	LD TON P−T RON P−R I_O=1.0mA	
Off level leakage current 1	I_{OFF1}	−	−	1.0	μA	LD TON P−T RON P−R V_O=10V	
Output low level voltage 2	V_{OL2}	−	−	0.3	V	F−T F−R I_{OUT}=0.1mA	
Output high level voltage	V_{OH3}	V_{DD}−50	V_{DD}−1.0	−	mV	TPD RPD I_{OUT}=−0 μA	
Output low level voltage	V_{OL3}	−	1.3	50	mV	TPD RPD I_{OUT}=0 μA	
Output high level voltage	V_{OH4}	V_{DD}−100	V_{DD}−40	−	mV	TPD RPD I_{OUT}=−100 μA	
Output low level voltage	V_{OL4}	−	30	100	mV	TPD RPD I_{OUT}=100 μA	
Off level leakage current 2	I_{OFF2}	−	−	100	nA	TPD RPD $V_{OUT}=V_{DD}$	
Off level leakage current 3	I_{OFF3}	−100	−	−	nA	TPD RPD $V_{OUT}=V_{SS}$	
Internal feedback resistance 1	R_{F1}	−	10	−	MΩ	XIN	
Internal feedback resistance 2	R_{F2}	−	500	−	kΩ	F−T F−R	
Input frequency 1	F_{IN1}	1.0	10.24	16.0	MHz	XIN, sine wave, C coupling	
Input frequency 2	F_{IN2}	1.0	−	20	MHz	F-T F-R, sine wave, C coupling*2, V_{IN} = 100 mVrms	
Input frequency 3	F_{IN3}	50	−	80	MHz	F-T F-R, sine wave, C coupling*2, V_{IN} = 100 mVrms	
Input frequency 4	F_{IN4}	20	−	50	MHz	F-T F-R, sine wave, C coupling*2, V_{IN} = 50 mVrms	
Input frequency 5*1	F_{IN5}	0.4	−	20	MHz	F-T F-R, sine wave, C coupling*2, V_{IN} =100mVrms	
Maximum input amplitude	$F_{INMax.}$	−	−	V_{DD}+ 0.3	V_{P-P}	XIN , F−T F−R	
Input capacitance	C_{IN}	−	4	7	PF	F−T F−R	
Minimum pulse width	TW	1.0	−	−	μs	CK, DA	
Input data rise time	TR	−	−	300	ns	CK, DA	
Input data fall time	TF	−	−	300	ns	CE, CK, DA	

◎ Not designed for radiation resistance.

*1 PS = 1

*2 Minimum input level at which operation is possible

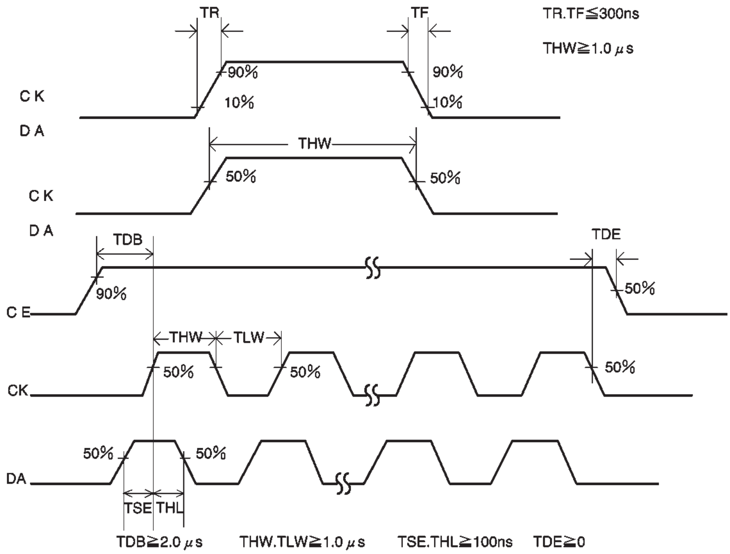
Divider values which can be set

Program divider: PS = 0: 256 to 65535, PS = 1: 3 to 4095

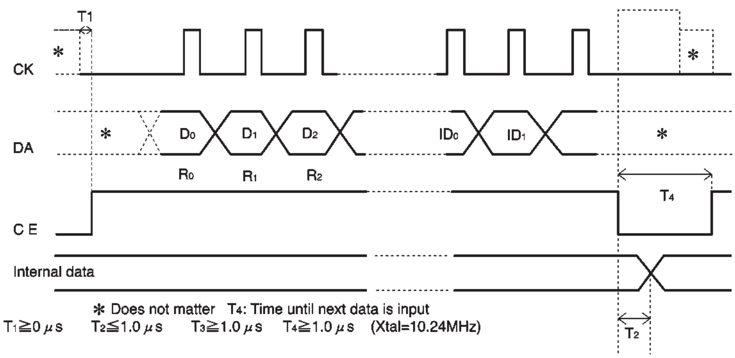
Reference frequency divider: 3 to 16383

●Circuit operation

Input data switching characteristics



Input data format



Programmable divider and control data input: TX side (ID_0 = 0, ID_1 = 0), RX side (ID_0 = 1, ID_1 = 0)

LSB ← Input from D_0

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	
				P-T	TON	OFF	PS	T_0	T_1	ID_0	ID_1					MSB
				(P-R	TON	OFF	PS	T_0	T_1)							

Reference frequency divider data input: TX side (ID_0 = 0, ID_1 = 1), RX side (ID_0 = 1, ID_1 = 1)

R_0	R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9	R_{10}	R_{11}	R_{12}	R_{13}	PL	PH	
LSB				*	*	LD_0	LD_1	*	*	ID_0	ID_1					MSB

* Does not matter (LD_0 and LD_{10} are valid on TX side only)

Description of data

(1) Programmable divider data: D_0 ~ D_{15}

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

Example: For a transmission frequency of 46.610MHz and a reference frequency of 5.00 kHz
No. of divisions: 46.610 ÷ 5.00 kHz = 9322 (D) = 246A (H)

0	1	0	1	0	1	1	0	0	0	1	0	0	1	0	0
A				6				4				2			

(2) Reference frequency data: R_0 ~ R_{13}

R_0	R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9	R_{10}	R_{11}	R_{12}	R_{13}

Example: When XTAL = 10.24 MHz and reference frequency is 5.00 kHz
No. of divisions: 10.24 MHz ÷ 5.00 kHz = 2048 (D) = 800 (H)

0	0	0	0	0	0	0	0	0	0	0	1	0	0
0				0				8				0	

(3) Output port control data : P-T (P-R) TON (RON)
1 : Open drain output ON (LO)
0 : Open drain output OFF (HI)

(4) OFF transmission side (reception side) : Operation stopped
F - T (F - R) pull-down : TPD (RPD) high-impedance, LD = OFF

(5) PS
Programmable device change : No. of divisions = 3 ~ 4095

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
*	*	*	*	LSB											MSB
DON'T CARE															

(6) PL, PH, and PD pin control

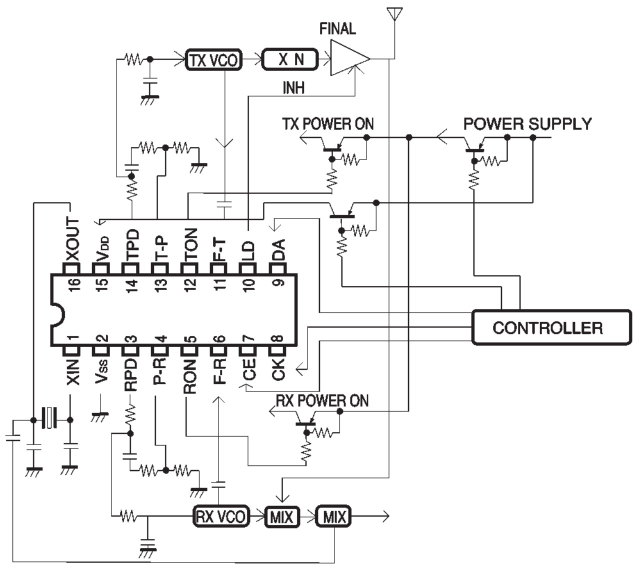
0 0 : PLL operation
1 0 : Forced LO state
0 1 : Forced HI state
1 1 : Forced LO state

(7) LD_0, LD_1, LD pin control (valid only on TX side)

0 0 : ON when unlocked (LO)
0 1 : Air pulse output
1 0 : Forced ON state (LO)
1 1 : Forced OFF state (HI)

(8) Input (00) to test T0 and T1.

● Application example



*: Immediately after the power supply is turned on,
the various pins remain unstable until data is input.

Fig. 1

●Electrical characteristic curves

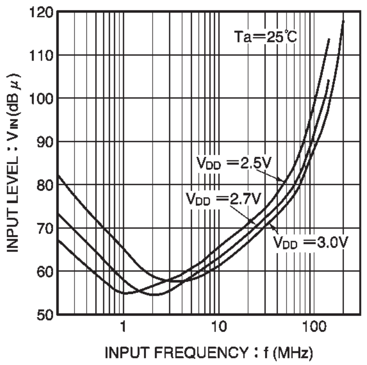


Fig. 2 Input frequency vs. input level

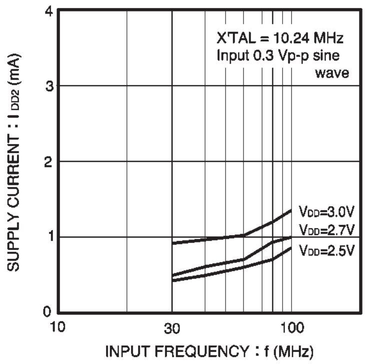


Fig. 3 Input frequency vs. supply current (for single operation)

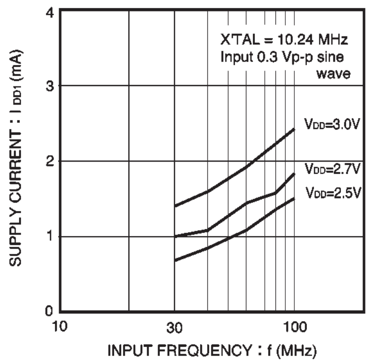
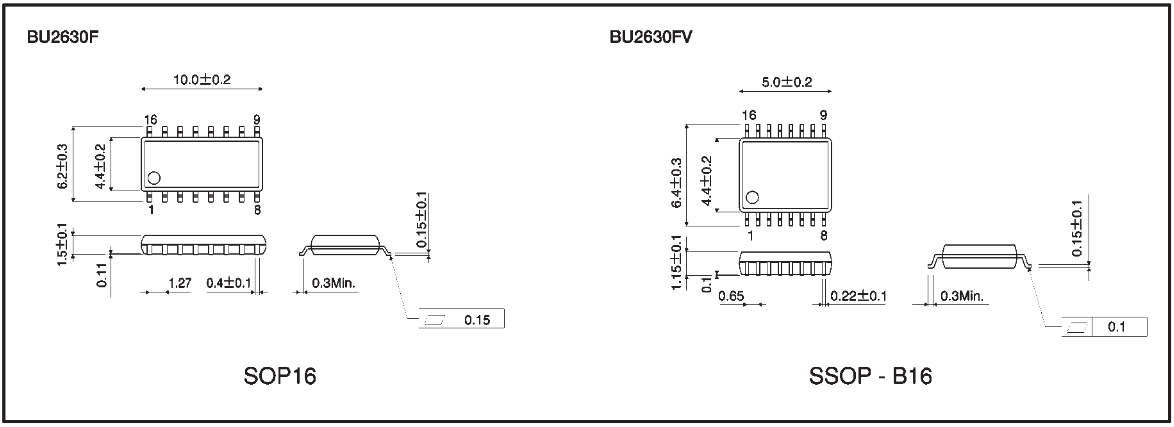


Fig. 4 Input frequency vs. supply current (for dual operation)

●External dimensions (Units: mm)



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