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Low EMI Spectrum Spread Clock

Features

- Spread Spectrum clock generator (SSCG) with 1x, 2x, and 4x outputs
- 6- to 82-MHz operating frequency range
- Modulates external clocks including crystals, crystal oscillators, or ceramic resonators
- Programmable modulation with simple R-C external loop filter (LF)
- Center spread modulation
- 3V-5V power supply
- TTL-/CMOS-compatible outputs
- Low short-term jitter
- Low-power Dissipation
 - 3.3 VDC = 37 mW – typical
 - 5.0 VDC = 115 mW – typical
- Available in 8-pin SOIC and TSSOP packages

Applications

- Desktop/notebook computers
- Printers, copiers, and MFP
- Scanners and fax
- LCD displays and monitors
- CD-ROM, VCD, and DVD
- Automotive and embedded systems
- Networking, LAN/WAN
- Digital cameras and camcorders
- Modems

Benefits

- Programmable EMI reduction
- Fast time to market
- Lower cost of compliance
- No degradation in rise/fall times
- Lower component and PCB layer count

Functional Description

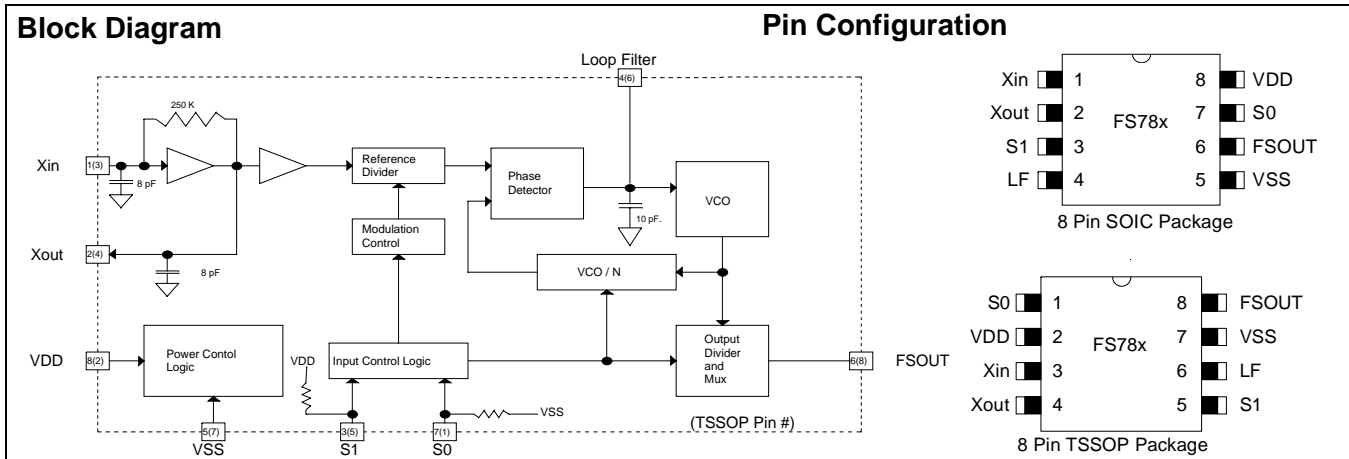
The Cypress FS781/82/84 are Spread Spectrum clock generator ICs (SSCG) designed for the purpose of reducing electromagnetic interference (EMI) found in today's high-speed digital systems.

The FS781/82/84 SSCG clocks use a Cypress-proprietary technology to modulate the input clock frequency, XIN, by modulating the frequency of the digital clock. By modulating the reference clock the measured EMI at the fundamental and harmonic frequencies of FSOUT is greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements without degrading digital waveforms.

The Cypress FS781/82/84 clocks are very simple and versatile devices to use. By programming the two range select lines, S0 and S1, any frequency from 6- to 82-MHz operating range can be selected. The FS781/2/4 are designed to operate over a very wide range of input frequencies and provides 1x, 2x, and 4x modulated clock outputs.

The FS78x devices have a simple frequency selection table that allows operation from 6 MHz to 82 MHz in four separate ranges. The bandwidth of the frequency spread at FSOUT is determined by the values of the loop filter components. The modulation rate is determined internally by the input frequency and the selected input frequency range.

The Bandwidth of these products can be programmed from as little as 1.0% up to as much as 4.0% by selecting the proper loop filter value. Refer to the Loop Filter Selection chart in *Table 2* and *Table 3* for the recommended values. Due to a wide range of application requirements, an external loop filter (LF) is used on the FS78x products. The user can select the exact amount of frequency modulation suitable for the application. Using a fixed internal loop filter would severely limit the use of a wide range of modulation bandwidths (Spread %) to a few discrete values. Refer to FS791/2/4 products for applications requiring 80- to 140-MHz frequency range.



Pin Description

| Pin | Name | I/O | Type | Description |
|---------------------------|-----------------------------------|-----|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1/2 (SOIC) 3/4 (TSSOP) | X _{IN} /X _{OUT} | I/O | Analog | Pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. X _{IN} may be connected to TTL/CMOS external clock source. If X _{IN} is connected to an external clock other than crystal, leave X _{OUT} (pin 2) unconnected. |
| 7/3 (SOIC) 1/5 (TSSOP) | S0 / S1 | I | CMOS/TTL | Digital control inputs to select input frequency range and output frequency scaling. Refer to <i>Table 2</i> and <i>Table 3</i> for selection. S0 has internal pull-down. S1 has internal pull-up. |
| 4 (SOIC) 6 (TSSOP) | LF | I | Analog | Loop Filter. Single ended three-state output of the phase detector. A two-pole passive loop filter is connected to LF. |
| 6 (SOIC) 8 (TSSOP) | FSOUT | O | CMOS/TTL | Modulated Clock Frequency Output. The center frequency is the same as the input reference frequency for FS781. Input frequency is multiplied by 2x and 4x for FS782 and FS784, respectively. |
| 8 (SOIC) 2 (TSSOP) | V _{DD} | P | Power | Positive Power Supply. |
| 5 (SOIC) 7 (TSSOP) | V _{SS} | P | Power | Power Supply Ground. |

Output Frequency Selection

Table 1. FSOUT SSCG (Modulated Output Clock) Product Selection

| Product Number | FSOUT Frequency Scaling | Description |
|----------------|-------------------------|---------------------------------------|
| FS781 | 1x | 1x modulated frequency of input clock |
| FS782 | 2x | 2x modulated frequency of input clock |
| FS784 | 4x | 4x modulated frequency of input clock |

Loop Filter Selection Chart

The following table provides a list of recommended loop filter values for the FS781/82/84. The FS78X is divided into four ranges and operated at both 3.3V and 5.5 VDC. The loop filter at the right is representative of the loop filter components in *Table 2*.

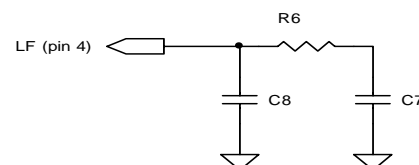


Table 2. FS781/82/84 Recommended Loop Filter Values C7 (pF) @ +3.3 VDC ±5% (R6 = 3.3K)^[1, 2, 3, 4]

| Input MHz | S1 | S0 | BW = 1.0% ^[3] | BW = 1.5% ^[3] | BW = 2.0% ^[3] | BW = 2.5% ^[3] | BW = 3.0% ^[3] | BW = 3.5% ^[3] | BW = 4.0% ^[3] |
|-----------|----|----|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| 6 | 0 | 0 | 10,000/1000 | 1550 | 910 | 780 | 700 | 640 | 560 |
| 8 | 0 | 0 | 10,000/330 | 990 | 820 | 640 | 520 | 450 | 400 |
| 10 | 0 | 0 | 1040 | 680 | 460 | 360 | 300 | 240 | 210 |
| 12 | 0 | 0 | 830 | 420 | 300 | 220 | 200 | 190 | 170 |
| 14 | 0 | 0 | 580 | 230 | 200 | 160 | 140 | 100 | 80 |
| 16 | 0 | 1 | 10000 | 980 | 760 | 580 | 470 | 410 | 385 |
| 18 | 0 | 1 | 1200 | 750 | 580 | 470 | 415 | 370 | 300 |
| 20 | 0 | 1 | 1000 | 730 | 470 | 390 | 320 | 220 | 190 |
| 22 | 0 | 1 | 960 | 640 | 410 | 270 | 230 | 200 | 180 |
| 24 | 0 | 1 | 920 | 400 | 250 | 210 | 180 | 160 | 150 |
| 26 | 0 | 1 | 660 | 300 | 220 | 180 | 150 | 140 | 120 |
| 28 | 0 | 1 | 470 | 230 | 180 | 150 | 130 | 100 | 70 |
| 30 | 0 | 1 | 470 | 180 | 140 | 120 | 100 | 80 | 60 |
| 32 | 0 | 1 | 330 | 170 | 120 | 100 | 82 | 68 | 47 |
| 34 | 1 | 0 | 10000 | 860 | 640 | 520 | 430 | 380 | 330 |
| 36 | 1 | 0 | 2200 | 820 | 620 | 470 | 400 | 330 | 290 |
| 38 | 1 | 0 | 1500 | 690 | 520 | 410 | 340 | 290 | 240 |
| 40 | 1 | 0 | 960 | 600 | 420 | 340 | 280 | 220 | 160 |
| 42 | 1 | 0 | 940 | 620 | 380 | 275 | 230 | 210 | 180 |
| 44 | 1 | 0 | 950 | 680 | 400 | 250 | 210 | 190 | 170 |
| 46 | 1 | 0 | 900 | 580 | 270 | 220 | 190 | 180 | 165 |
| 48 | 1 | 0 | 790 | 440 | 260 | 210 | 180 | 160 | 140 |
| 50 | 1 | 0 | 660 | 360 | 250 | 190 | 170 | 150 | 140 |
| 52 | 1 | 0 | 470 | 325 | 220 | 185 | 155 | 135 | 120 |
| 54 | 1 | 0 | 470 | 270 | 200 | 170 | 140 | 130 | 100 |
| 56 | 1 | 0 | 445 | 250 | 185 | 150 | 120 | 85 | 47 |
| 58 | 1 | 0 | 430 | 210 | 165 | 130 | 100 | 65 | 33 |
| 60 | 1 | 0 | 295 | 185 | 150 | 120 | 100 | 90 | 82 |
| 62 | 1 | 0 | 270 | 220 | 150 | 120 | 100 | 82 | 68 |
| 64 | 1 | 1 | 1180 | 860 | 560 | 410 | 340 | 290 | 230 |
| 65 | 1 | 1 | 1180 | 850 | 540 | 400 | 330 | 280 | 220 |
| 66 | 1 | 1 | 1180 | 760 | 560 | 350 | 260 | 220 | 210 |
| 68 | 1 | 1 | 1180 | 750 | 500 | 320 | 260 | 230 | 210 |
| 70 | 1 | 1 | 1120 | 740 | 470 | 370 | 300 | 240 | 170 |
| 72 | 1 | 1 | 1160 | 780 | 470 | 300 | 250 | 220 | 190 |
| 74 | 1 | 1 | 1110 | 770 | 470 | 280 | 230 | 210 | 190 |
| 76 | 1 | 1 | 1000 | 720 | 440 | 240 | 210 | 190 | 170 |
| 78 | 1 | 1 | 910 | 670 | 270 | 210 | 190 | 170 | 160 |
| 80 | 1 | 1 | 900 | 620 | 260 | 210 | 190 | 170 | 156 |
| 82 | 1 | 1 | 900 | 540 | 250 | 210 | 190 | 170 | 150 |

Notes:

1. If the value selected from the above chart is not a standard, use the next available larger value.
2. All bandwidths indicated above are total peak-to-peak spread. 1% = +0.5% to -0.5%. 4% = +2.0% to -2.0%.
3. If C8 is not listed in the chart for a particular bandwidth and frequency, it is not used in the loop filter.
4. Contact Cypress for LF values less than 1.0% bandwidth.

Table 3. FS781/82/84 Recommended Loop Filter Values C7 (pF) @ +5.0 VDC ±5% (R6 = 3.3K)^[1, 2, 3, 4]

| Input MHz | S1 | S0 | BW = 1.0% ^[3] | BW = 1.5% ^[3] | BW = 2.0% ^[3] | BW = 2.5% ^[3] | BW = 3.0% ^[3] | BW = 3.5% ^[3] | BW = 4.0% ^[3] |
|-----------|----|----|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| 6 | 0 | 0 | 1140 | 1030 | 930 | 830 | 710 | 610 | 510 |
| 8 | 0 | 0 | 1170 | 970 | 740 | 570 | 460 | 400 | 280 |
| 10 | 0 | 0 | 1030 | 660 | 430 | 350 | 280 | 210 | 130 |
| 12 | 0 | 0 | 760 | 340 | 230 | 200 | 180 | 160 | 130 |
| 14 | 0 | 0 | 450 | 240 | 180 | 140 | 100 | 70 | 50 |
| 16 | 0 | 1 | 2490 | 970 | 730 | 590 | 480 | 430 | 370 |
| 18 | 0 | 1 | 2490 | 870 | 650 | 510 | 430 | 370 | 310 |
| 20 | 0 | 1 | 1360 | 680 | 480 | 370 | 280 | 190 | 250 |
| 22 | 0 | 1 | 990 | 560 | 330 | 260 | 230 | 200 | 190 |
| 24 | 0 | 1 | 820 | 360 | 250 | 200 | 180 | 160 | 150 |
| 26 | 0 | 1 | 530 | 270 | 210 | 170 | 150 | 110 | 90 |
| 28 | 0 | 1 | 430 | 230 | 180 | 150 | 110 | 100 | 90 |
| 30 | 0 | 1 | 250 | 200 | 150 | 110 | 100 | 90 | 80 |
| 32 | 1 | 0 | Note 4 | 1000 | 740 | 570 | 470 | 410 | 370 |
| 34 | 1 | 0 | Note 4 | 990 | 710 | 520 | 420 | 360 | 300 |
| 36 | 1 | 0 | Note 4 | 970 | 670 | 480 | 380 | 310 | 230 |
| 38 | 1 | 0 | Note 4 | 880 | 560 | 380 | 310 | 270 | 220 |
| 40 | 1 | 0 | Note 4 | 800 | 460 | 290 | 240 | 230 | 220 |
| 42 | 1 | 0 | 1030 | 680 | 360 | 260 | 220 | 200 | 190 |
| 44 | 1 | 0 | 790 | 560 | 260 | 220 | 200 | 190 | 170 |
| 46 | 1 | 0 | 1110 | 420 | 280 | 210 | 180 | 170 | 140 |
| 48 | 1 | 0 | 1110 | 280 | 200 | 190 | 170 | 140 | 120 |
| 50 | 1 | 0 | 830 | 330 | 200 | 180 | 160 | 130 | 110 |
| 52 | 1 | 0 | 560 | 340 | 205 | 170 | 140 | 120 | 90 |
| 54 | 1 | 0 | 510 | 280 | 180 | 140 | 110 | 110 | 90 |
| 56 | 1 | 0 | 470 | 210 | 160 | 120 | 100 | 90 | 90 |
| 58 | 1 | 0 | 450 | 220 | 250 | 110 | 90 | 80 | 80 |
| 60 | 1 | 0 | 430 | 240 | 120 | 90 | 80 | 80 | 70 |
| 62 | 1 | 1 | Note 4 | 800 | 580 | 430 | 330 | 250 | 180 |
| 64 | 1 | 1 | Note 4 | 720 | 490 | 375 | 285 | 200 | 140 |
| 66 | 1 | 1 | Note 4 | 630 | 400 | 320 | 240 | 150 | 100 |
| 68 | 1 | 1 | Note 4 | 690 | 365 | 285 | 225 | 170 | 140 |
| 70 | 1 | 1 | Note 4 | 650 | 330 | 250 | 210 | 190 | 180 |
| 72 | 1 | 1 | Note 4 | 575 | 340 | 250 | 210 | 190 | 170 |
| 74 | 1 | 1 | Note 4 | 500 | 355 | 245 | 205 | 180 | 165 |
| 76 | 1 | 1 | Note 4 | 550 | 330 | 230 | 200 | 175 | 160 |
| 78 | 1 | 1 | Note 4 | 600 | 290 | 220 | 190 | 170 | 155 |
| 80 | 1 | 1 | Note 4 | 570 | 240 | 210 | 185 | 165 | 150 |
| 82 | 1 | 1 | Note 4 | 540 | 250 | 200 | 180 | 160 | 140 |

Table 4. Modulation Rate Divider Ratios

| S1 | S0 | Input Frequency Range (MHz) | Modulation Divider Number |
|----|----|-----------------------------|---------------------------|
| 0 | 0 | 6 to 16 | 120 |
| 0 | 1 | 16 to 32 | 240 |
| 1 | 0 | 32 to 66 | 480 |
| 1 | 1 | 66 to 82 | 720 |

SSCG Modulation Profile

The digital control inputs S0 and S1 determine the modulation frequency of FS781/2/4 products. The input frequency is divided by a fixed number, depending on the operating range that is selected. The modulation frequency of the FS78x can be determined from *Table 4*. To compute the modulation frequency, determine the values of S0 and S1, and find the modulation divider number in *Table 4*.

Theory of Operation

The FS781/82/84 devices are phase-locked loop-(PLL)-type clock generators using Direct Digital Synthesis (DDS). By precisely controlling the bandwidth of the output clock, the FS781/2/4 products become a low-EMI clock generator. The theory and detailed operation of these products will be discussed in the following sections.

EMI

All clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50%. Because of the 50/50 duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics (e.g., third, fifth, seventh). It is possible to reduce the amount of energy contained in the fundamental and harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, conse-

quently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test is able to satisfy agency requirements for EMI. Conventional methods of reducing EMI have been to use shielding, filtering, multi-layer PCBs, etc. These FS781/2 and 4 reduce the peak energy in the clock by increasing the clock bandwidth and lowering the Q of the clock.

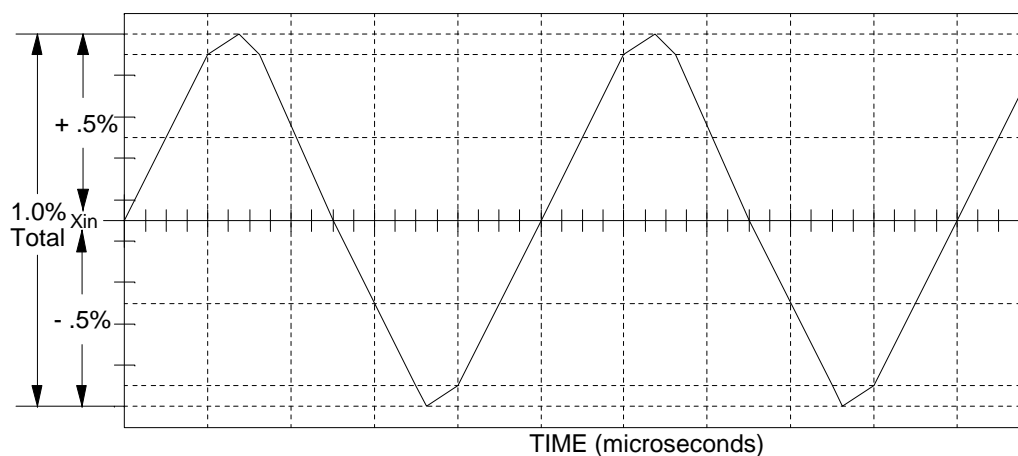
SSCG

The FS781/82/84 products use a unique method of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak to peak and cycle to cycle. The FS78x products take a narrow band digital reference clock in the range of 6–82 MHz and produce a clock that sweeps between a controlled start and stop frequency and precise rate of change. To understand what happens to an SSCG clock, consider that we have a 20-MHz clock with a 50% duty cycle. From a 20-MHz clock we know the following:

Clock Frequency = $F_c = 20 \text{ MHz}$.

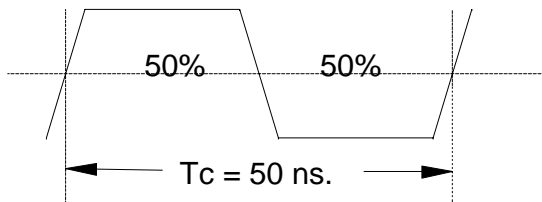
Clock Period = $T_c = 1/20 \text{ MHz} = 50 \text{ ns}$.

Consider that this 20-MHz clock is applied to the X_{IN} input of the FS78x as either an externally driven clock or the result of a parallel resonant crystal connected to pins 1 and 2 of the FS78x. Also consider that the products are operating from a 5V DC power supply and the loop filter is set for a total bandwidth spread of 2%. Refer to *Figure 2*.


Figure 1. Frequency Profile in Time Domain^[5]

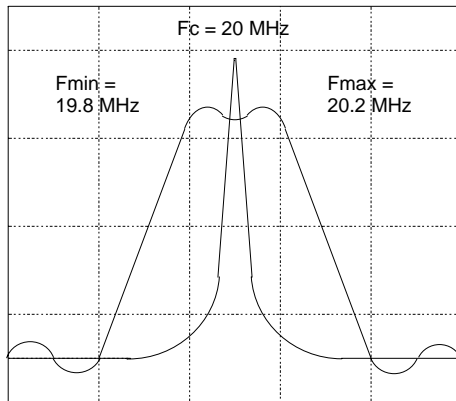
Note:

5. With the correct loop filter connected to Pin 4, the following profile will provide the best EMI reduction. This profile can be seen on a Time Domain Analyzer.

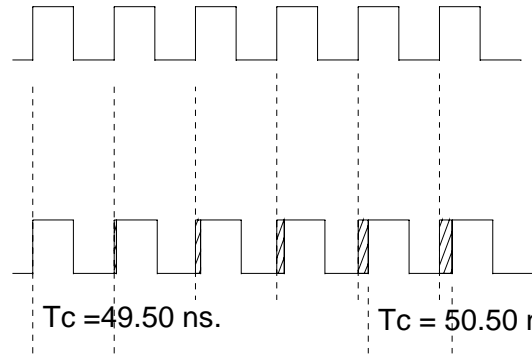

Figure 2. 20-MHz Unmodulated Clock

From the above parameters, the output clock at FSOUT will be sweeping symmetrically around a center frequency of 20 MHz.

The minimum and maximum extremes of this clock will be +200 kHz and -200 kHz. So we have a clock that is sweeping from 19.8 MHz to 20.2 MHz and back again. If we were to look at this clock on a spectrum analyzer we would see the picture in *Figure 3*. Keep in mind that this is a drawing of a perfect clock with no noise.


Figure 3. Spectrum Analysis of 19.8–20.2 MHz Clock

We see that the original 20-MHz reference clock is at the center frequency (F_c), and the min. and max. extremes are positioned symmetrically about the center frequency. This type of modulation is called Center-Spread. *Figure 4* shows a 20-MHz clock as it would be seen on an oscilloscope. The top trace is the non-modulated reference clock. The bottom trace is the modulated clock at pin 6. From this comparison chart you can see that the frequency is decreasing and the period of each successive clock is increasing. The T_c measurements on the left and right of the bottom trace indicate the max. and min. extremes of the clock. Intermediate clock changes are small and accumulate to achieve the total period deviation. The reverse of this figure would show the clock going from minimum extreme back to the high extreme.


Figure 4. Period Comparison Chart

Looking at *Figure 3*, you will note that the peak amplitude of the 20-MHz non-modulated clock is higher than the wideband modulated clock. This difference in peak amplitudes between modulated and unmodulated clocks is the reason why SSCG clocks are so effective in digital systems. This figure refers to the fundamental frequency of a clock. A very important characteristic of the SSCG clock is that the bandwidth of the fundamental frequency is multiplied by the harmonic number. In other words, if the bandwidth of a 20-MHz clock is 200 kHz, the bandwidth of the third harmonic will be 3×200 , or 600 kHz. The amount of bandwidth is relative to the amount of energy in the clock. Consequently, the wider the bandwidth, the greater the energy reduction of the clock.

Most applications will not have a problem meeting agency specifications at the fundamental frequency. It is the higher harmonics that usually cause the most problems. With an SSCG clock, the bandwidth and peak energy reduction increases with the harmonic number. Consider that the eleventh harmonic of a 20-MHz clock is 220 MHz. With a total spread of 200 kHz at 20 MHz, the spread at the eleventh harmonic would be 2.20 MHz, which greatly reduces the peak energy content. It is typical to see as much as 12- to 18-dB reduction at the higher harmonics, due to a modulated clock.

The difference in the peak energy of the modulated clock and the non-modulated clock in typical applications will see a 2 – 3 dB reduction at the fundamental and as much as 8 – 10 dB reduction at the intermediate harmonics: third, fifth, seventh, etc. At the higher harmonics, it is quite possible to reduce the peak harmonic energy, compared to the unmodulated clock, by as much as 12 to 18 dB.

Application Notes and Schematic

Figure 5 is configured for the following parameters:

Package selected = FS781.

X_{IN} = 20-MHz crystal

FSOUT = 20 MHz ($S_0 = 1$ and $S_1 = 0$).

Bandwidth of the FSOUT clock is determined by the values of the loop filter connected to pin 4.

Crystal is 20 MHz is 1st Order with 18 pF load capacitance.

If Crystal load capacitance is different than 18 pF, C1 and C2 must be re-calculated.

For third overtone crystals, a parallel or series resonant trap is required.

Mount loop filter components as close to LF pin as possible.

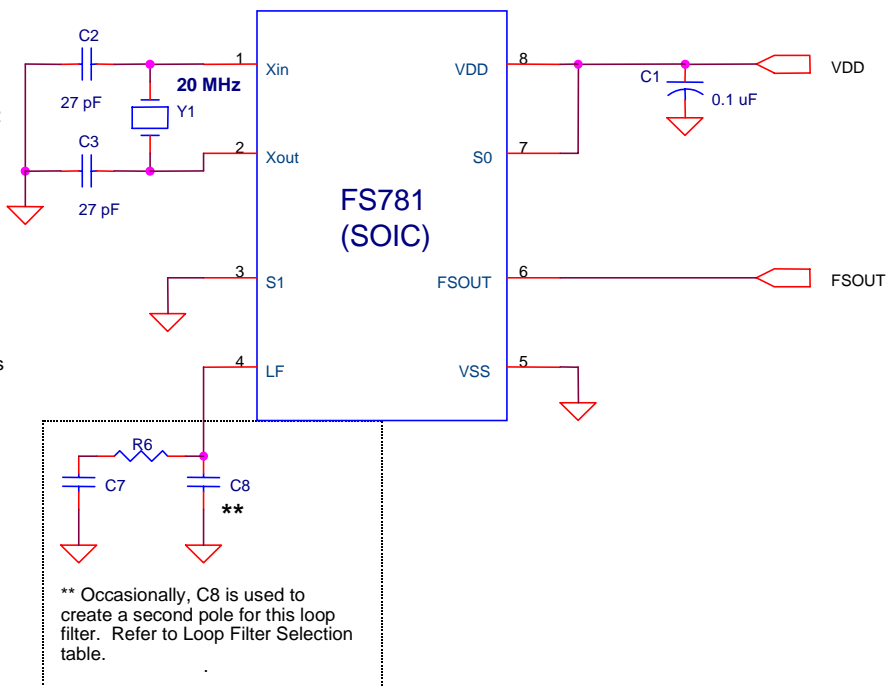


Figure 5. FS781 Schematic

Absolute Maximum Ratings^[6]

This device contains circuitry to protect the input against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of any voltage higher than the absolute maximum rated voltages to

this circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range, $V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$. All digital inputs are tied high or low internally. Refers to electrical specifications for operating supply range.

Table 5. Absolute Maximum Ratings

| Parameter | Description | Min. | Max. | Unit |
|-------------|------------------------------|------|----------------|------|
| V_{DD} | Operating Voltage | 3.0 | 6.0 | VDC |
| V_{IRvss} | Input, relative to V_{SS} | -0.3 | $V_{DD} + 0.3$ | VDC |
| V_{ORvss} | Output, relative to V_{SS} | -0.3 | $V_{DD} + 0.3$ | VDC |
| TOP | Temperature, Operating | 0 | +70 | °C |
| TST | Temperature, Storage | -65 | +150 | °C |
| T_J | Temperature, Junction | - | +125 | °C |

Table 6. DC Electrical Characteristics $V_{DD} = 3.3V$ and $5.0V \pm 10\%$, $X_{IN} = 48$ MHz, $T_A = 0^\circ C$ to $70^\circ C$

| Parameter | Description | Min. | Typ. | Max. | Unit |
|------------|------------------------------------------------------|----------------|------|----------------|----------|
| V_{IL} | Input Low Voltage | - | | $0.3 * V_{DD}$ | VDC |
| V_{IH} | Input High Voltage | $0.7 * V_{DD}$ | | | VDC |
| I_{IL} | Input Low Current | | | 100 | μA |
| I_{IH} | Input High Current | | | 100 | μA |
| V_{OL} | Output Low Voltage $I_{OL} = 10$ mA, $V_{DD} = 5V$ | | | 0.4 | VDC |
| V_{OH} | Output High Voltage $I_{OH} = 10$ mA, $V_{DD} = 5V$ | $V_{DD} - 1.0$ | | | VDC |
| V_{OL} | Output Low Voltage $I_{OL} = 6$ mA, $V_{DD} = 3.3V$ | | | 0.4 | VDC |
| V_{OH} | Output High Voltage $I_{OH} = 5$ mA, $V_{DD} = 3.3V$ | 2.4 | | | VDC |
| Rpd | Resistor, Pull-down (Pin 7) | 60K | 125K | 200K | Ω |
| Rpu | Resistor, Pull-up (Pin 3) | 60K | 125K | 200K | Ω |
| C_{xin} | Input Capacitance (Pin 1) | | 8 | | pF |
| C_{xout} | Output Capacitance (Pin 2) | | 10 | | pF |
| I_{CC} | 5V Dynamic Supply Current (CL = No Load) | | 38 | | mA |
| I_{CC} | 3.3V Dynamic Supply Current (CL = No Load) | | 20 | | mA |
| ISC | Short Circuit Current (FSOUT) | | 25 | | mA |
| BW | BW% Variations, $3.30V^{[7]}$ | -20 | 0 | +20 | % |
| BW | BW% Variations, $5.00V^{[7]}$ | -30 | 0 | +30 | % |

Table 7. Timing Electrical Characteristics $V_{DD} = 3.3V$ and $5.0V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$, $C_L = 15$ pF, $X_{IN} = 48$ MHz

| Parameter | Description | Min. | Typ. | Max. | Unit |
|-----------|---------------------------------------------------|------|------|------|------|
| tTLH | Output Rise Time Measured at 10%–90% @ 5 VDC | 1.8 | 2.2 | 2.7 | ns |
| tTHL | Output Fall Time Measured at 10%–90% @ 5 VDC | 1.5 | 2.0 | 2.5 | ns |
| tTLH | Output Rise Time Measured at 0.8V–2.0V @ 5 VDC | 0.5 | 0.65 | 0.8 | ns |
| tTHL | Output Fall Time Measured at 0.8V–2.0 V @ 5 VDC | 0.5 | 0.65 | 0.8 | ns |
| tTLH | Output Rise Time Measured at 10%–90% @ 3.3 VDC | 2.1 | 2.65 | 3.2 | ns |
| tTHL | Output Fall Time Measured at 10%–90% @ 3.3 VDC | 1.7 | 2.1 | 2.6 | ns |
| tTLH | Output Rise Time Measured at 0.8V–2.0V @ 3.3 VDC | 0.7 | 0.95 | 1.2 | ns |
| tTHL | Output Fall Time Measured at 0.8V–2.0 V @ 3.3 VDC | 0.6 | 0.85 | 1.1 | ns |
| TsymF1 | Output Duty Cycle | 45 | 50 | 55 | % |

Notes:

6. **Single Power Supply:** The Voltage on any input or /O pin cannot exceed the power pin during power-up.
7. Percentage variations from the bandwidth % values given in *Table 2* and *Table 3*.

Table 7. Timing Electrical Characteristics $V_{DD} = 3.3V$ and $5.0V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$, $C_L = 15$ pF, $X_{IN} = 48$ MHz (continued)

| Parameter | Description | Min. | Typ. | Max. | Unit |
|-----------|---------------------------------------------------------|------|------|------|------|
| CCJ | FSOUT, Cycle-to-Cycle Jitter, 48 MHz @ 3.30 VDC (Pin 6) | – | 320 | 370 | ps |
| CCJ | FSOUT, Cycle-to-Cycle Jitter, 48 MHz @ 5.0 VDC (Pin 6) | – | 310 | 360 | ps |
| CCJ | FSOUT, Cycle-to-Cycle Jitter, 72 MHz @ 3.30 VDC (Pin 6) | – | 270 | 325 | ps |
| CCJ | FSOUT, Cycle-to-Cycle Jitter, 72 MHz @ 5.0 VDC (Pin 6) | – | 390 | 440 | ps |

Table 8. Range Selection Table

| S1 (pin 3) | S0 (pin 7) | Fin (MHz) (pin 2/3) | Modulation Rate | FS781 FSOUT (pin 6) | FS782 FSOUT (pin 6) | FS784 FSOUT (pin 6) |
|------------|------------|---------------------|-----------------|---------------------|---------------------|---------------------|
| 0 | 0 | 6–16 | Fin/120 | 6–16 MHz | 12–32 MHz | 32–64 MHz |
| 0 | 1 | 16–32 | Fin/240 | 16–32 MHz | 32–64 MHz | 64–82 MHz |
| 1 | 0 | 32–66 | Fin/480 | 32–66 MHz | 64–82 MHz | N/A |
| 1 | 1 | 66–82 | Fin/720 | 66–82 MHz | N/A | N/A |

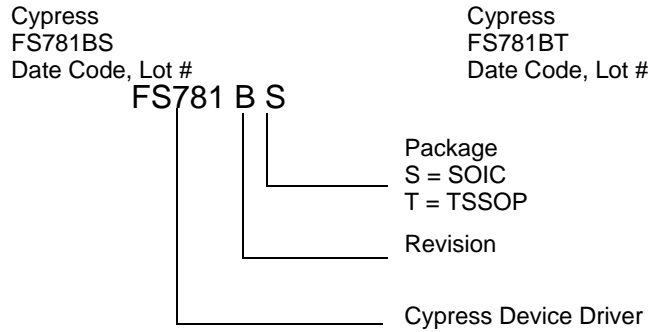
Ordering Information^[8]

| Part Number | Package Type | Product Flow |
|------------------|-------------------------------------------|-----------------------|
| IMIFS781BZB | 8-pin 150-mil SOIC | Commercial, 0 to 70°C |
| IMIFS781BZBT | 8-pin 150-mil SOIC – Tape and Reel | Commercial, 0 to 70°C |
| IMIFS782BZB | 8-pin 150-mil SOIC | Commercial, 0 to 70°C |
| IMIFS782BZBT | 8-pin 150-mil SOIC – Tape and Reel | Commercial, 0 to 70°C |
| IMIFS784BZB | 8-pin 150-mil SOIC | Commercial, 0 to 70°C |
| IMIFS784BZBT | 8-pin 150-mil SOIC – Tape and Reel | Commercial, 0 to 70°C |
| IMIFS781BT | 8-pin (4.4 mm body) TSSOP | Commercial, 0 to 70°C |
| IMIFS781BTT | 8-pin (4.4 mm body) TSSOP – Tape and Reel | Commercial, 0 to 70°C |
| IMIFS784BT | 8-pin (4.4 mm body) TSSOP | Commercial, 0 to 70°C |
| IMIFS784BTT | 8-pin (4.4 mm body) TSSOP – Tape and Reel | Commercial, 0 to 70°C |
| Lead-free | | |
| CYIFS781BSXC | 8-pin 150-mil SOIC | Commercial, 0 to 70°C |
| CYIFS781BSXCT | 8-pin 150-mil SOIC – Tape and Reel | Commercial, 0 to 70°C |
| CYIFS782BSXC | 8-pin 150-mil SOIC | Commercial, 0 to 70°C |
| CYIFS782BSXCT | 8-pin 150-mil SOIC – Tape and Reel | Commercial, 0 to 70°C |
| CYIFS784BSXC | 8-pin 150-mil SOIC | Commercial, 0 to 70°C |
| CYIFS784BSXCT | 8-pin 150-mil SOIC – Tape and Reel | Commercial, 0 to 70°C |
| CYIFS781BZXC | 8-pin (4.4 mm body) TSSOP | Commercial, 0 to 70°C |
| CYIFS781BZXCT | 8-pin (4.4 mm body) TSSOP – Tape and Reel | Commercial, 0 to 70°C |
| CYIFS782BZXC | 8-pin (4.4 mm body) TSSOP | Commercial, 0 to 70°C |
| CYIFS782BZXCT | 8-pin (4.4 mm body) TSSOP – Tape and Reel | Commercial, 0 to 70°C |
| CYIFS784BZXC | 8-pin (4.4 mm body) TSSOP | Commercial, 0 to 70°C |
| CYIFS784BZXCT | 8-pin (4.4 mm body) TSSOP – Tape and Reel | Commercial, 0 to 70°C |

Note:

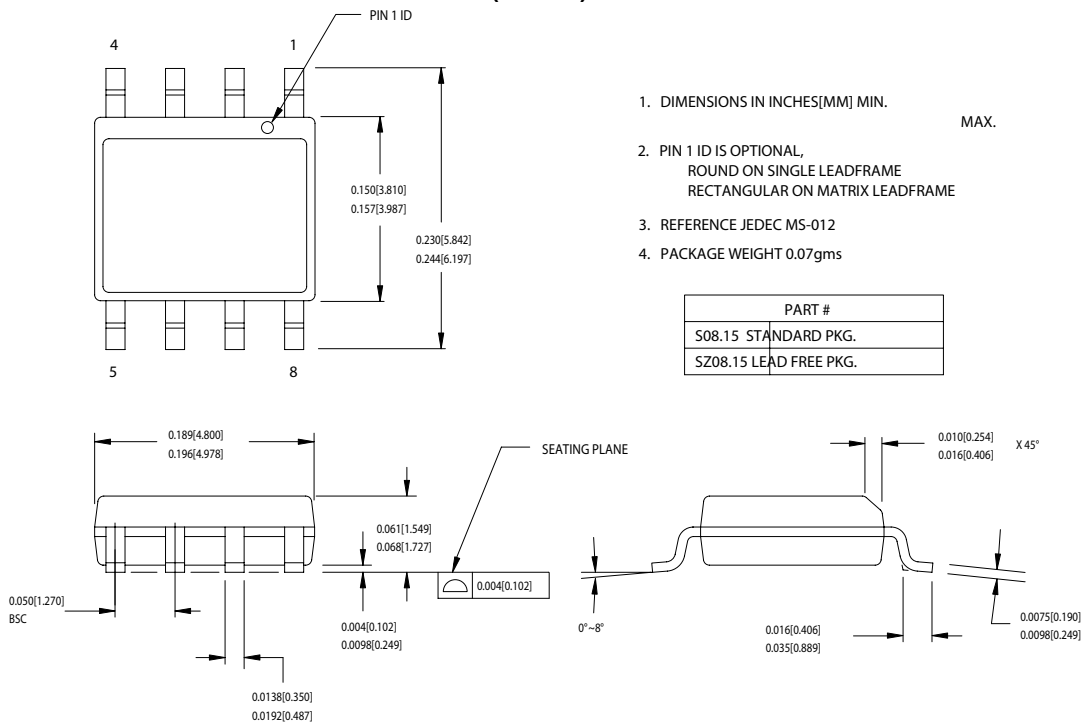
8. The ordering part number differs from the marking on the actual device.

Marking Example



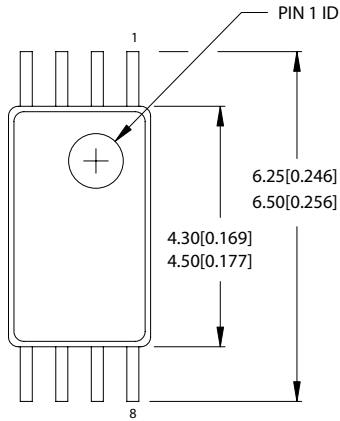
Package Drawing and Dimensions

8-lead (150-Mil) SOIC S8

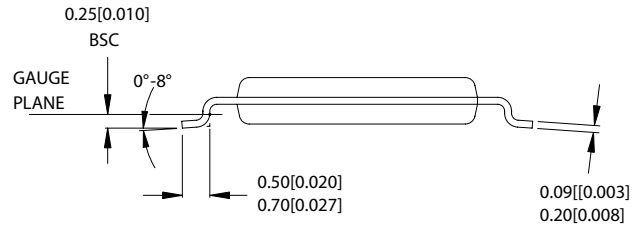
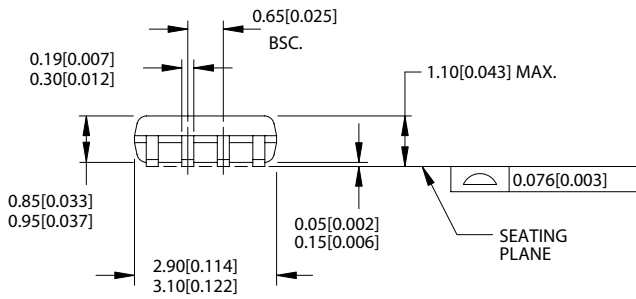


Package Drawing and Dimensions (continued)

8-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z8



DIMENSIONS IN MM[INCHES] MIN.
MAX.



51-85093-*A

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Document History Page

| Document Title: FS781/82/84 Low EMI Spectrum Spread Clock | | | | |
|-----------------------------------------------------------|---------|------------|-----------------|----------------------------------------------------------------------|
| Document Number: 38-07029 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 106948 | 06/07/01 | IKA | Convert from IMI to Cypress |
| *A | 111654 | 02/27/02 | IKL | Add new marking suffix for SOIC packages. Converted to FrameMaker. |
| *B | 118355 | 08/30/02 | RGL | Swap the location of S0 and S1 in tables 2 and 3 in pages 2,3 and 4. |
| *C | 122679 | 12/14/02 | RBI | Add power up requirements to operating conditions information. |
| *D | 277189 | See ECN | RGL | Added Lead-free Devices |
| *E | 314274 | See ECN | RGL | Fixed the Ordering Information to match the DevMaster |
| *F | 417662 | See ECN | RGL | Added Maximum Junction Temperature in Absolute Maximum Ratings table |