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PERICOM®

Low-Noise, Phase-Locked Loop Clock Driver with 10 Clock Outputs

Features

- Operating Frequency up to 150 MHz
- Low-Noise Phase-Locked Loop Clock Distribution that meets 133 MHz Registered DIMM Synchronous DRAM modules for server/workstation/PC applications
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-Output delay: Distribute one Clock Input to one Bank of Ten outputs, with an output enable.
- Low jitter: Cycle-to-Cycle jitter ±75ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Packaging(Pb-free & Green available):
 - 24-pin TSSOP(L)

Description

The PI6C2510-133 is a "quiet," low-skew, low-jitter, phase-locked loop (PLL) clock driver, distributing high-frequency clock signals for SDRAM and server applications. By connecting the feedback FB_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero. This zero-delay feature allows the CLK_IN input clock to be distributed, providing one clock input to one bank of ten outputs, with an output enable.

This clock driver is designed to meet the PC133 SDRAM Registered DIMM specification. For test purposes, the PLL can be bypassed by strapping AV_{CC} to ground.

Block Diagram
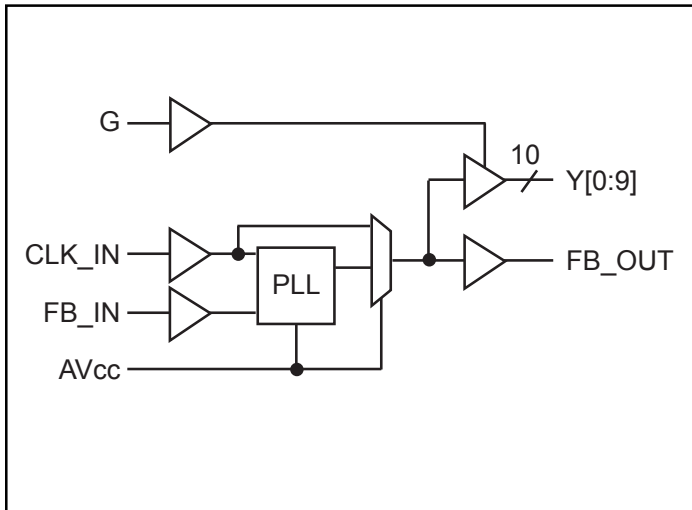
Pin Configuration
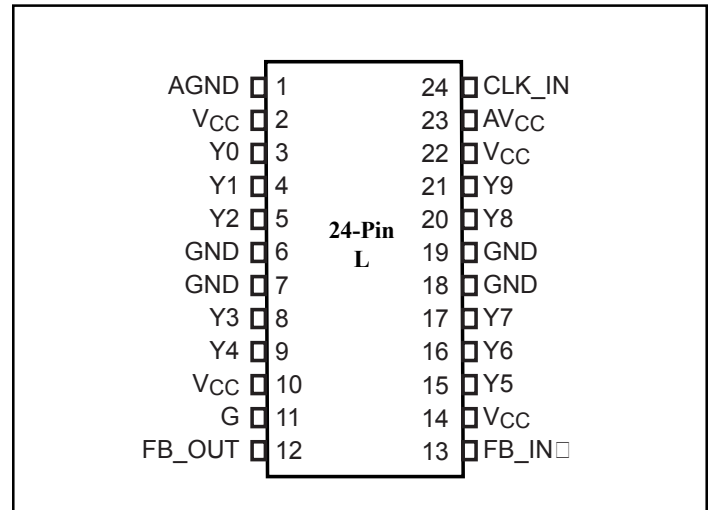
Functional Table

Inputs	Outputs	
G	**Y[0:9]**	**FB_OUT**
L	L	CLK_IN
H	CLK_IN	CLK_IN

Pin Functions

Pin Name	Pin Number	Type	Description
CLK_IN	24	I	Reference Clock input. CLK_IN allows spread spectrum.
FB_IN	13	I	Feedback input. FB_IN provides the feedback signal to the internal PLL
G	11	I	Output bank enable. When G is LOW, outputs Y[0:9] are disabled to a logic low state. When G is HIGH, all outputs Y[0:9] are enabled.
FB_OUT	12	O	Feedback output. FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs Y[0:9].
Y[0:9]	3,4,5,8,9,15 16,17,20,21	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded series-damping resistor.
AV_{CC}	23	Power	Analog power supply. AV_{CC} can be also used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK_IN buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	2,10,14,22	Power	Power supply
GND	6,7,18,19	Ground	Ground

DC Specifications

Absolute maximum ratings over operating free-air temperature range.

Symbol	Parameter	Min.	Max.	Units
V_I	Input voltage range	-0.5	V_{CC}+ 0.5	V
V_O	Output voltage range			
V_I_DC	DC input voltage		+5.0	
I_O_DC	DC output current		100	mA
Power	Maximum power dissipation at $T_A = 55^oC$ in still air		1.0	W
T_{STG}	Storage temperature	-65	150	^oC

Note: Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

Parameter	Test Conditions	V_{CC}	Min.	Typ.	Max.	Units
I_{CC}	$V_I = V_{CC}$ or GND; $I_O = 0$	3.6V			10	μA
C_I	$V_I = V_{CC}$ or GND	3.3V		4		pF
C_O	$V_O=V_{CC}$ or GND			6		

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply voltage	3.0	3.6	V
V_{IH}	High level input voltage	2.0		
V_{IL}	Low level input voltage		0.8	
V_I	Input voltage	0.0	V_{CC}	
T_A	Operating free-air temperature	0	70	^oC

Electrical characteristics over recommended operating free-air temperature range

Pull Up/Down Currents of PI6C2510-133, $V_{CC} = 3.0V$

Symbol	Parameter	Condition	Min.	Max.	Units
I_{OH}	Pull-up current	$V_{OUT} = 2.4V$		-13.6	mA
	Pull-up current	$V_{OUT} = 2.0V$		-22	
I_{OL}	Pull-down current	$V_{OUT} = 0.8V$	19		
	Pull-down current	$V_{OUT} = 0.55V$	13		

AC Specifications

**Timing requirements over recommended ranges of supply voltage and operating free-air temperature.**

Symbol	Parameter	Min.	Max.	Units
F_{CLK}	Input clock frequency	25	150	MHz
	Input clock duty cycle	40	60	%
	Stabilization Time after power up		1	ms

Switching characteristics over recommended ranges of supply voltage and operating free-air temperature, CL=30pF

Parameter	From	To	V_{CC}= 3.3V ±0.3V, 0-70°C			Units
			Min.	Typ.	Max.	
tphase error, with and without spread spectrum	CLK_IN↑ at 133 MHz	FB_IN↑	−150		+150	ps
Jitter, cycle-to-cycle, with and without spread spectrum	Any Output or FB_OUT in CLK_n at 133 MHz	Output or FB_OUT in CLK_{n+1}	−75		+75	
Skew, at 133 MHz	Any Y or FB_OUT	Any Y or FB_OUT			150	
Duty cycle			45	50	55	%
tr, rise-time, 0.4V to 2.0V				1.0		ns
tf, fall-time, 2.0V to 0.4V				1.1		

Note: These switching parameters are guaranteed, but not production tested.

Packaging Mechanical: 24-pin TSSOP (L)
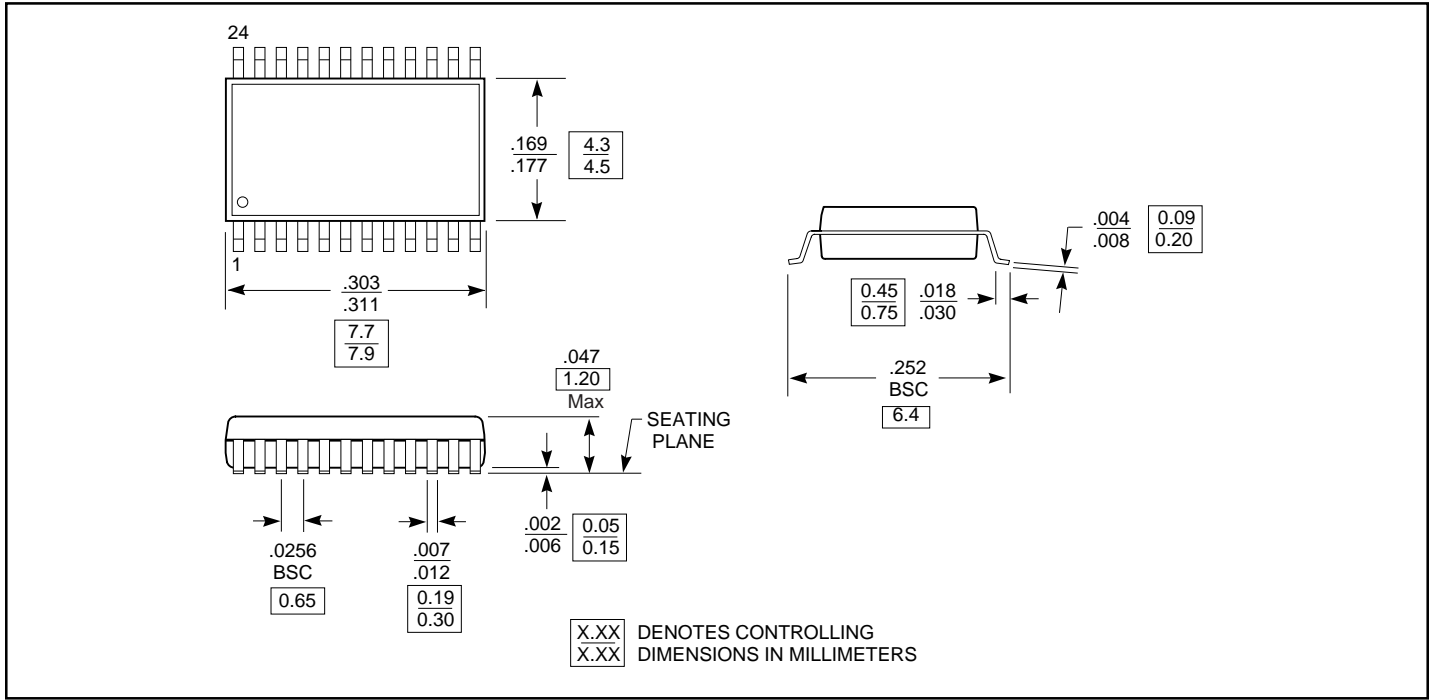
Ordering Information

Ordering Code	Package Code	Package Type
PI6C2510-133L	L	24-pin TSSOP
PI6C2510-133LE	L	Pb-free & Green, 24-pin TSSOP

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/