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CY22050, CY220501

One-PLL General Purpose Flash Programmable Clock Generator

Features

- Integrated phase-locked loop (PLL)
- Commercial and Industrial operation
- Flash-programmable
- Field-programmable
- Low-skew, low-jitter, high-accuracy outputs
- 3.3V operation with 2.5V output option
- 16-Pin TSSOP package (CY22050)
- 16-Pin TSSOP package with NiPdAu lead finish (CY220501)

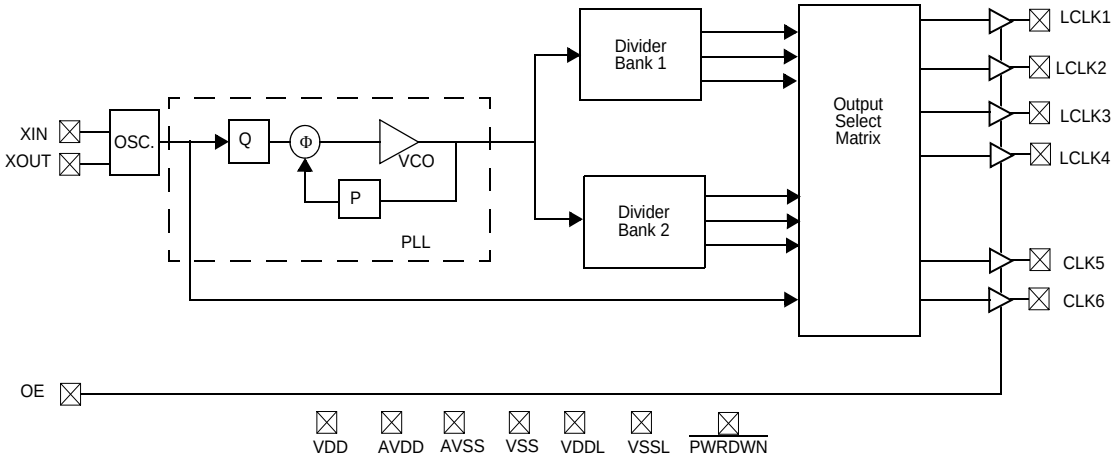
Benefits

- Internal PLL to generate six outputs up to 200 MHz. Able to generate custom frequencies from an external reference crystal or driven source.
- Performance guaranteed for applications that require an extended temperature range.
- Reprogrammable technology allows easy customization, quick turnaround on design changes and product performance enhancements, and better inventory control. Parts can be reprogrammed up to 100 times, reducing inventory of custom parts and providing an easy method for upgrading existing designs.
- In-house programming of samples and prototype quantities is available using the CY3672 FTG Development Kit. Production quantities are available through Cypress's value-added distribution partners or by using third party programmers from BP Microsystems, HiLo Systems, and others.
- Industry standard packaging saves on board space.

Table 1. Device Selection

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifications
CY22050KFZXC	6	8 MHz–30 MHz (external crystal) 1 MHz–133 MHz (driven clock)	80 kHz–200 MHz (3.3V) 80 KHz–166.6 MHz (2.5V)	Field-programmable commercial temperature
CY22050KFZXI	6	8 MHz–30 MHz (external crystal) 1 MHz–133 MHz (driven clock)	80 kHz–166.6 MHz (3.3V) 80 KHz–150 MHz (2.5V)	Field-programmable industrial temperature
CY220501KFZXI	6	8 MHz–30 MHz (external crystal) 1 MHz–133 MHz (driven clock)	80 kHz–166.6 MHz (3.3V) 80 KHz–150 MHz (2.5V)	Field-programmable industrial temperature NiPdAu lead finish

Logic Block Diagram



Pin Configuration

Figure 1. 16-Pin TSSOP

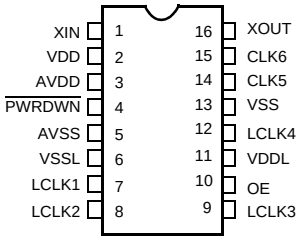


Table 2. Pin Definitions

Name	Pin Number	Description
XIN	1	Reference Input. Driven by a crystal (8 MHz–30 MHz) or external clock (1 MHz–133 MHz). Programmable input load capacitors allow for maximum flexibility in selecting a crystal, based on manufacturer, process, performance, or quality.
VDD	2	3.3V voltage supply
AVDD	3	3.3V analog voltage supply
PWRDWN[1]	4	Power Down. When pin 4 is driven LOW, the CY22050 goes into shut down mode.
AVSS	5	Analog ground
VSSL	6	LCLK ground
LCLK1	7	Configurable clock output 1 at V_{DDL} level (3.3V or 2.5V)
LCLK2	8	Configurable clock output 2 at V_{DDL} level (3.3V or 2.5V)
LCLK3	9	Configurable clock output 3 at V_{DDL} level (3.3V or 2.5V)
OE[1]	10	Output Enable. When pin 10 is driven LOW, all outputs are three-stated.
VDDL	11	LCLK voltage supply (2.5V or 3.3V)
LCLK4	12	Configurable clock output 4 at V_{DDL} level (3.3V or 2.5V)
VSS	13	Ground
CLK5	14	Configurable clock output 5 (3.3V)
CLK6	15	Configurable clock output 6 (3.3V)
XOUT[2]	16	Reference output

Notes
1. The CY22050 has no internal pull up or pull down resistors. $\overline{\text{PWRDWN}}$ and OE pins need to be driven as appropriate or tied to power or ground.
2. Float XOUT if XIN is driven by an external clock source.

Functional Description

The CY22050 is the next-generation programmable FTG (frequency timing generator) for use in networking, telecommunication, datacom, and other general-purpose applications. The CY22050 offers up to six configurable outputs in a 16-pin TSSOP, running off a 3.3V power supply. The on-chip reference oscillator is designed to run off an 8–30-MHz crystal, or a 1–133-MHz external clock signal.

The CY22050 has a single PLL driving 6 programmable output clocks. The output clocks are derived from the PLL or the reference frequency (REF). Output post dividers are available for either. Four of the outputs can be set as 3.3V or 2.5V, for use in a wide variety of portable and low-power applications.

The CY220501 is the CY22050 with NiPdAu lead finish.

Field Programming the CY22050F

The CY22050 is programmed at the package level, that is, in a programmer socket, prior to installation on a PCB. The CY22050 is flash-technology based, so the parts can be reprogrammed up to 100 times. This allows for fast and easy design changes and product updates, and eliminates any issues with old and out-of-date inventory.

Samples and small prototype quantities can be programmed on the CY3672 programmer. Cypress's value-added distribution partners and third-party programming systems from BP Microsystems, HiLo Systems, and others are available for large-production quantities.

CyberClocks™ Software

CyberClocks is an easy-to-use software application that allows the user to custom-configure the CY22050. Within CyberClocks, select the CyClocksRT™ tool. Users can specify the REF, PLL frequency, output frequencies and/or post-dividers, and different functional options. CyClocksRT outputs an industry-standard JEDEC file used for programming the CY22050.

CyClocksRT can be downloaded free of charge from the Cypress website at http://www.cypress.com. Install and run it on any PC running the Windows operating system.

CY3672 Development Kit

The Cypress CY3672 Development Kit comes complete with everything needed to design with the CY22050 and program samples and small prototype quantities. The kit comes with the latest version of CyClocksRT and a small portable programmer that connects to a PC for on-the-fly programming of custom frequencies.

The JEDEC file output of CyClocksRT can be downloaded to the portable programmer for small-volume programming, or for use with a production programming system for larger volumes.

Applications

Controlling Jitter

Jitter is defined in many ways, including: phase noise, long-term jitter, cycle-to-cycle jitter, period jitter, absolute jitter, and deterministic jitter. These jitter terms are usually given in terms of rms, peak-to-peak, or in the case of phase noise dBC/Hz with respect to the fundamental frequency. Actual jitter is dependent on XIN jitter and edge rate, number of active outputs, output frequencies, V_{DDL} (2.5V or 3.3V), temperature, and output load.

Power supply noise and clock output loading are two major system sources of clock jitter. Power supply noise can be mitigated by proper power supply decoupling (0.1-μF ceramic cap) of the clock and ensuring a low-impedance ground to the chip. Reducing capacitive clock output loading to a minimum lowers current spikes on the clock edges and thus reduces jitter.

Reducing the total number of active outputs also reduce jitter in a linear fashion. However, it is better to use two outputs to drive two loads than one output to drive two loads.

The rate and magnitude that the PLL corrects the VCO frequency is directly related to jitter performance. If the rate is too slow, then long term jitter and phase noise is poor. Therefore, to improve long-term jitter and phase noise, reducing Q to a minimum is advisable. This technique increases the speed of the phase frequency detector, which in turn drives the input voltage of the VCO. In a similar manner, increasing P until the VCO is near its maximum rated speed also decreases long term jitter and phase noise. For example: input reference of 12 MHz; desired output frequency of 33.3 MHz. One might arrive at the following solution: Set Q = 3, P = 25, Post Div = 3. However, the best jitter results are Q = 2, P = 50, Post Div = 9.

For additional information, refer to the application note, "Jitter in PLL-based Systems: Causes, Effects, and Solutions," available at http://www.cypress.com (click on "Application Notes"), or contact your local Cypress Field Applications Engineer.

CY22050 Frequency Calculation

The CY22050 is an extremely flexible clock generator with up to six individual outputs, generated from an integrated PLL.

There are four variables used to determine the final output frequency. They are: the input REF, the P and Q dividers, and the post divider. The three basic formulas for determining the final output frequency of a CY22150-based design are:

- CLK = ((REF * P)/Q)/Post Divider
- CLK = REF/Post Divider
- CLK = REF

The basic PLL block diagram is shown in Figure 2. Each of the six clock outputs has a total of seven output options available to it. There are six post divider options: /2 (two of these), /3, /4, /DIV1N, and DIV2N. DIV1N and DIV2N are separately calculated and can be independent of each other. The post divider options can be applied to the calculated PLL frequency or to the REF directly.

In addition to the six post divider options, the seventh option bypasses the PLL and passes the REF directly to the crosspoint switch matrix.

Clock Output Settings: Crosspoint Switch Matrix

Each of the six clock outputs can come from any of seven unique frequency sources. The crosspoint switch matrix defines which source is attached to each individual clock output. Although it may seem that there are an unlimited number of divider options, there are several rules that must be taken into account when selecting divider options.

Figure 2. Basic PLL Block Diagram

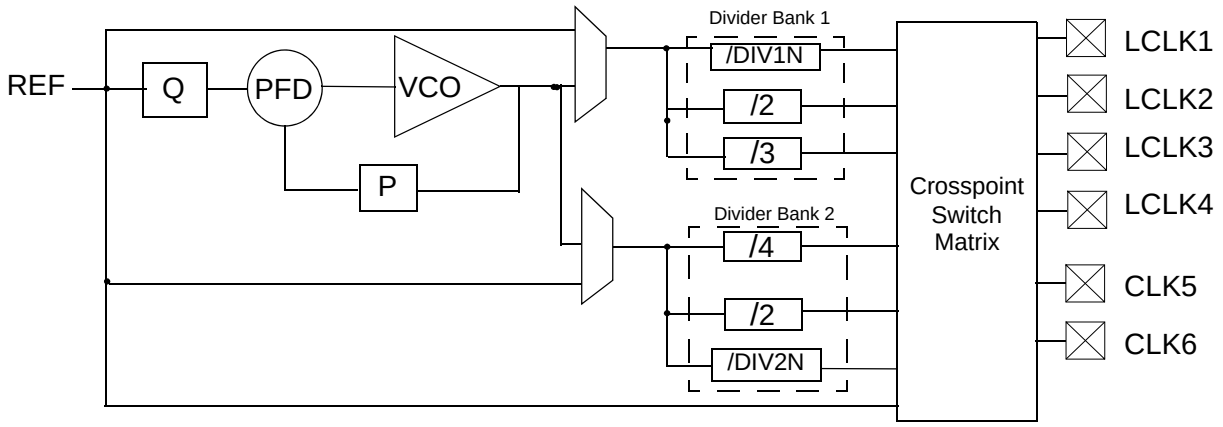


Table 3. Clock Output Definition

Clock Output Divider	Definition and Notes
None	Clock output source is the reference input frequency
/DIV1N	Clock output uses a generated /DIV1N option from Divider Bank 1. Allowable values for DIV1N are 4 to 127. If Divider Bank 1 is not being used, set DIV1N to 8.
/2	Clock output uses a fixed /2 option from Divider Bank 1. If this option is used, DIV1N must be divisible by 4.
/3	Clock output uses a fixed /3 option from Divider Bank 1. If this option is used, set DIV1N to 6.
/DIV2N	Clock output uses a generated /DIV2N option from Divider Bank 2. Allowable values for DIV2N are 4 to 127. If Divider Bank 2 is not being used, set DIV2N to 8.
/2	Clock output uses a fixed /2 option from Divider Bank 2. If this option is used, DIV2N must be divisible by 4.
/4	Clock output 2 uses a fixed /4 option from Divider Bank 2. If this option is used, DIV2N must be divisible by 8.

Reference Crystal Input

The input crystal oscillator of the CY22050 is an important feature because of the flexibility it allows the user in selecting a crystal as a reference clock source. The oscillator inverter has programmable gain, allowing for maximum compatibility with a reference crystal, based on manufacturer, process, performance, and quality.

The value of the input load capacitors is determined by eight bits in a programmable register. Total load capacitance is determined by the formula:

$$CapLoad = (C_L - C_{BRD} - C_{CHIP})/0.09375\ pF$$

In CyClocksRT, enter the crystal capacitance (C_L). The value of CapLoad is determined automatically and programmed into the CY22050.

If you require greater control over the CapLoad value, consider using the CY22150 for serial configuration and control of the input load capacitors. For an external clock source, the default is 0.

Input load capacitors are placed on the CY22050 die to reduce external component cost. These capacitors are true parallel-plate capacitors, designed to reduce the frequency shift that occurs when non-linear load capacitance is affected by load, bias, supply, and temperature changes.

Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
V_{DDL}	I/O Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature[3]	–65	125	°C
T_J	Junction Temperature		125	°C
	Package Power Dissipation—Commercial Temp		450	mW
	Package Power Dissipation—Industrial Temp		380	mW
	Digital Inputs	AV_{SS} – 0.3	AV_{DD} + 0.3	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs referred to V_{DDL}	V_{SS} – 0.3	V_{DDL} +0.3	V
ESD	Static Discharge Voltage per MIL-STD-833, Method 3015		2000	V

Recommended Operating Conditions

Parameter	Description	Min	Typ.	Max	Unit
V_{DD}	Operating Voltage	3.135	3.3	3.465	V
$VDDL_{HI}$	Operating Voltage	3.135	3.3	3.465	V
$VDDL_{LO}$	Operating Voltage	2.375	2.5	2.625	V
T_{AC}	Ambient Commercial Temp	0		70	°C
T_{AI}	Ambient Industrial Temp	–40		85	°C
C_{LOAD}	Max. Load Capacitance V_{DD}/V_{DDL} = 3.3V			15	pF
C_{LOAD}	Max. Load Capacitance V_{DDL} = 2.5V			15	pF
f_{REFD}	Driven REF	1		133	MHz
f_{REFC}	Crystal REF	8		30	MHz
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

Note
3. Rated for 10 years

DC Electrical Characteristics

Parameter[4]	Name	Description	Min	Typ.	Max	Unit
$I_{OH3.3}$	Output High Current	$V_{OH} = V_{DD} – 0.5V$, $V_{DD}/V_{DDL} = 3.3V$	12	24		mA
$I_{OL3.3}$	Output Low Current	$V_{OL} = 0.5V$, $V_{DD}/V_{DDL} = 3.3V$	12	24		mA
$I_{OH2.5}$	Output High Current	$V_{OH} = V_{DDL} – 0.5V$, $V_{DDL} = 2.5V$	8	16		mA
$I_{OL2.5}$	Output Low Current	$V_{OL} = 0.5V$, $V_{DDL} = 2.5V$	8	16		mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7		1.0	V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	0		0.3	V_{DD}
I_{VDD}[5,6]	Supply Current	AV_{DD}/V_{DD} Current		45		mA
$I_{VDDL3.3}$[5,6]	Supply Current	V_{DDL} Current ($V_{DDL} = 3.465V$)		25		mA
$I_{VDDL2.5}$[5,6]	Supply Current	V_{DDL} Current ($V_{DDL} = 2.625V$)		17		mA
I_{DDS}	Power Down Current	$V_{DD} = V_{DDL} = AV_{DD} = 3.465V$			50	µA
I_{OHZ} I_{OLZ}	Output Leakage	$V_{DD} = V_{DDL} = AV_{DD} = 3.465V$			10	µA

AC Electrical Characteristics

Parameter[4]	Name	Description	Min	Typ.	Max	Unit
t1	Output frequency, commercial temp	Clock output limit, 3.3V	0.08 (80 kHz)		200	MHz
		Clock output limit, 2.5V	0.08 (80 kHz)		166.6	MHz
	Output frequency, industrial temp	Clock output limit, 3.3V	0.08 (80 kHz)		166.6	MHz
		Clock output limit, 2.5V	0.08 (80 kHz)		150	MHz
t2	Output duty cycle	Duty cycle is defined in Figure 4; t1/t2 $f_{OUT} > 166$ MHz, 50% of V_{DD}	40	50	60	%
		Duty cycle is defined in Figure 4; t1/t2 $f_{OUT} < 166$ MHz, 50% of V_{DD}	45	50	55	%
$t3_{LO}$	Rising edge slew rate ($V_{DDL} = 2.5V$)	Output clock rise time, 20% – 80% of V_{DDL}. Defined in Figure 5	0.6	1.2		V/ns
$t4_{LO}$	Falling edge slew rate ($V_{DDL} = 2.5V$)	Output clock fall time, 80% – 20% of V_{DDL}. Defined in Figure 5	0.6	1.2		V/ns
$t3_{HI}$	Rising edge slew rate ($V_{DDL} = 3.3V$)	Output clock rise time, 20% – 80% of V_{DD}/V_{DDL}. Defined in Figure 5	0.8	1.4		V/ns
$t4_{HI}$	Falling edge slew rate ($V_{DDL} = 3.3V$)	Output clock fall time, 80% – 20% of V_{DD}/V_{DDL}. Defined in Figure 5	0.8	1.4		V/ns
t5[7]	Skew	Output-output skew between related outputs			250	ps
t6[8]	Clock jitter	Peak-to-peak period jitter (see Figure 6)		250		ps
t10	PLL lock time			0.30	3	ms

Notes
4. Not 100% tested, guaranteed by design.
5. IVDD currents specified for two CLK outputs running at 125 MHz, two LCLK outputs running at 80 MHz, and two LCLK outputs running at 66.6 MHz. All outputs are loaded with 15pF.
6. Use CyClocksRT to calculate actual IVDD and IVDDL for specific output frequency configurations.
7. Skew value guaranteed when outputs are generated from the same divider bank. See Logic Block Diagram for more information.
8. Jitter measurement will vary. Actual jitter is dependent on XIN jitter and edge rate, number of active outputs, output frequencies, VDDL (2.5V or 3.3V), temperature, and output load. For more information, refer to the application note, “Jitter in PLL-based Systems: Causes, Effects, and Solutions,” available at http://www.cypress.com, or contact your local Cypress Field Applications Engineer.

Figure 3. Test Circuit

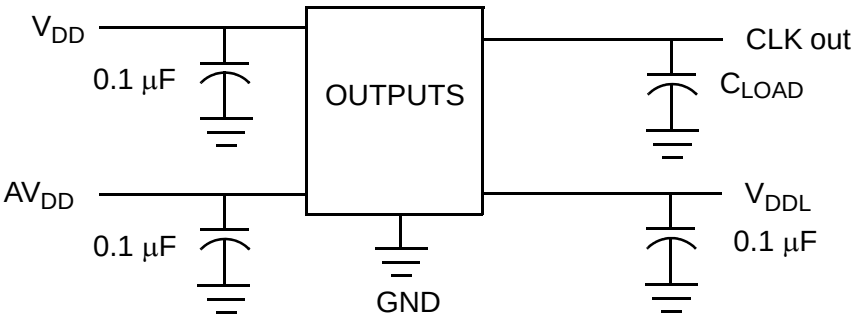


Figure 4. Duty Cycle Definition: DC = t2/t1

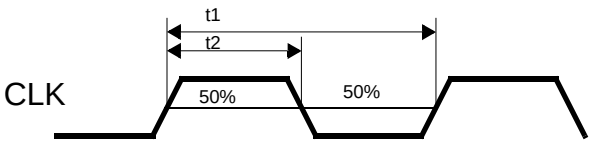


Figure 5. Rise and Fall Time Definitions

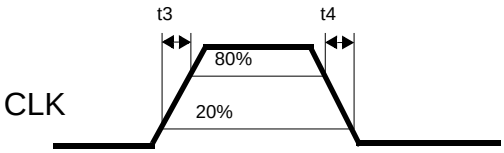
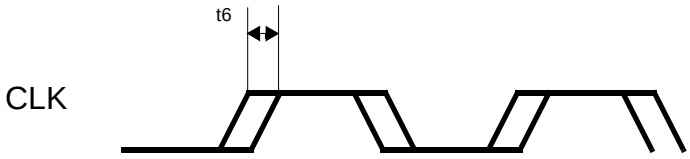


Figure 6. Peak-to-Peak Jitter



Ordering Information

Ordering Code	Package Type	Temperature Operating Range	Operating Voltage
CY22050FC[9]	16-lead TSSOP	Commercial (0 to 70°C)	3.3V
CY22050FI[9]	16-lead TSSOP	Industrial (–40 to 85°C)	3.3V
CY22050ZC-xxx[9, 10]	16-lead TSSOP	Commercial (0 to 70°C)	3.3V
CY22050KFC	16-lead TSSOP	Commercial (0 to 70°C)	3.3V
CY22050KFI	16-lead TSSOP	Industrial (–40 to 85°C)	3.3V
Pb-Free			
CY220501KFZXI	16-lead TSSOP with NiPdAu lead finish	Industrial (–40 to 85°C)	3.3V
CY22050FZXC[9]	16-lead TSSOP	Commercial (0 to 70°C)	3.3V
CY22050FZXI[9]	16-lead TSSOP	Industrial (–40 to 85°C)	3.3V
CY22050ZXC-xxx[9, 10]	16-lead TSSOP	Commercial (0 to 70°C)	3.3V
CY22050ZXC-xxxT[9, 10]	16-lead TSSOP-Tape and Reel	Commercial (0 to 70°C)	3.3V
CY22050ZXI-xxx[9, 10]	16-lead TSSOP	Industrial (–40 to 85°C)	3.3V
CY22050ZXI-xxxT[9, 10]	16-lead TSSOP-Tape and Reel	Industrial (–40 to 85°C)	3.3V
CY22050KFZXC	16-lead TSSOP	Commercial (0 to 70°C)	3.3V
CY22050KFZXI	16-lead TSSOP	Industrial (–40 to 85°C)	3.3V
CY22050KZXC-xxx[10]	16-lead TSSOP	Commercial (0 to 70°C)	3.3V
CY22050KZXC-xxxT[10]	16-lead TSSOP-Tape and Reel	Commercial (0 to 70°C)	3.3V
CY22050KZXI-xxx[10]	16-lead TSSOP	Industrial (–40 to 85°C)	3.3V
CY22050KZXI-xxxT[10]	16-lead TSSOP-Tape and Reel	Industrial (–40 to 85°C)	3.3V
Programmer			
CY3672-USB	Programming Kit		
CY3695	CY22050F, CY22050KFand CY220501KF Adapter for CY3672 Programmer		

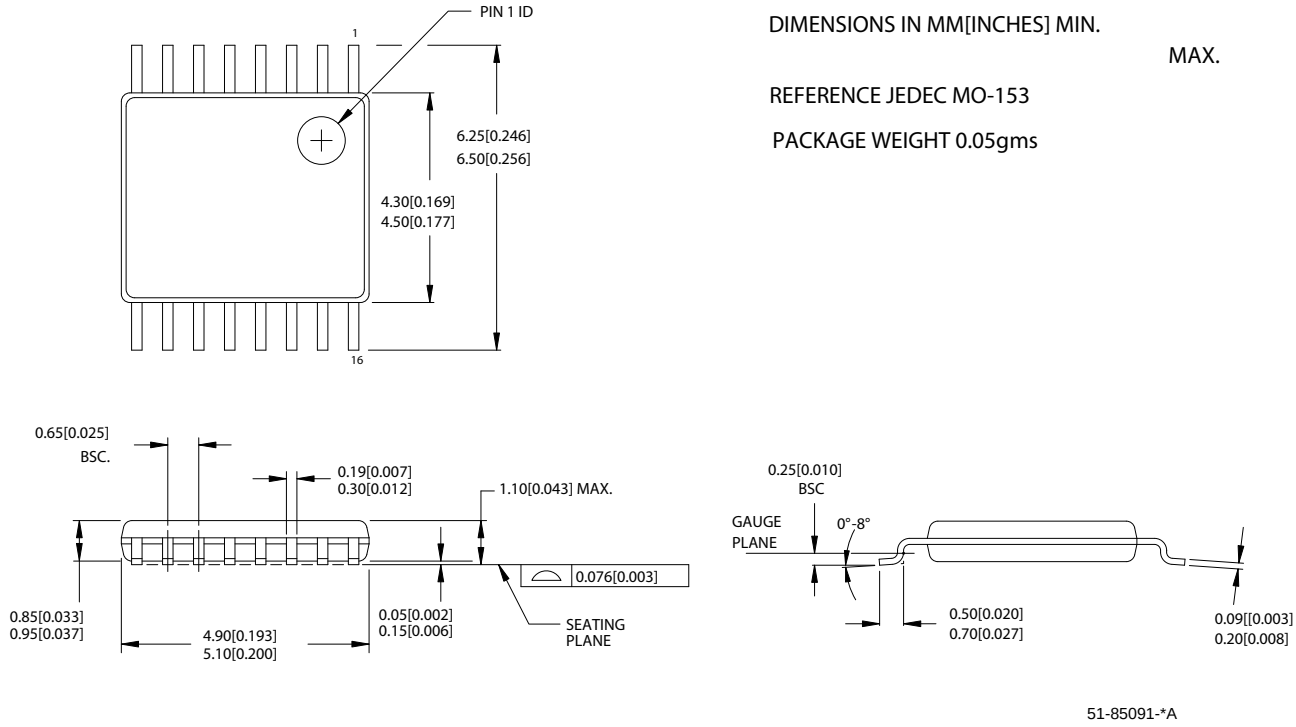
16-Pin TSSOP Package Characteristics

Parameter	Name	Value	Unit
θ_{JA}	theta JA	115	°C/W
Complexity	Transistor Count	74,600	Transistors

Notes
9. Not recommended for new designs. Part numbers without a “K” are being replaced by part numbers with a “K”. There are no changes to device specifications as a result of the part number change.
10. The CY22050KZXC-xxx and CY22050KZXI-xxx are factory-programmed configurations. Factory programming is available for high-volume design opportunities of 100 Ku/year or more in production. For more details, contact your local Cypress field application engineer or Cypress sales representative.

Package Drawing and Dimensions

Figure 7. 16-Pin TSSOP 4.40 MM Body Z16.173



Document History Page

Document Title: CY22050, CY220501 One-PLL General Purpose Flash-Programmable Clock Generator Document Number: 38-07006				
REV.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	108185	CKN	08/08/01	New Data Sheet.
*A	110054	CKN	03/04/02	Changed from Preliminary to Final.
*B	121862	RBI	12/14/02	Power up requirements added to Operating Conditions Information.
*C	310575	RGL	01/20/05	Added Lead-free devices.
*D	314233	RGL	01/31/05	Removed the Tape and Reel devices in the non-dash parts.
*E	2440826	AESA	05/15/08	Updated template. Added Note “Not recommended for new designs.” and “38-07409, CY3672 PTG Programming Kit”. Corrected "FTG" to PTG" in Ordering information table. Added part numbers CY22050KFC, CY22050KFI, CY22050KFZXC, CY22050KFZXI, CY22050KZXC-xxx, CY22050KZXC-xxxT, CY22050KZXI-xxx, and CY22050KZXI-xxxT in ordering information table. Changed Lead-Free to Pb-Free.
*F	2642064	KVM	01/21/09	Added CY220501 to title. Added CY220501KFZXI to ordering table.
*G	2743347	KVM	07/24/09	Revised the Device Selection table on page 1 and renamed it. Updates to programmer and softwre descriptions. Clarified that I_{VDD} and I_{VDDL} are for loaded outputs. Updated footnotes to show that the standard part numbers are now with a “K”. Changed CY3672 part number to CY3672-USB, changed CY3672ADP000 to CY3695, and repositioned them in the Ordering Information table. Deleted part numbers CY22050ZC-xxxT, CY22050ZI-xxx and CY22050ZI-xxxT.

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