

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

LOW EMI CLOCK GENERATOR

ICS181-01

Description

The ICS181-01 generates a low EMI output clock from a clock or crystal input. The device uses IDT's proprietary mix of analog and digital Phase-Locked Loop (PLL) technology to spread the frequency spectrum of the output, thereby reducing the frequency amplitude peaks by several dB.

The ICS181-01 offers down spread selection of -1.25% and -3.75%. Refer to the MK1714-01/02 for the widest selection of input frequencies and multipliers.

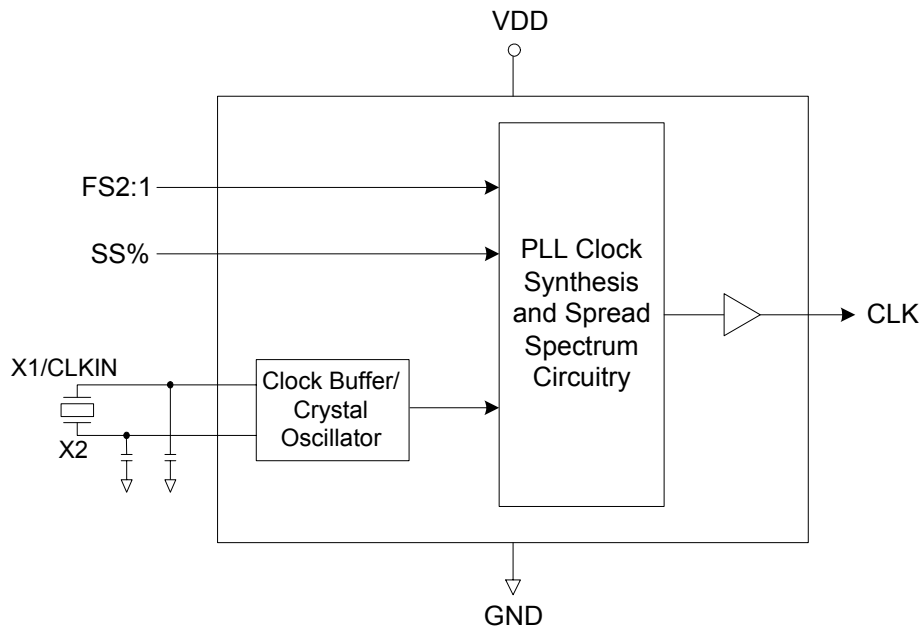
IDT offers a complete line of EMI reducing clock generators. Consult us when you need to remove crystals and oscillators from your board.

Features

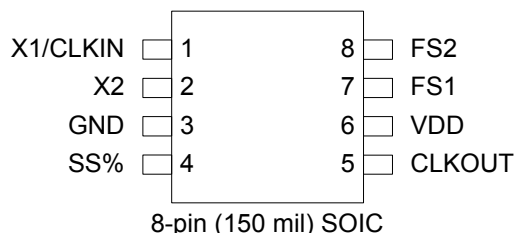
- Pin and function compatible to Cypress W181-01
- Packaged in 8-pin SOIC
- Provides a spread spectrum output clock
- Accepts a clock input and provides same frequency dithered output
- Input frequency of 28 to 75 MHz for Clock input
- Peak reduction by 7dB - 14dB typical on 3rd - 19th odd harmonics
- Spread percentage selection for -1.25% and -3.75%
- Operating voltage of 3.3 V and 5 V
- Available in Pb (lead) free package
- Industrial temperature range available
- Advanced, low-power CMOS process

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



Pin Assignment



Spread Spectrum Select Table

SS% (Pin 4)	Spread Direction	Spread Percentage (%)
0	Down	-1.25%
1	Down	-3.75%

0 = connect to GND

1 = connect directly to VDD

Note: SS% pin has an internal pull-up resistor

Frequency Range Selection Table

FS2 (Pin 8)	FS1 (Pin 7)	Frequency Range Selection (MHz)
0	0	28-38
0	1	38-48
1	0	46-60
1	1	58-75

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/CLKIN	Input	Crystal or Clock input.
2	X2	Output	Crystal output. Float for a clock input.
3	GND	Power	Connect to ground.
4	SS%	Input	Select pin for spread amount. See table above. Internal pull-up resistor.
5	CLKOUT	Output	Spread spectrum clock output per table above.
6	VDD	Power	Connect to 3.3 V or 5 V.
7	FS1	Input	Select pin for input frequency. See table above. Internal pull-up resistor.
8	FS2	Input	Select pin for input frequency. See table above. Internal pull-up resistor.

External Components

The ICS181-01 requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01 μ F must be connected between VDD and GND on pins 6 and 3, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output and the load is over 1 inch, series termination should be used. To series terminate a 50 Ω trace (a commonly used trace impedance) place a 33 Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 Ω

value of these capacitors is given by the following equation:

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

- 1) The 0.01 μ F decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.
- 2) To minimize EMI, the 33 Ω series termination resistor (if needed) should be placed close to the clock output.
- 3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS181-01. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS181-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70° C
Ambient Operating Temperature (industrial)	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.135		+5.5	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ± 5%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Supply Current	IDD	No load, at 3.3 V		18	32	mA
Input High Voltage	V _{IH}		2.4			V
Input Low Voltage	V _{IL}				0.8	V
Output High Voltage	V _{OH}	I _{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V _{OH}	I _{OH} = -15 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 15 mA			0.4	V
Input Capacitance	C _{IN}	All pins except CLKIN		5	7	pF
		CLKIN pin only		6	10	pF
Output Impedance	R _{out}			25		ohms
Input Pull-up Resistor				500		KΩ
Power-up Time		First locked clock cycle after steady power			5	ms

Unless stated otherwise, **VDD = 5 V, ±10%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		4.5	5	5.5	V
Supply Current	IDD	No load, at 3.3 V		30	50	mA
Input High Voltage	V _{IH}		0.7VDD			V
Input Low Voltage	V _{IL}				0.15VDD	V
Output High Voltage	V _{OH}	I _{OH} = -24 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 24 mA			0.4	V
Output Impedance	R _{out}			20		ohms
Input Capacitance	C _{IN}	All pins except CLKIN		5	7	pF
		CLKIN pin only		6	10	pF
Input Pull-up Resistor				500		KΩ
Power-up Time		First locked clock cycle after steady power			5	ms

AC Electrical Characteristics

Unless stated otherwise, $V_{DD} = 3.3\text{ V} \pm 5\%$ or $5\text{ V} \pm 10\%$, Ambient Temperature -40 to $+85^\circ\text{C}$, $C_L = 15\text{ pF}$

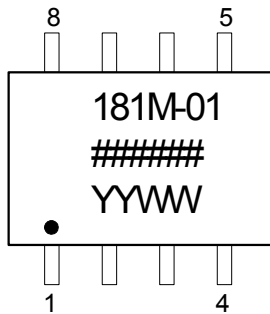
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input/Output Clock Frequency			28		75	MHz
Input Crystal Frequency			28		40	MHz
Input Clock Duty Cycle		Time above $V_{DD}/2$	40		60	%
Output Clock Duty Cycle		Note 1	40	50	60	%
Output Rise Time	t_{OR}	0.8 to 2.4 V, note 1		2	5	ns
Output Fall Time	t_{OF}	2.4 to 0.8 V, note 1		2	5	ns
Jitter		Cycle-to-cycle		250	300	ps

Note 1: Measured with 15 pF load

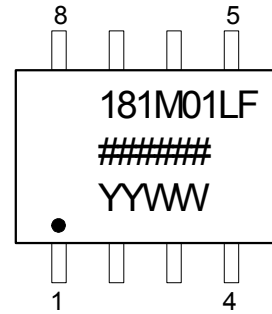
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		$^\circ\text{C/W}$
	θ_{JA}	1 m/s air flow		140		$^\circ\text{C/W}$
	θ_{JA}	3 m/s air flow		120		$^\circ\text{C/W}$
Thermal Resistance Junction to Case	θ_{JC}			40		$^\circ\text{C/W}$

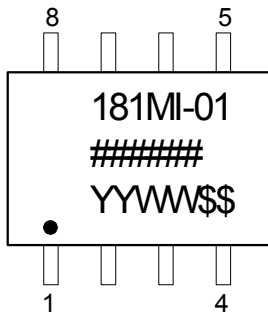
Marking Diagram (ICS181M-01)



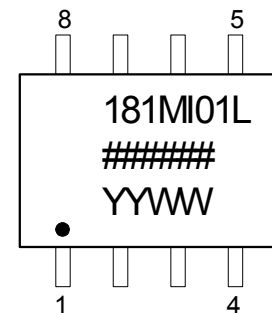
Marking Diagram (ICS181M-01LF)



Marking Diagram (ICS181MI-01)



Marking Diagram (ICS181MI-01LF)

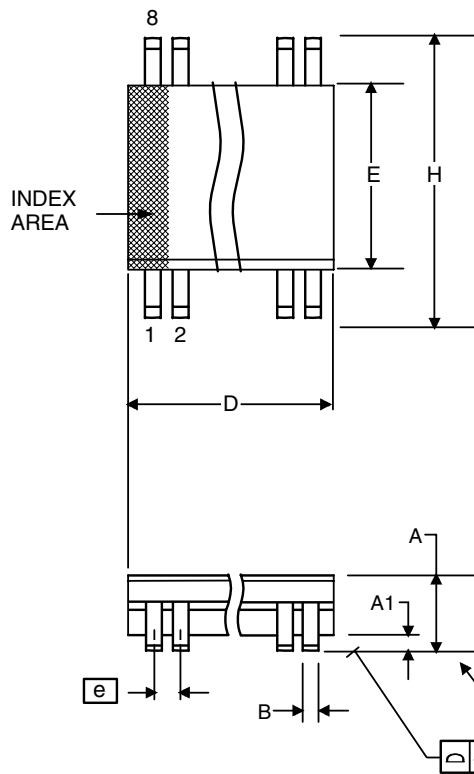


Notes:

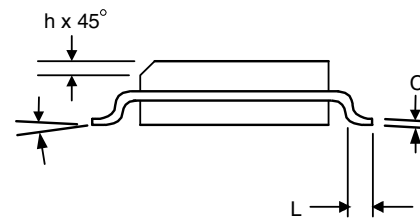
1. ##### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "LF" denotes Pb (lead) free package.
4. "I" denotes industrial temperature range.
5. Bottom marking: country of origin.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
181M-01*	see page 6	Tubes	8-pin SOIC	0 to +70° C
181M-01T*		Tape and Reel	8-pin SOIC	0 to +70° C
181M-01LF		Tubes	8-pin SOIC	0 to +70° C
181M-01LFT		Tape and Reel	8-pin SOIC	0 to +70° C
181MI-01*	see page 6	Tubes	8-pin SOIC	-40 to +85° C
181MI-01T*		Tape and Reel	8-pin SOIC	-40 to +85° C
181MI-01LF		Tubes	8-pin SOIC	-40 to +85° C
181MI-01LFT		Tape and Reel	8-pin SOIC	-40 to +85° C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, IDT assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

www.idt.com/go/clockhelp

Corporate Headquarters

Integrated Device Technology, Inc.
www.idt.com



www.IDT.com