

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .



3.3V ZERO DELAY CLOCK BUFFER

IDT2305

FEATURES:

- Phase-Lock Loop Clock Distribution
- 10MHz to 133MHz operating frequency
- Distributes one clock input to one bank of five outputs
- Zero Input-Output Delay
- Output Skew < 250ps
- Low jitter <200 ps cycle-to-cycle
- IDT2305-1 for Standard Drive
- IDT2305-1H for High Drive
- No external RC network required
- Operates at 3.3V V_{DD}
- Power down mode
- Available in SOIC package

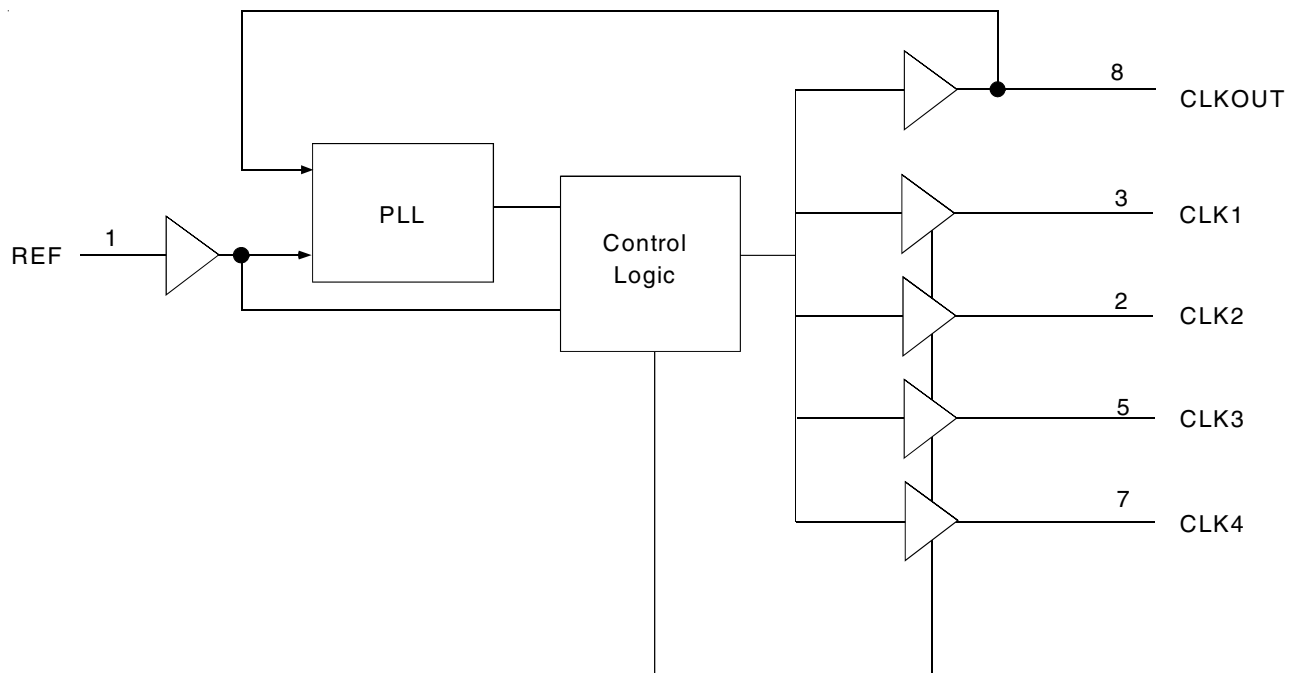
DESCRIPTION:

The IDT2305 is a high-speed phase-lock loop (PLL) clock buffer, designed to address high-speed clock distribution applications. The zero delay is achieved by aligning the phase between the incoming clock and the output clock, operable within the range of 10 to 133MHz.

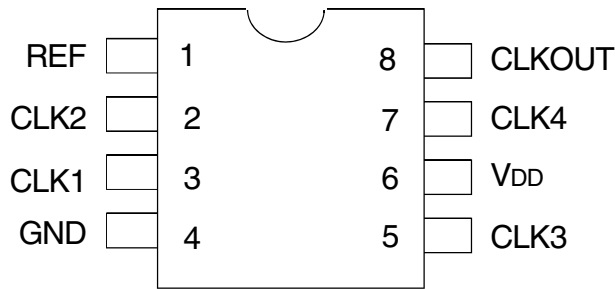
The IDT2305 is an 8-pin version of the IDT2309. IDT2305 accepts one reference input, and drives out five low skew clocks. The -1H version of this device operates, up to 133MHz frequency and has a higher drive than the -1 device. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad. In the absence of an input clock, the IDT2305 enters power down. In this mode, the device will draw less than 25µA, the outputs are tri-stated, and the PLL is not running, resulting in a significant reduction of power.

The IDT2305 is characterized for both Industrial and Commercial operation.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Max.	Unit
V _{DD}	Supply Voltage Range	-0.5 to +4.6	V
V _I ⁽²⁾	Input Voltage Range (REF)	-0.5 to +5.5	V
V _I	Input Voltage Range (except REF)	-0.5 to V _{DD} +0.5	V
I _{IK} (V _I < 0)	Input Clamp Current	-50	mA
I _O (V _O = 0 to V _{DD})	Continuous Output Current	±50	mA
V _{DD} or GND	Continuous Current	±100	mA
T _A = 55°C (in still air) ⁽³⁾	Maximum Power Dissipation	0.7	W
T _{STG}	Storage Temperature Range	-65 to +150	°C
Operating Temperature	Commercial Temperature Range	0 to +70	°C
Operating Temperature	Industrial Temperature Range	-40 to +85	°C

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

APPLICATIONS:

- SDRAM
- Telecom
- Datacom
- PC Motherboards/Workstations
- Critical Path Delay Designs

PIN DESCRIPTION

Pin Name	Pin Number	Type	Functional Description
REF ⁽¹⁾	1	IN	Input reference clock, 5 Volt tolerant input
CLK2 ⁽²⁾	2	Out	Output clock
CLK1 ⁽²⁾	3	Out	Output clock
GND	4	Ground	Ground
CLK3 ⁽²⁾	5	Out	Output clock
V _{DD}	6	PWR	3.3V Supply
CLK4 ⁽²⁾	7	Out	Output clock
CLKOUT ⁽²⁾	8	Out	Output clock, internal feedback on this pin

NOTES:

- Weak pull down.
- Weak pull down on all outputs.

OPERATING CONDITIONS - COMMERCIAL

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	Supply Voltage	3	3.6	V
T _A	Operating Temperature (Ambient Temperature)	0	70	°C
C _L	Load Capacitance < 100MHz	—	30	pF
	Load Capacitance 100MHz - 133MHz	—	10	
C _{IN}	Input Capacitance	—	7	pF

DC ELECTRICAL CHARACTERISTICS - COMMERCIAL

Symbol	Parameter	Conditions		Min.	Max.	Unit
V _{IL}	Input LOW Voltage Level			—	0.8	V
V _{IH}	Input HIGH Voltage Level			2	—	V
I _{IL}	Input LOW Current	V _{IN} = 0V		—	50	μA
I _{IH}	Input HIGH Current	V _{IN} = V _{DD}		—	100	μA
V _{OL}	Output LOW Voltage	Standard Drive	I _{OL} = 8mA	—	0.4	V
		High Drive	I _{OL} = 12mA (-1H)			
V _{OH}	Output HIGH Voltage	Standard Drive	I _{OH} = -8mA	2.4	—	V
		High Drive	I _{OH} = -12mA (-1H)			
I _{DD_PD}	Power Down Current	REF = 0MHz		—	12	μA
I _{DD}	Supply Current	Unloaded Outputs at 66.66MHz		—	32	mA

SWITCHING CHARACTERISTICS (2305-1) - COMMERCIAL ^(1,2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t _i	Output Frequency	10pF Load	10	—	133	MHz
		30pF Load	10	—	100	
	Duty Cycle = t ₂ ÷ t ₁	Measured at 1.4V, F _{OUT} = 66.66MHz	40	50	60	%
t _r	Rise Time	Measured between 0.8V and 2V	—	—	2.5	ns
t _f	Fall Time	Measured between 0.8V and 2V	—	—	2.5	ns
t _s	Output to Output Skew	All outputs equally loaded	—	—	250	ps
t _d	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at V _{DD} /2	—	0	±350	ps
t ₇	Device-to-Device Skew	Measured at V _{DD} /2 on the CLKOUT pins of devices	—	0	700	ps
t _j	Cycle-to-Cycle Jitter, pk - pk	Measured at 66.66MHz, loaded outputs	—	—	200	ps
t _{LOCK}	PLL Lock Time	Stable power supply, valid clock presented on REF pin	—	—	1	ms

NOTES:

- REF Input has a threshold voltage of V_{DD}/2.
- All parameters specified with loaded outputs.

SWITCHING CHARACTERISTICS (2305-1H) - COMMERCIAL ^(1,2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t _f	Output Frequency	10pF Load	10	—	133	MHz
		30pF Load	10	—	100	
	Duty Cycle = t ₂ ÷ t ₁	Measured at 1.4V, F _{OUT} = 66.66MHz	40	50	60	%
	Duty Cycle = t ₂ ÷ t ₁	Measured at 1.4V, F _{OUT} <50MHz	45	50	55	%
t _r	Rise Time	Measured between 0.8V and 2V	—	—	1.5	ns
t _f	Fall Time	Measured between 0.8V and 2V	—	—	1.5	ns
t _s	Output to Output Skew	All outputs equally loaded	—	—	250	ps
t _d	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at V _{DD} /2	—	0	±350	ps
t ₇	Device-to-Device Skew	Measured at V _{DD} /2 on the CLKOUT pins of devices	—	0	700	ps
t _s	Output Slew Rate	Measured between 0.8V and 2V using Test Circuit #2	1	—	—	V/ns
t _j	Cycle-to-Cycle Jitter, pk - pk	Measured at 66.66MHz, loaded outputs	—	—	200	ps
t _{LOCK}	PLL Lock Time	Stable power supply, valid clock presented on REF pin	—	—	1	ms

NOTES:

1. REF Input has a threshold voltage of V_{DD}/2.
2. All parameters specified with loaded outputs.

OPERATING CONDITIONS - INDUSTRIAL

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	Supply Voltage	3	3.6	V
T _A	Operating Temperature (Ambient Temperature)	-40	+85	°C
C _L	Load Capacitance < 100MHz	—	30	pF
	Load Capacitance 100MHz - 133MHz	—	10	
C _{IN}	Input Capacitance	—	7	pF

DC ELECTRICAL CHARACTERISTICS - INDUSTRIAL

Symbol	Parameter	Conditions		Min.	Max.	Unit
V _{IL}	Input LOW Voltage Level			—	0.8	V
V _{IH}	Input HIGH Voltage Level			2	—	V
I _{IL}	Input LOW Current	V _{IN} = 0V		—	50	μA
I _{IH}	Input HIGH Current	V _{IN} = V _{DD}		—	100	μA
V _{OL}	Output LOW Voltage	Standard Drive	I _{OL} = 8mA	—	0.4	V
		High Drive	I _{OL} = 12mA (-1H)			
V _{OH}	Output HIGH Voltage	Standard Drive	I _{OH} = -8mA	2.4	—	V
		High Drive	I _{OH} = -12mA (-1H)			
I _{DD_PD}	Power Down Current	REF = 0MHz		—	25	μA
I _{DD}	Supply Current	Unloaded Outputs at 66.66MHz		—	35	mA

SWITCHING CHARACTERISTICS (2305-1) - INDUSTRIAL^(1,2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t ₁	Output Frequency	10pF Load	10	—	133	MHz
		30pF Load	10	—	100	
	Duty Cycle = t ₂ ÷ t ₁	Measured at 1.4V, F _{OUT} = 66.66MHz	40	50	60	%
t ₃	Rise Time	Measured between 0.8V and 2V	—	—	2.5	ns
t ₄	Fall Time	Measured between 0.8V and 2V	—	—	2.5	ns
t ₅	Output to Output Skew	All outputs equally loaded	—	—	250	ps
t ₆	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at V _{DD} /2	—	0	±350	ps
t ₇	Device-to-Device Skew	Measured at V _{DD} /2 on the CLKOUT pins of devices	—	0	700	ps
t ₈	Cycle-to-Cycle Jitter, pk - pk	Measured at 66.66MHz, loaded outputs	—	—	200	ps
t _{LOCK}	PLL Lock Time	Stable power supply, valid clock presented on REF pin	—	—	1	ms

NOTES:

1. REF Input has a threshold voltage of V_{DD}/2.
2. All parameters specified with loaded outputs.

SWITCHING CHARACTERISTICS (2305-1H) - INDUSTRIAL^(1,2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t ₁	Output Frequency	10pF Load	10	—	133	MHz
		30pF Load	10	—	100	
	Duty Cycle = t ₂ ÷ t ₁	Measured at 1.4V, F _{OUT} = 66.66MHz	40	50	60	%
	Duty Cycle = t ₂ ÷ t ₁	Measured at 1.4V, F _{OUT} <50MHz	45	50	55	%
t ₃	Rise Time	Measured between 0.8V and 2V	—	—	1.5	ns
t ₄	Fall Time	Measured between 0.8V and 2V	—	—	1.5	ns
t ₅	Output to Output Skew	All outputs equally loaded	—	—	250	ps
t ₆	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at V _{DD} /2	—	0	±350	ps
t ₇	Device-to-Device Skew	Measured at V _{DD} /2 on the CLKOUT pins of devices	—	0	700	ps
t ₈	Output Slew Rate	Measured between 0.8V and 2V using Test Circuit #2	1	—	—	V/ns
t ₈	Cycle-to-Cycle Jitter, pk - pk	Measured at 66.66MHz, loaded outputs	—	—	200	ps
t _{LOCK}	PLL Lock Time	Stable power supply, valid clock presented on REF pin	—	—	1	ms

NOTES:

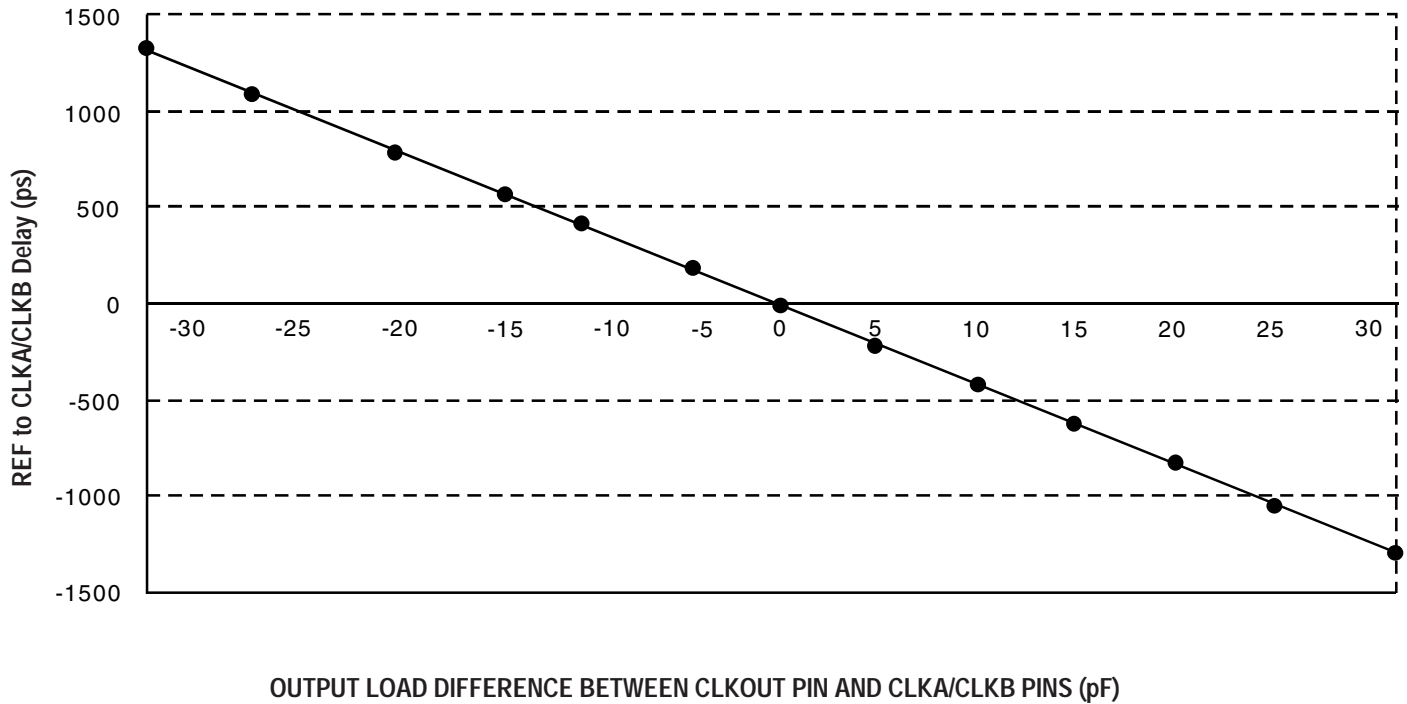
1. REF Input has a threshold voltage of V_{DD}/2.
2. All parameters specified with loaded outputs.

ZERO DELAY AND SKEW CONTROL

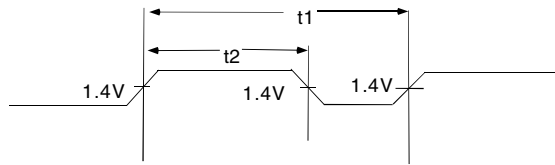
All outputs should be uniformly loaded in order to achieve Zero I/O Delay. Since the CLKOUT pin is the internal feedback for the PLL, its relative loading can affect and adjust the input/output delay. The Output Load Difference diagram illustrates the PLL's relative loading with respect to the other outputs that can adjust the Input-Output (I/O) Delay.

For designs utilizing zero I/O Delay, all outputs including CLKOUT must be equally loaded. Even if the output is not used, it must have a capacitive load equal to that on the other outputs in order to obtain true zero I/O Delay. If I/O Delay adjustments are needed, use the Output Load Difference diagram to calculate loading differences between the CLKOUT pin and other outputs. For zero output-to-output skew, all outputs must be loaded equally.

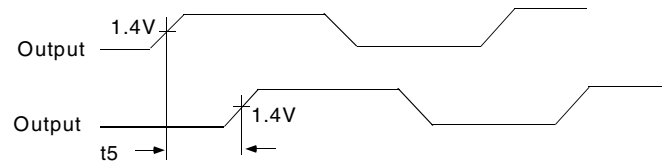
REF TO CLKA/CLKB RELAY vs. OUTPUT LOAD DIFFERENCE BETWEEN CLKOUT PIN AND CLKA/CLKB PINS



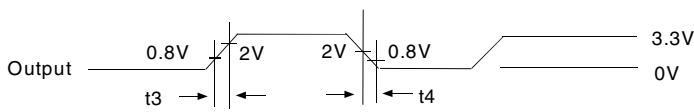
SWITCHING WAVEFORMS



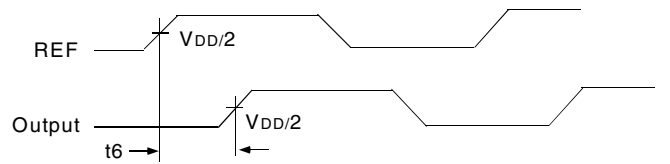
Duty Cycle Timing



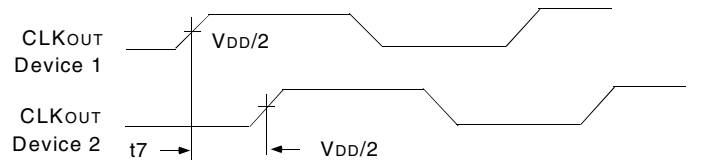
Output to Output Skew



All Outputs Rise/Fall Time

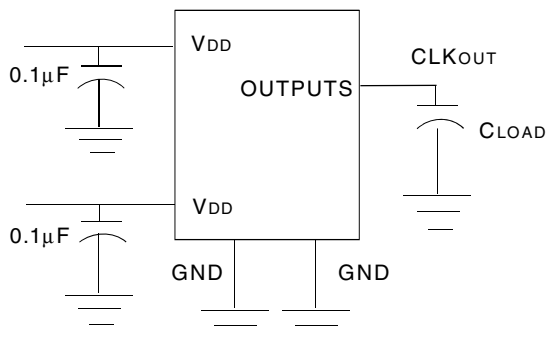


Input to Output Propagation Delay

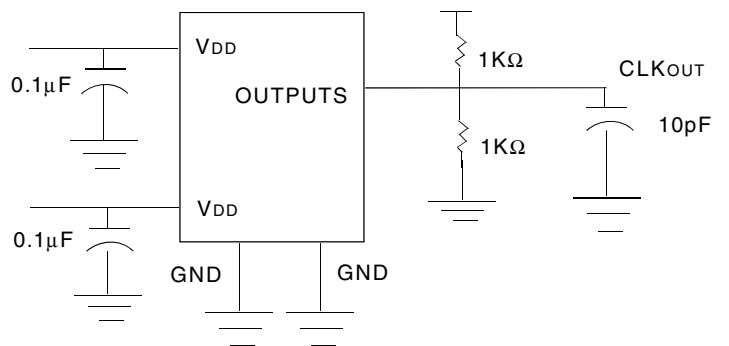


Device to Device Skew

TEST CIRCUITS

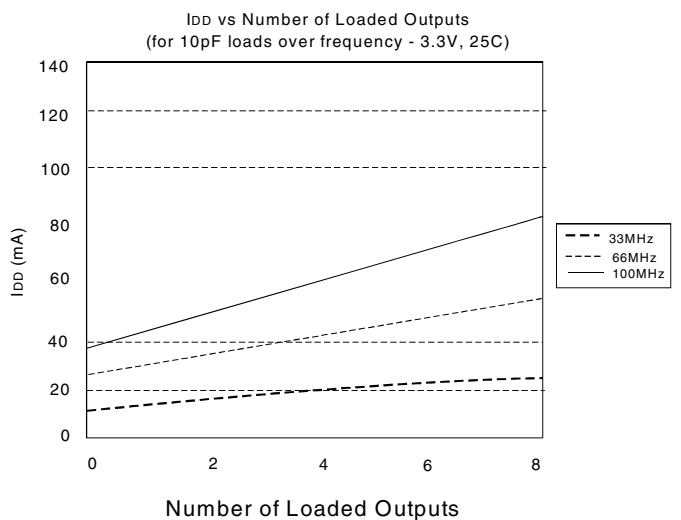
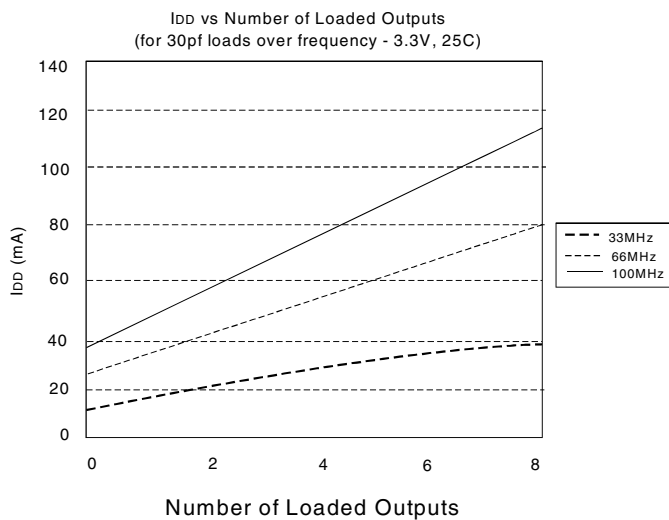
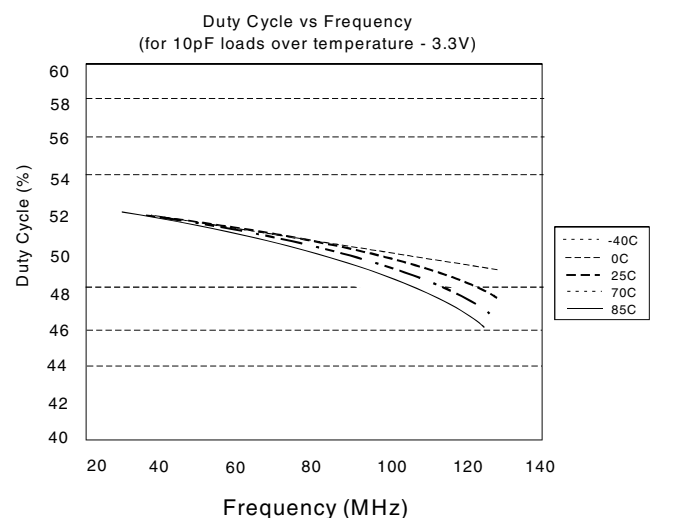
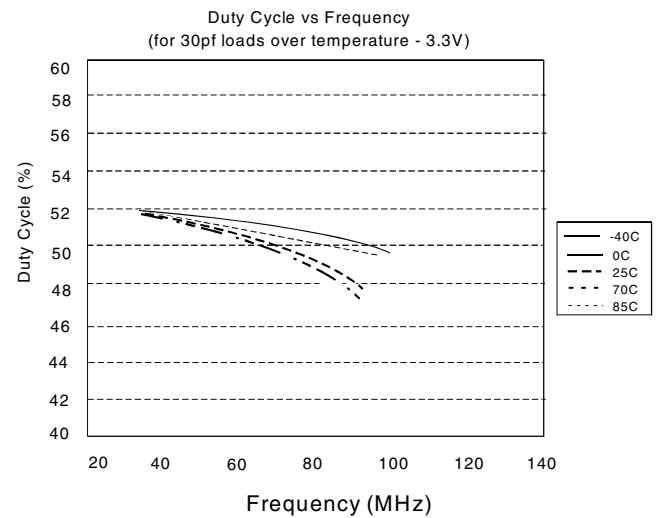
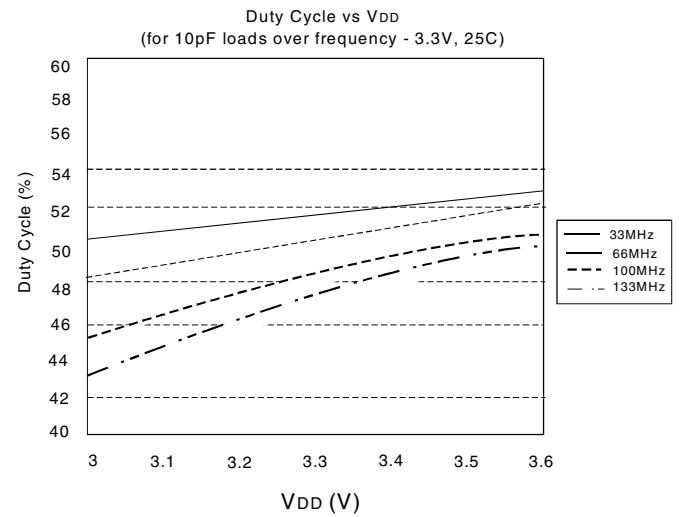
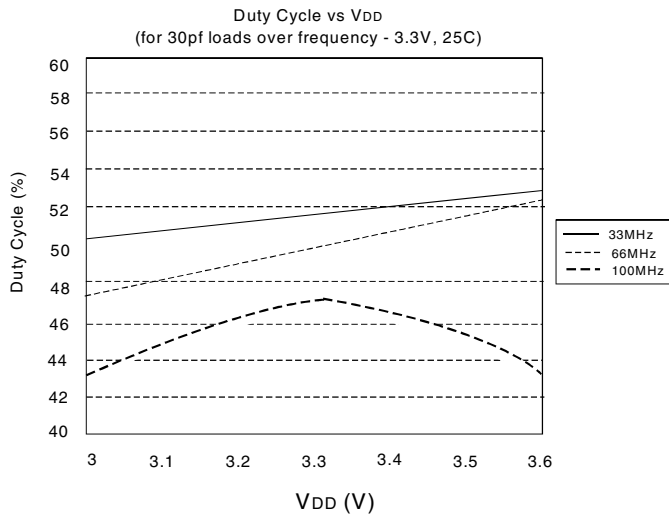


Test Circuit 1 (all Parameters Except t8)



Test Circuit 2 (t8, Output Slew Rate On -1H Devices)

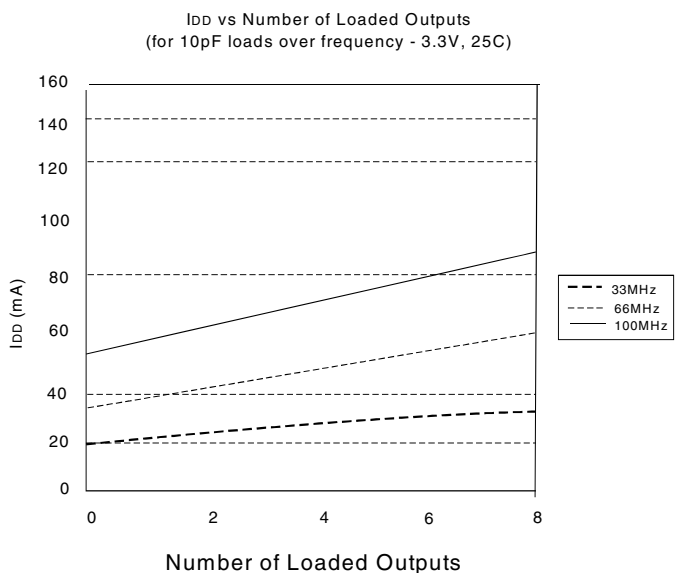
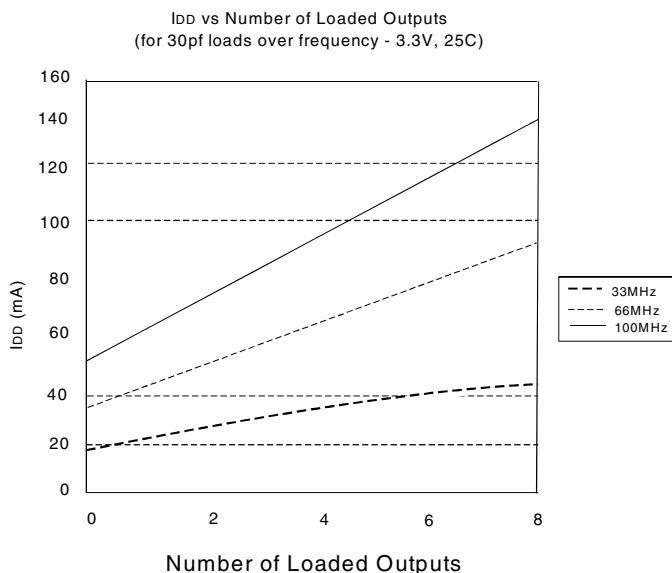
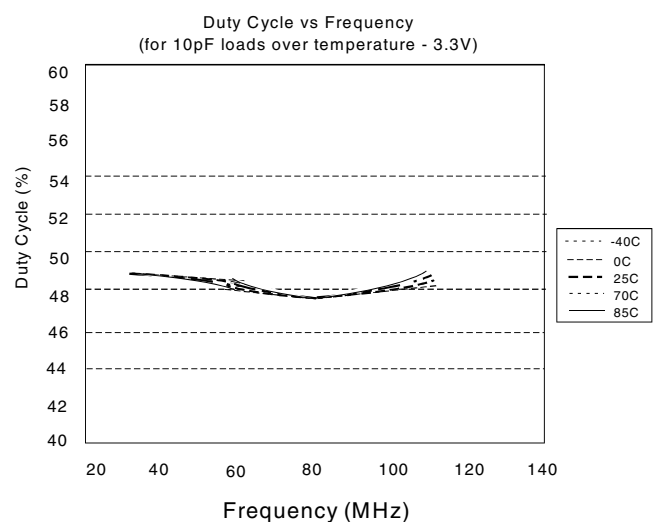
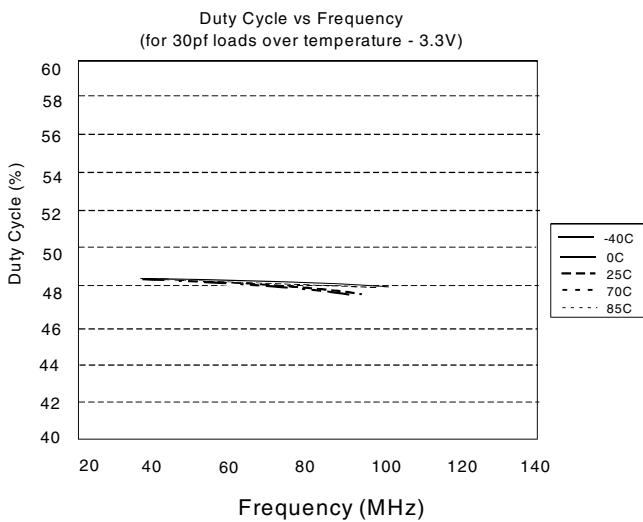
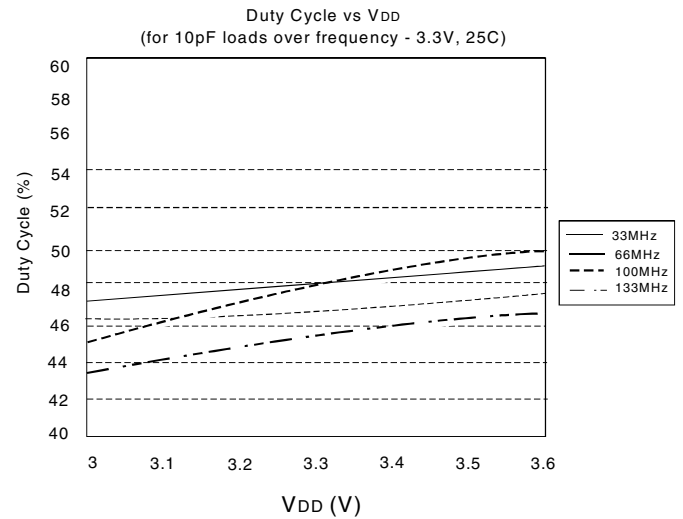
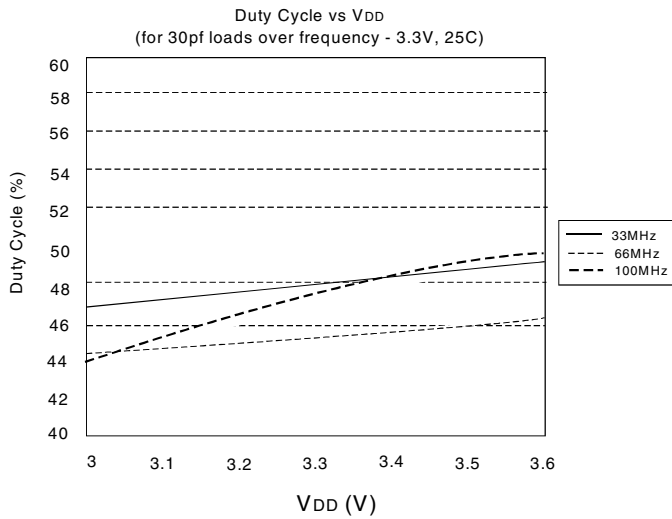
TYPICAL DUTY CYCLE⁽¹⁾ AND I_{DD} TRENDS⁽²⁾ FOR IDT2305-1



NOTES:

- Duty Cycle is taken from typical chip measured at 1.4V.
- I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current. (n = Number of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = Frequency (Hz))

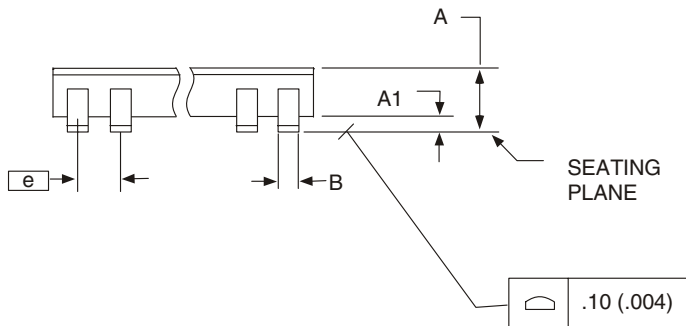
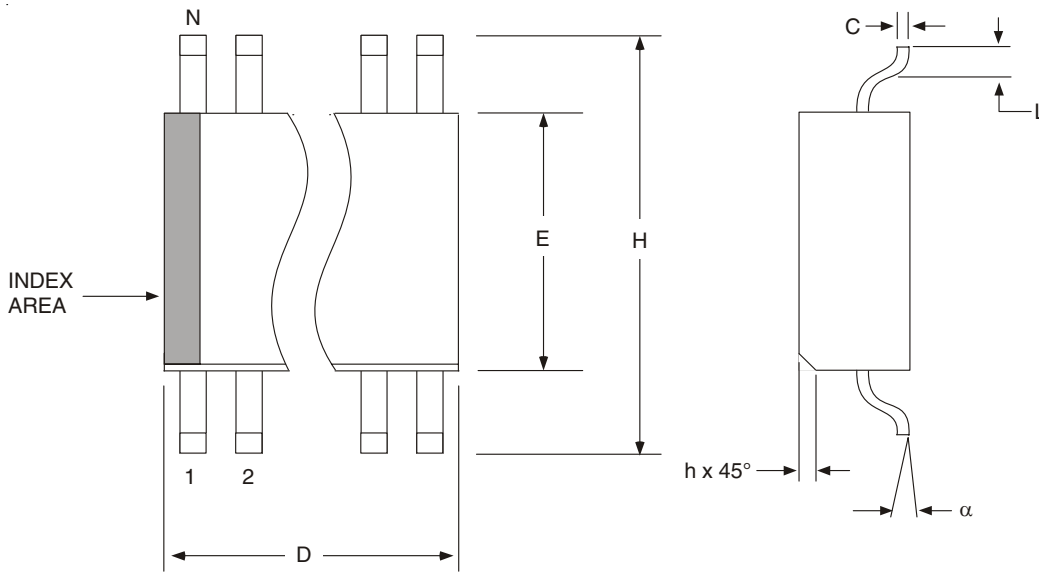
TYPICAL DUTY CYCLE⁽¹⁾ AND I_{DD} TRENDS⁽²⁾ FOR IDT2305-1H



NOTES:

- Duty Cycle is taken from typical chip measured at 1.4V.
- I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCfV$, where I_{CORE} is the unloaded current. (n = Number of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = Frequency (Hz))

PACKAGE OUTLINE AND PACKAGE DIMENSIONS - SOIC



150 mil (Narrow Body) SOIC

SYMBOL	In Millimeters		In Inches ⁽¹⁾	
	COMMON DIMENSIONS		COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.0130	.0200
C	0.19	0.25	.0075	.0098
D	SEE VARIATIONS		SEE VARIATIONS	
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

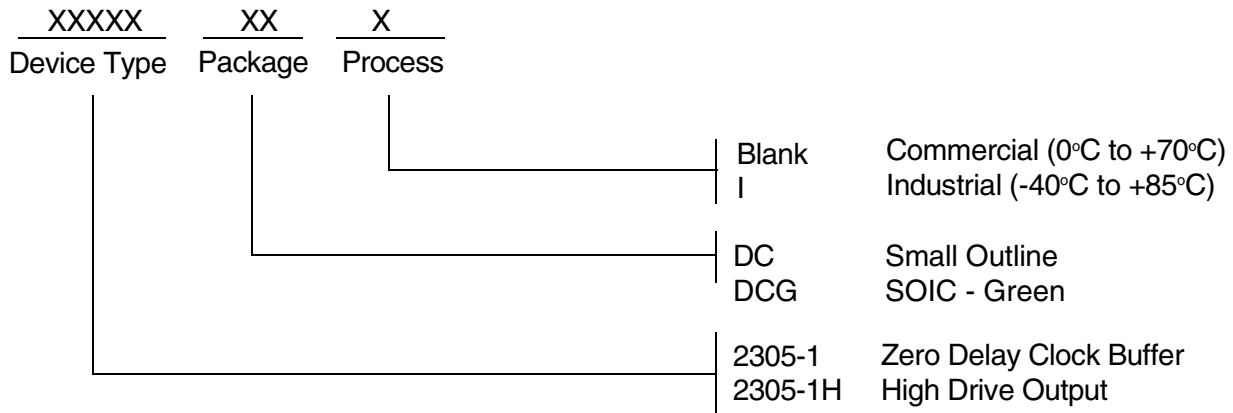
NOTE:
1. For reference only. Controlling dimensions are in mm.

VARIATIONS

N	D (mm)		D (inch) ⁽¹⁾	
	MIN	MAX	MIN	MAX
8	4.80	5.00	.1890	.1968
14	8.55	8.75	.3367	.3444
16	9.80	10.00	.3859	.3937

NOTE:
1. For reference only. Controlling dimensions are in mm.

ORDERING INFORMATION



Ordering Code	Package Type	Operating Range
IDT2305-1DC	8-Pin SOIC	Commercial
IDT2305-1DCG	8-Pin SOIC	Commercial
IDT2305-1DCI	8-Pin SOIC	Industrial
IDT2305-1DCGI	8-Pin SOIC	Industrial
IDT2305-1HDC	8-Pin SOIC	Commercial
IDT2305-1HDCI	8-Pin SOIC	Industrial



CORPORATE HEADQUARTERS
 6024 Silver Creek Valley Road
 San Jose, CA 95138

for SALES:
 800-345-7015 or 408-284-8200
 fax: 408-284-2775
 www.idt.com

for Tech Support:
 clockhelp@idt.com