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3.3V ZERO DELAY CLOCK MULTIPLIER

IDT2308

FEATURES:

- Phase-Lock Loop Clock Distribution for Applications ranging from 10MHz to 133MHz operating frequency
- Distributes one clock input to two banks of four outputs
- Separate output enable for each output bank
- External feedback (FBK) pin is used to synchronize the outputs to the clock input
- Output Skew <200 ps
- Low jitter <200 ps cycle-to-cycle
- 1x, 2x, 4x output options (see table):
 - IDT2308-1 1x
 - IDT2308-2 1x, 2x
 - IDT2308-3 2x, 4x
 - IDT2308-4 2x
 - IDT2308-1H, -2H, and -5H for High Drive
- No external RC network required
- Operates at 3.3V VDD
- Available in SOIC and TSSOP packages

DESCRIPTION:

The IDT2308 is a high-speed phase-lock loop (PLL) clock multiplier. It is designed to address high-speed clock distribution and multiplication applications. The zero delay is achieved by aligning the phase between the incoming clock and the output clock, operable within the range of 10 to 133MHz.

The IDT2308 has two banks of four outputs each that are controlled via two select addresses. By proper selection of input addresses, both banks can be put in tri-state mode. In test mode, the PLL is turned off, and the input clock directly drives the outputs for system testing purposes. In the absence of an input clock, the IDT2308 enters power down, and the outputs are tri-stated. In this mode, the device will draw less than 25µA.

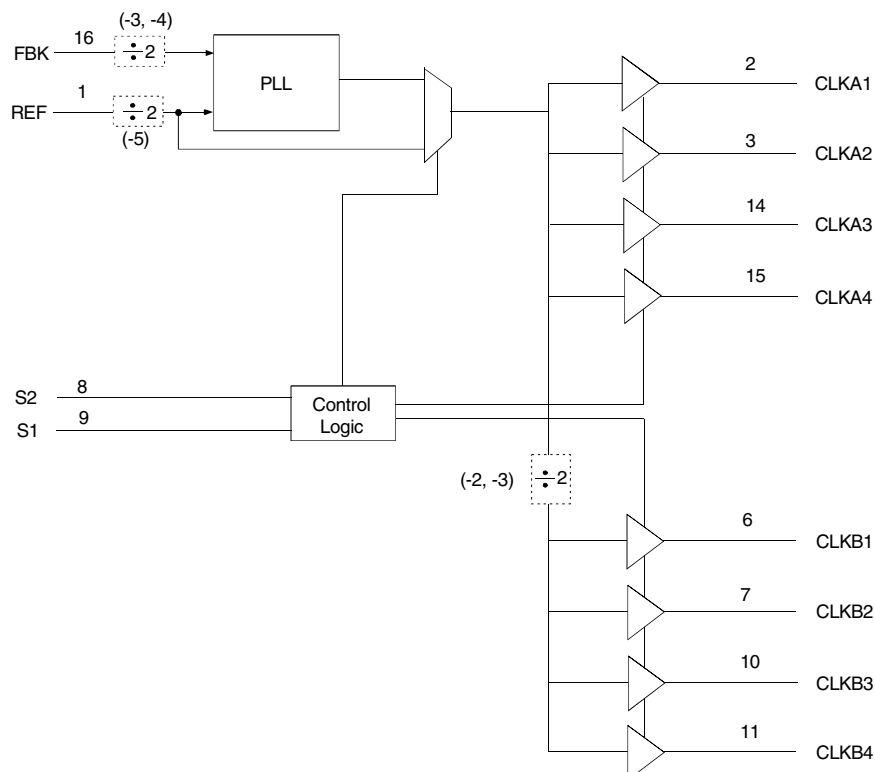
The IDT2308 is available in six unique configurations for both pre-scaling and multiplication of the Input REF Clock. (See available options table.)

The PLL is closed externally to provide more flexibility by allowing the user to control the delay between the input clock and the outputs.

The IDT2308 is characterized for both Industrial and Commercial operation.

NOTE: EOL for non-green parts to occur on 5/13/10 per PDNU-09-01

FUNCTIONAL BLOCK DIAGRAM

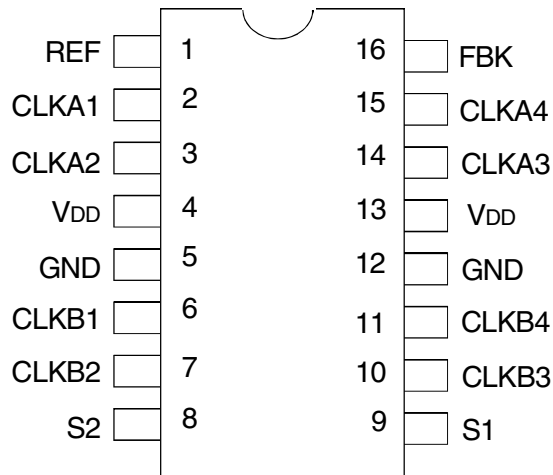


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COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES

AUGUST 2009

PIN CONFIGURATION



SOIC/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Rating | Max. | Unit |
|---|--|------------------------------|------|
| V _{DD} | Supply Voltage Range | -0.5 to +4.6 | V |
| V _I ⁽²⁾ | Input Voltage Range (REF) | -0.5 to +5.5 | V |
| V _I | Input Voltage Range (except REF) | -0.5 to V _{DD} +0.5 | V |
| I _{IK} (V _I < 0) | Input Clamp Current | -50 | mA |
| I _{OK} | Terminal Voltage with Respect to GND (inputs V _{IH} 2.5, V _{IL} 2.5) | ±50 | mA |
| I _O | Continuous Output Current (V _O = 0 to V _{DD}) | ±50 | mA |
| V _{DD} or GND | Continuous Current | ±100 | mA |
| T _A = 55°C (in still air) ⁽³⁾ | Maximum Power Dissipation | 0.7 | W |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| Operating Temperature | Commercial Temperature Range | 0 to +70 | °C |
| Operating Temperature | Industrial Temperature Range | -40 to +85 | °C |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

PIN DESCRIPTION

| | Pin Number | Functional Description |
|----------------------|------------|--|
| REF ⁽¹⁾ | 1 | Input Reference Clock, 5 Volt Tolerant Input |
| CLKA1 ⁽²⁾ | 2 | Clock Output for Bank A |
| CLKA2 ⁽²⁾ | 3 | Clock Output for Bank A |
| V _{DD} | 4 | 3.3V Supply |
| GND | 5 | Ground |
| CLKB1 ⁽²⁾ | 6 | Clock Output for Bank B |
| CLKB2 ⁽²⁾ | 7 | Clock Output for Bank B |
| S2 ⁽³⁾ | 8 | Select Input, Bit 2 |
| S1 ⁽³⁾ | 9 | Select Input, Bit 1 |
| CLKB3 ⁽²⁾ | 10 | Clock Output for Bank B |
| CLKB4 ⁽²⁾ | 11 | Clock Output for Bank B |
| GND | 12 | Ground |
| V _{DD} | 13 | 3.3V Supply |
| CLKA3 ⁽²⁾ | 14 | Clock Output for Bank A |
| CLKA4 ⁽²⁾ | 15 | Clock Output for Bank A |
| FBK | 16 | PLL Feedback Input |

NOTES:

- Weak pull down.
- Weak pull down on all outputs.
- Weak pull ups on these inputs.

APPLICATIONS:

- SDRAM
- Telecom
- Datacom
- PC Motherboards/Workstations
- Critical Path Delay Designs

FUNCTION TABLE⁽¹⁾ SELECT INPUT DECODING

| S2 | S1 | CLK A | CLK B | Output Source | PLL Shut Down |
|----|----|-----------|-----------|---------------|---------------|
| L | L | Tri-State | Tri-State | PLL | Y |
| L | H | Driven | Tri-State | PLL | N |
| H | L | Driven | Driven | REF | Y |
| H | H | Driven | Driven | PLL | N |

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level

AVAILABLE OPTIONS FOR IDT2308

| Device | Feedback From | Bank A Frequency | Bank B Frequency |
|------------|------------------|------------------|---------------------------------------|
| IDT2308-1 | Bank A or Bank B | Reference | Reference |
| IDT2308-1H | Bank A or Bank B | Reference | Reference |
| IDT2308-2 | Bank A | Reference | Reference/2 |
| IDT2308-2 | Bank B | 2 x Reference | Reference |
| IDT2308-2H | Bank A | Reference | Reference/2 |
| IDT2308-2H | Bank B | 2 x Reference | Reference |
| IDT2308-3 | Bank A | 2 x Reference | Reference or Reference ⁽¹⁾ |
| IDT2308-3 | Bank B | 4 x Reference | 2 x Reference |
| IDT2308-4 | Bank A or Bank B | 2 x Reference | 2 x Reference |
| IDT2308-5H | Bank A or Bank B | Reference/2 | Reference/2 |

NOTE:

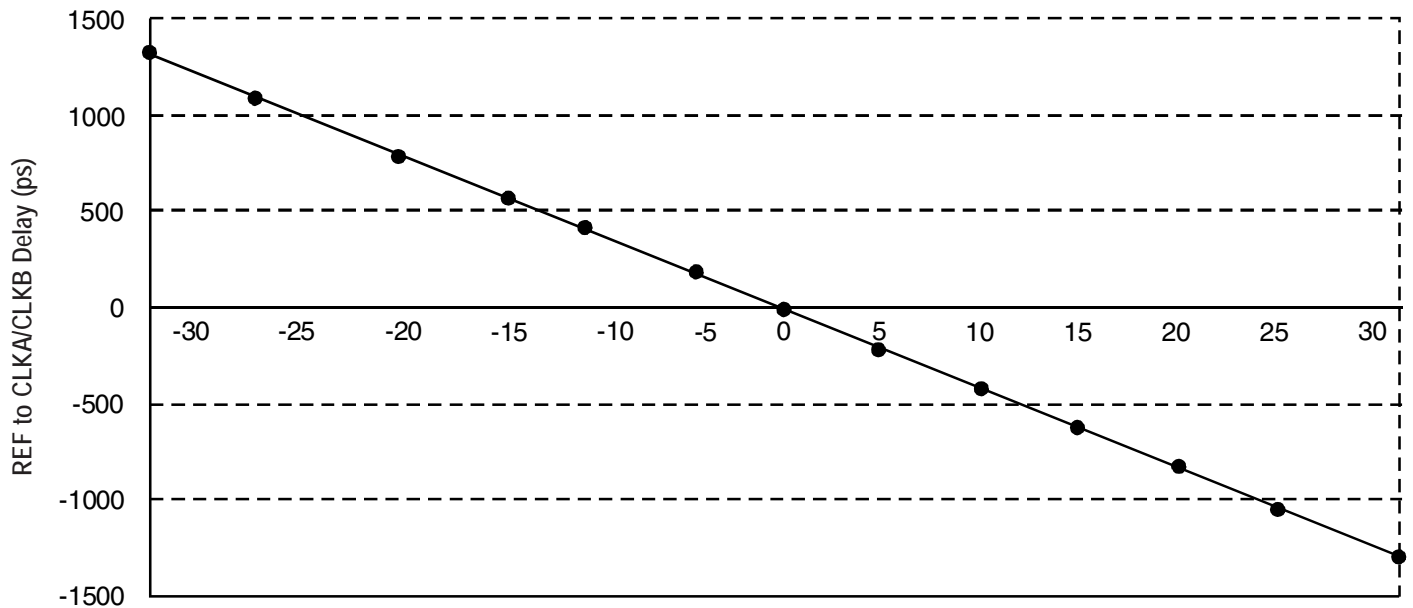
- Output phase is indeterminant (0° or 180° from input clock).

ZERO DELAY AND SKEW CONTROL

To close the feedback loop of the IDT2308, the FBK pin can be driven from any of the eight available output pins. The output driving the FBK pin will be driving a total load of 7pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use the Output Load Difference Chart to calculate loading differences between the feedback output and remaining outputs. Ensure the outputs are loaded equally, for zero output-output skew.

REF TO CLKA/CLKB DELAY vs. OUTPUT LOAD DIFFERENCE BETWEEN FBK PIN AND CLKA/CLKB PINS



OUTPUT LOAD DIFFERENCE BETWEEN FBK PIN AND CLKA/CLKB PINS (pF)

OPERATING CONDITIONS- COMMERCIAL

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|---|-----------------|------|------|------|
| V _{DD} | Supply Voltage | | 3 | 3.6 | V |
| T _A | Operating Temperature (Ambient Temperature) | | 0 | 70 | °C |
| C _L | Load Capacitance below 100MHz | | — | 30 | pF |
| | Load Capacitance from 100MHz to 133MHz | | — | 15 | pF |
| C _{IN} | Input Capacitance ⁽¹⁾ | | — | 7 | pF |

NOTE:

1. Applies to both REF and FBK.

DC ELECTRICAL CHARACTERISTICS - COMMERCIAL

| Symbol | Parameter | Conditions | Min. | Typ. ⁽¹⁾ | Max. | Unit | |
|--------------------|--------------------------|--|------------------------------|---------------------|------|------|----|
| V _{IL} | Input LOW Voltage Level | | — | — | 0.8 | V | |
| V _{IH} | Input HIGH Voltage Level | | 2 | — | — | V | |
| I _{IL} | Input LOW Current | V _{IN} = 0V | — | — | 50 | μA | |
| I _{IH} | Input HIGH Current | V _{IN} = V _{DD} | — | — | 100 | μA | |
| V _{OL} | Output LOW Voltage | I _{oL} = 8mA (-1, -2, -3, -4) I _{oL} = 12mA (-1H, -2H, -5H) | — | — | 0.4 | V | |
| V _{OH} | Output HIGH Voltage | I _{oH} = -8mA (-1, -2, -3, -4) I _{oH} = -12mA (-1H, -2H, -5H) | 2.4 | — | — | V | |
| I _{DD_PD} | Power Down Current | REF = 0MHz (S2 = S1 = H) | — | — | 12 | μA | |
| I _{DD} | Supply Current | Unloaded Outputs Select Inputs at V _{DD} or GND | 100MHz CLKA (-1, -2, -3, -4) | — | — | 45 | mA |
| | | | 100MHz CLKA (-1H, -2H, -5H) | — | — | 70 | |
| | | | 66MHz CLKA (-1, -2, -3, -4) | — | — | 32 | |
| | | | 66MHz CLKA (-1H, -2H, -5H) | — | — | 50 | |
| | | | 33MHz CLKA (-1, -2, -3, -4) | — | — | 18 | |
| | | | 33MHz CLKA (-1H, -2H, -5H) | — | — | 30 | |

SWITCHING CHARACTERISTICS - COMMERCIAL

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------------|---|---|------|------|-------|------|
| t _i | Output Frequency | 30pF Load, all devices | 10 | — | 100 | MHz |
| t _i | Output Frequency | 20pF Load, -1H, -2H, -5H Devices ⁽¹⁾ | 10 | — | 133.3 | MHz |
| t _i | Output Frequency | 15pF Load, -1, -2, -3, -4 devices | 10 | — | 133.3 | MHz |
| | Duty Cycle = t ₂ ÷ t ₁ (-1, -2, -3, -4, -1H, -2H, -5H) | Measured at 1.4V, F _{OUT} = 66.66MHz 30pF Load | 40 | 50 | 60 | % |
| | Duty Cycle = t ₂ ÷ t ₁ (-1, -2, -3, -4, -1H, -2H, -5H) | Measured at 1.4V, F _{OUT} = 50MHz 15pF Load | 45 | 50 | 55 | % |
| t _r | Rise Time (-1, -2, -3, -4) | Measured between 0.8V and 2V, 30pF Load | — | — | 2.2 | ns |
| t _r | Rise Time (-1, -2, -3, -4) | Measured between 0.8V and 2V, 15pF Load | — | — | 1.5 | ns |
| t _r | Rise Time (-1H, -2H, -5H) | Measured between 0.8V and 2V, 30pF Load | — | — | 1.5 | ns |
| t _f | Fall Time (-1, -2, -3, -4) | Measured between 0.8V and 2V, 30pF Load | — | — | 2.2 | ns |
| t _f | Fall Time (-1, -2, -3, -4) | Measured between 0.8V and 2V, 15pF Load | — | — | 1.5 | ns |
| t _f | Fall Time (-1H, -5H) | Measured between 0.8V and 2V, 30pF Load | — | — | 1.25 | ns |
| t _s | Output to Output Skew on same Bank (-1, -2, -3, -4) | All outputs equally loaded | — | — | 200 | ps |
| | Output to Output Skew (-1H, -2H, -5H) | All outputs equally loaded | — | — | 200 | ps |
| | Output Bank A to Output Bank B (-1, -4, -2H, -5H) | All outputs equally loaded | — | — | 200 | ps |
| | Output Bank A to Output Bank B Skew (-2, -3) | All outputs equally loaded | — | — | 400 | ps |
| t _d | Delay, REF Rising Edge to FBK Rising Edge | Measured at V _{DD} /2 | — | 0 | ±250 | ps |
| t ₇ | Device to Device Skew | Measured at V _{DD} /2 on the FBK pins of devices | — | 0 | 700 | ps |
| t _s | Output Slew Rate | Measured between 0.8V and 2V on -1H, -2H, -5H device using Test Circuit 2 | 1 | — | — | V/ns |
| ∅ | Cycle to Cycle Jitter (-1, -1H, -4, -5H) | Measured at 66.67 MHz, loaded outputs, 15pF Load | — | — | 200 | ps |
| | | Measured at 66.67 MHz, loaded outputs, 30pF Load | — | — | 200 | |
| | | Measured at 133.3 MHz, loaded outputs, 15pF Load | — | — | 100 | |
| ∅ | Cycle to Cycle Jitter (-2, -2H, -3) | Measured at 66.67 MHz, loaded outputs, 30pF Load | — | — | 400 | ps |
| | | Measured at 66.67 MHz, loaded outputs, 15pF Load | — | — | 400 | |
| t _{LOCK} | PLL Lock Time | Stable Power Supply, valid clocks presented on REF and FBK pins | — | — | 1 | ms |

NOTE:

1. IDT2308-5H has maximum input frequency of 133.33 MHz and maximum output of 66.67MHz.

OPERATING CONDITIONS- INDUSTRIAL

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|---|-----------------|------|------|------|
| V _{DD} | Supply Voltage | | 3 | 3.6 | V |
| T _A | Operating Temperature (Ambient Temperature) | | -40 | +85 | °C |
| C _L | Load Capacitance below 100MHz | | — | 30 | pF |
| | Load Capacitance from 100MHz to 133MHz | | — | 15 | pF |
| C _{IN} | Input Capacitance ⁽¹⁾ | | — | 7 | pF |

NOTE:

1. Applies to both REF and FBK.

DC ELECTRICAL CHARACTERISTICS - INDUSTRIAL

| Symbol | Parameter | Conditions | Min. | Typ. ⁽¹⁾ | Max. | Unit | |
|--------------------|--------------------------|--|------------------------------|---------------------|------|------|----|
| V _{IL} | Input LOW Voltage Level | | — | — | 0.8 | V | |
| V _{IH} | Input HIGH Voltage Level | | 2 | — | — | V | |
| I _{IL} | Input LOW Current | V _{IN} = 0V | — | — | 50 | μA | |
| I _{IH} | Input HIGH Current | V _{IN} = V _{DD} | — | — | 100 | μA | |
| V _{OL} | Output LOW Voltage | I _{OL} = 8mA (-1, -2, -3, -4) I _{OL} = 12mA (-1H, -2H, -5H) | — | — | 0.4 | V | |
| V _{OH} | Output HIGH Voltage | I _{OH} = -8mA (-1, -2, -3, -4) I _{OH} = -12mA (-1H, -2H, -5H) | 2.4 | — | — | V | |
| I _{DD_PD} | Power Down Current | REF = 0MHz (S2 = S1 = H) | — | — | 25 | μA | |
| I _{DD} | Supply Current | Unloaded Outputs Select Inputs at V _{DD} or GND | 100MHz CLKA (-1, -2, -3, -4) | — | — | 45 | mA |
| | | | 100MHz CLKA (-1H, -2H, -5H) | — | — | 70 | |
| | | | 66MHz CLKA (-1, -2, -3, -4) | — | — | 32 | |
| | | | 66MHz CLKA (-1H, -2H, -5H) | — | — | 50 | |
| | | | 33MHz CLKA (-1, -2, -3, -4) | — | — | 18 | |
| | | | 33MHz CLKA (-1H, -2H, -5H) | — | — | 30 | |

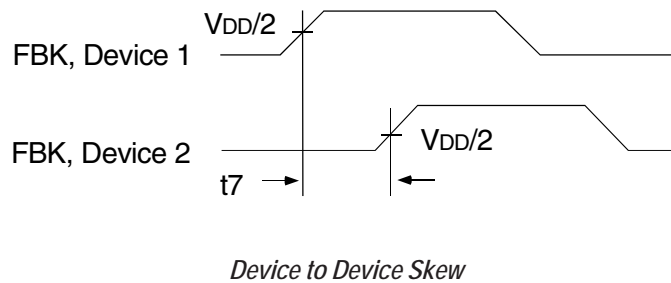
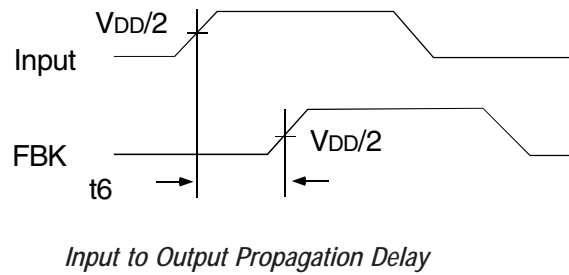
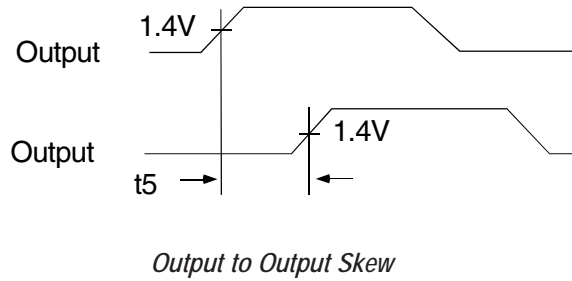
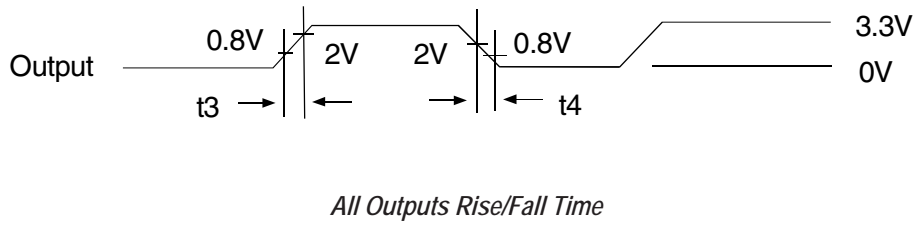
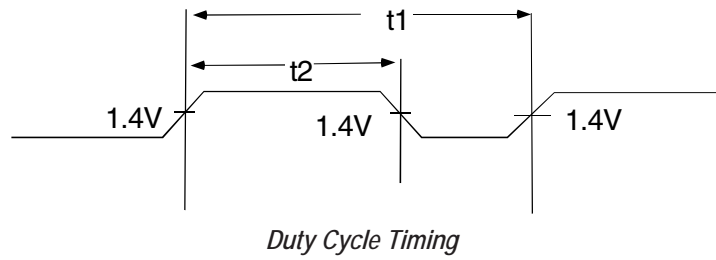
SWITCHING CHARACTERISTICS - INDUSTRIAL

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------------|--|---|------|------|-------|------|
| t _i | Output Frequency | 30pF Load, all devices | 10 | — | 100 | MHz |
| t _i | Output Frequency | 20pF Load, -1H, -2H, -5H Devices ⁽¹⁾ | 10 | — | 133.3 | MHz |
| t _i | Output Frequency | 15pF Load, -1, -2, -3, -4 devices | 10 | — | 133.3 | MHz |
| | Duty Cycle = $t_2 \div t_1$ (-1, -2, -3, -4, -1H, -2H, -5H) | Measured at 1.4V, F _{OUT} = 66.66MHz 30pF Load | 40 | 50 | 60 | % |
| | Duty Cycle = $t_2 \div t_1$ (-1, -2, -3, -4, -1H, -2H, -5H) | Measured at 1.4V, F _{OUT} = 50MHz 15pF Load | 45 | 50 | 55 | % |
| t _r | Rise Time (-1, -2, -3, -4) | Measured between 0.8V and 2V, 30pF Load | — | — | 2.2 | ns |
| t _r | Rise Time (-1, -2, -3, -4) | Measured between 0.8V and 2V, 15pF Load | — | — | 1.5 | ns |
| t _r | Rise Time (-1H, -2H, -5H) | Measured between 0.8V and 2V, 30pF Load | — | — | 1.5 | ns |
| t _f | Fall Time (-1, -2, -3, -4) | Measured between 0.8V and 2V, 30pF Load | — | — | 2.5 | ns |
| t _f | Fall Time (-1, -2, -3, -4) | Measured between 0.8V and 2V, 15pF Load | — | — | 1.5 | ns |
| t _f | Fall Time (-1H, -5H) | Measured between 0.8V and 2V, 30pF Load | — | — | 1.25 | ns |
| t _s | Output to Output Skew on same Bank (-1, -2, -3, -4) | All outputs equally loaded | — | — | 200 | ps |
| | Output to Output Skew (-1H, -2H, -5H) | All outputs equally loaded | — | — | 200 | ps |
| | Output Bank A to Output Bank B (-1, -4, -2H, -5H) | All outputs equally loaded | — | — | 200 | ps |
| | Output Bank A to Output Bank B Skew (-2, -3) | All outputs equally loaded | — | — | 400 | ps |
| t _d | Delay, REF Rising Edge to FBK Rising Edge | Measured at V _{DD} /2 | — | 0 | ±250 | ps |
| t _r | Device to Device Skew | Measured at V _{DD} /2 on the FBK pins of devices | — | 0 | 700 | ps |
| t _s | Output Slew Rate | Measured between 0.8V and 2V on -1H, -2H, -5H device using Test Circuit 2 | 1 | — | — | V/ns |
| ∅ | Cycle to Cycle Jitter (-1, -1H, -4, -5H) | Measured at 66.67 MHz, loaded outputs, 15pF Load | — | — | 200 | ps |
| | | Measured at 66.67 MHz, loaded outputs, 30pF Load | — | — | 200 | |
| | | Measured at 133.3 MHz, loaded outputs, 15pF Load | — | — | 100 | |
| ∅ | Cycle to Cycle Jitter (-2, -2H, -3) | Measured at 66.67 MHz, loaded outputs, 30pF Load | — | — | 400 | ps |
| | | Measured at 66.67 MHz, loaded outputs, 15pF Load | — | — | 400 | |
| t _{lock} | PLL Lock Time | Stable Power Supply, valid clocks presented on REF and FBK pins | — | — | 1 | ms |

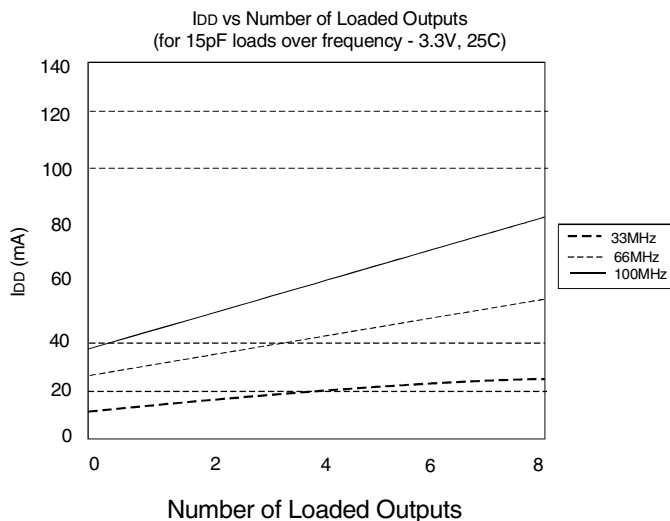
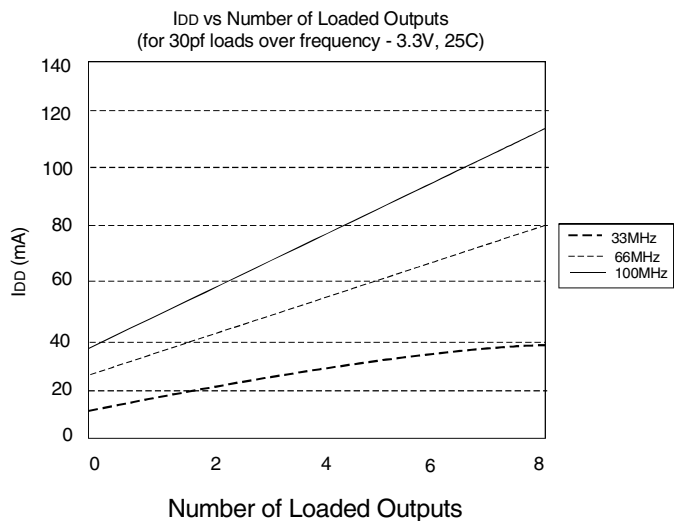
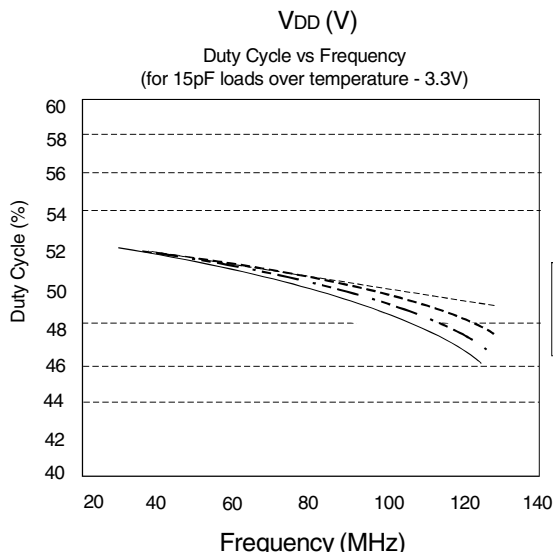
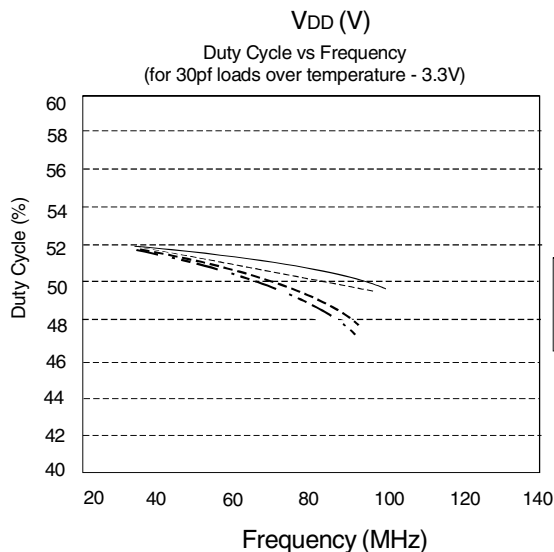
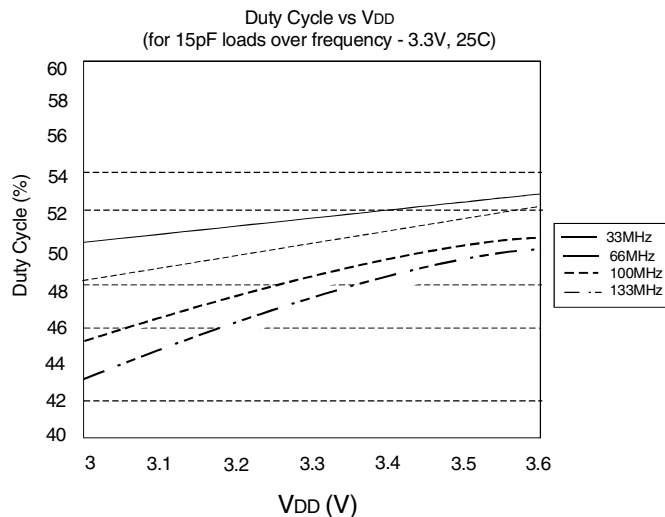
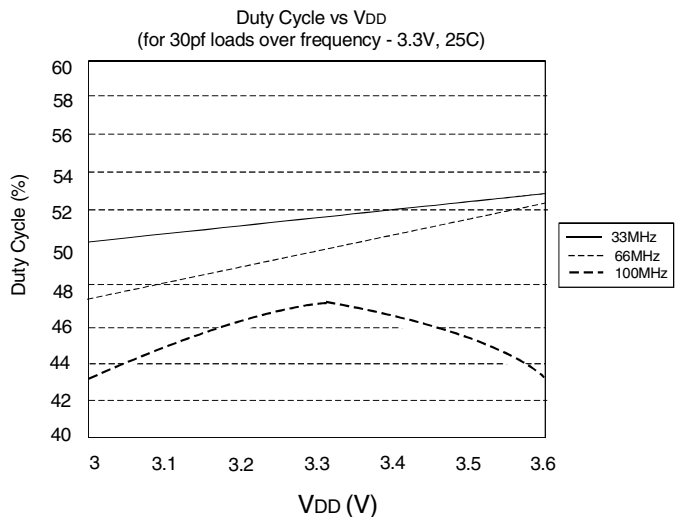
NOTE:

- IDT2308-5H has maximum input frequency of 133.33 MHz and maximum output of 66.67MHz.

SWITCHING WAVEFORMS



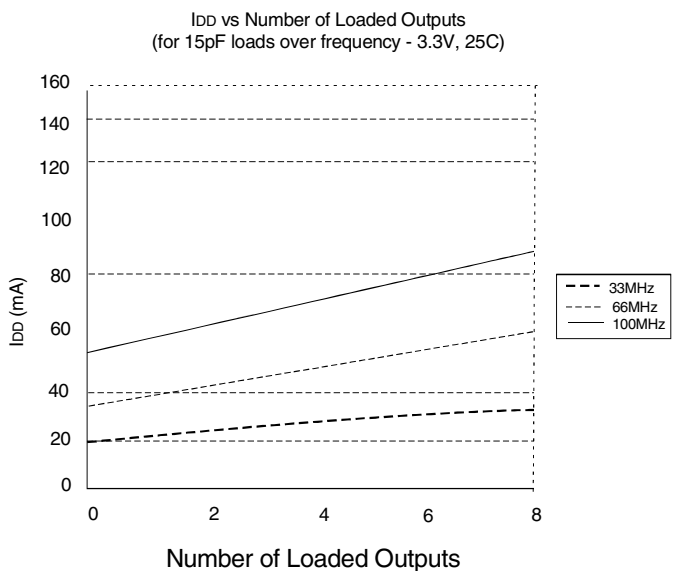
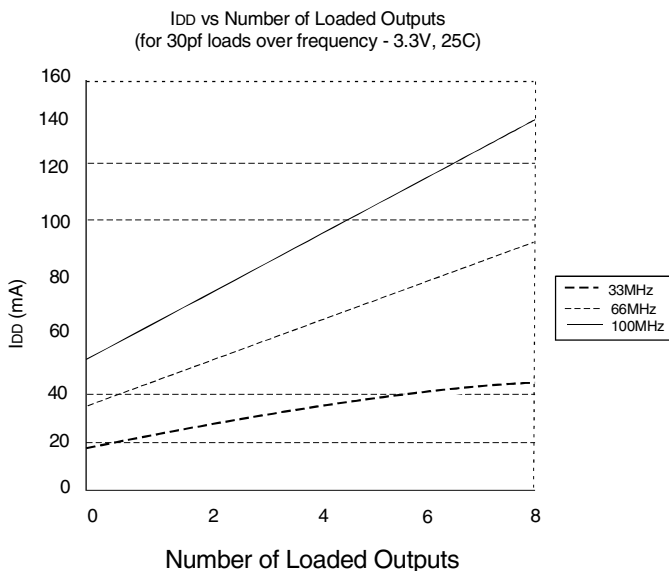
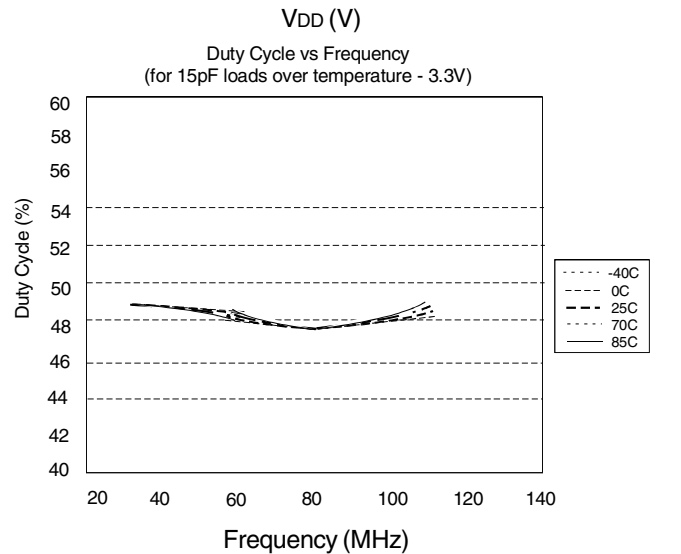
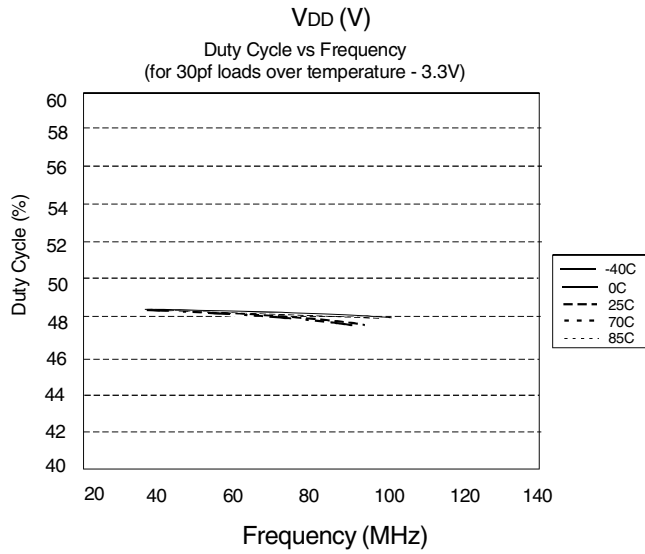
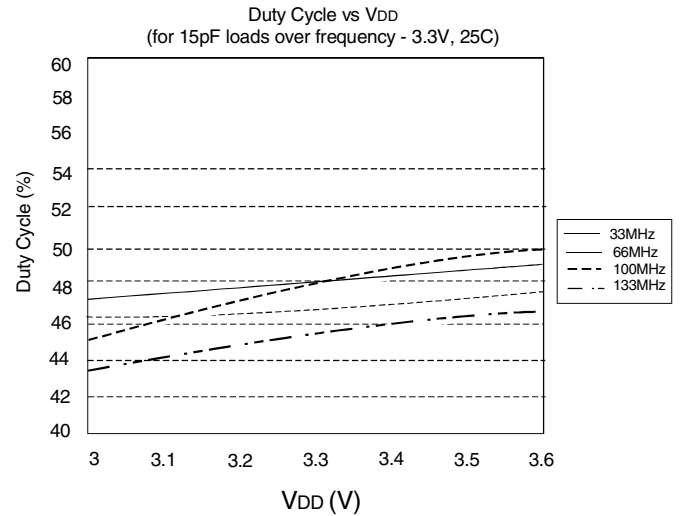
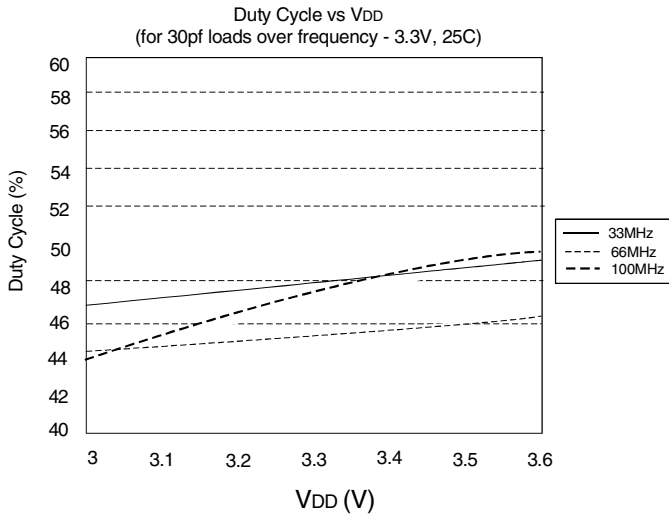
TYPICAL DUTY CYCLE⁽¹⁾ AND I_{DD} TRENDS⁽²⁾ FOR IDT2308-1, 2, 3, AND 4



NOTES:

- Duty Cycle is taken from typical chip measured at 1.4V.
- I_{DD} data is calculated from I_{DD} = I_{CORE} + nCVf, where I_{CORE} is the Unloaded Current (n = Number of Outputs; C = Capacitance Load per Output (F); V = Voltage Supply(V); f = Frequency (Hz)).

TYPICAL DUTY CYCLE⁽¹⁾ AND I_{DD} TRENDS⁽²⁾ FOR IDT2308-1H, -2H, AND -5H

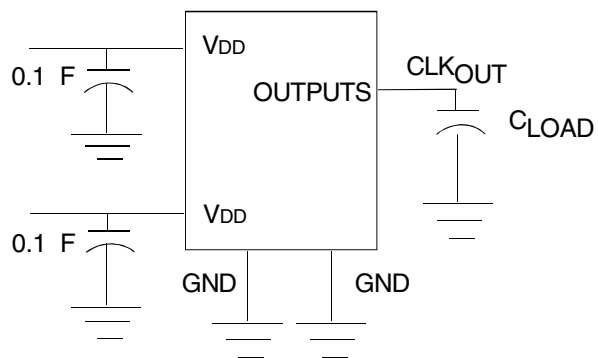


NOTES:

1. Duty Cycle is taken from typical chip measured at 1.4V.
2. I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the Unloaded Current (n = Number of Outputs; C = Capacitance Load per Output (F); V = Voltage Supply(V); f = Frequency (Hz)).

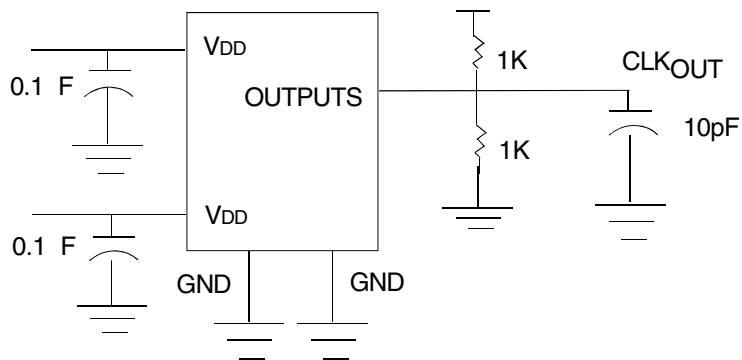
TEST CIRCUITS

TEST CIRCUIT 1



Test Circuit for all Parameters Except t_8

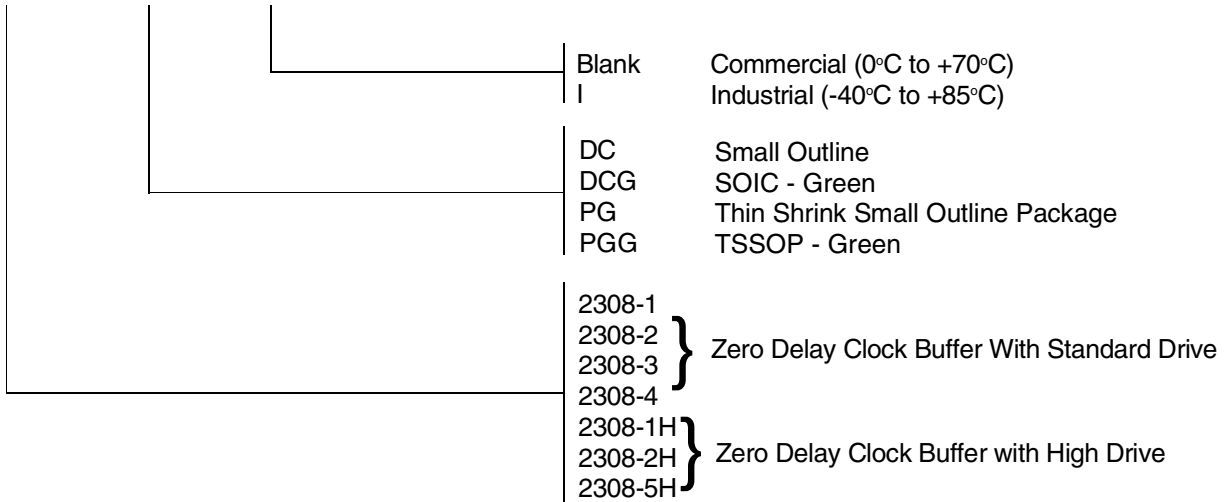
TEST CIRCUIT 1



Test Circuit for t_8 , Output Slew Rate On -1H, -2H, and -5H Device

ORDERING INFORMATION

IDT XXXXX XX X
 Device Type Package Process



***NOTE: EOL for non-green parts to occur on 5/13/10 per PDNU-09-01**

| Ordering Code | Package Type | Operating Range |
|----------------|--------------|-----------------|
| IDT2308-1DC* | 16-Pin SOIC | Commercial |
| IDT2308-1DCI* | 16-Pin SOIC | Industrial |
| IDT2308-1HDC* | 16-Pin SOIC | Commercial |
| IDT2308-1HDCG | 16-Pin SOIC | Commercial |
| IDT2308-1HDCI* | 16-Pin SOIC | Industrial |
| IDT2308-1HPG | 16-Pin TSSOP | Commercial |
| IDT2308-1HPGI | 16-Pin TSSOP | Industrial |
| IDT2308-2DC* | 16-Pin SOIC | Commercial |
| IDT2308-2DCG | 16-Pin SOIC | Commercial |
| IDT2308-2DCI* | 16-Pin SOIC | Industrial |
| IDT2308-2DCGI | 16-Pin SOIC | Industrial |
| IDT2308-2HDC* | 16-Pin SOIC | Commercial |
| IDT2308-2HDCI* | 16-Pin SOIC | Industrial |
| IDT2308-3DC* | 16-Pin SOIC | Commercial |
| IDT2308-3DCI* | 16-Pin SOIC | Industrial |
| IDT2308-4DC* | 16-Pin SOIC | Commercial |
| IDT2308-4DCI* | 16-Pin SOIC | Industrial |
| IDT2308-5HDC* | 16-Pin SOIC | Commercial |
| IDT2308-5HDCI* | 16-Pin SOIC | Industrial |
| IDT2308-5HPG | 16-Pin TSSOP | Commercial |
| IDT2308-5HPGI | 16-Pin TSSOP | Industrial |



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