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FRAME RATE COMMUNICATIONS PLL

MK1574-01A/B

Description

The MK1574-01A/B are Phase-Locked Loop (PLL) based clock synthesizers, which accept an 8 kHz clock input as a reference, and generate many popular communications frequencies. All outputs are frequency locked together and to the input. This allows for the generation of locked clocks to the 8 kHz backplane clock, simplifying clock generation and distribution in communications systems.

- 1) MK1574-01A — 5 V operation
- 2) MK1574-01B — 3.3 V operation

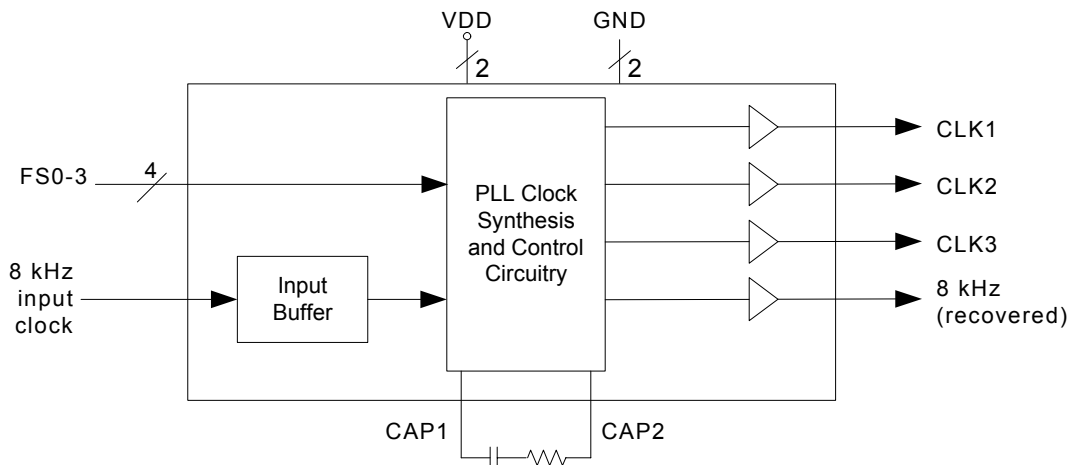
IDT manufactures the largest variety of clock generators and buffers, and can customize this device for a variety of frequencies.

Features

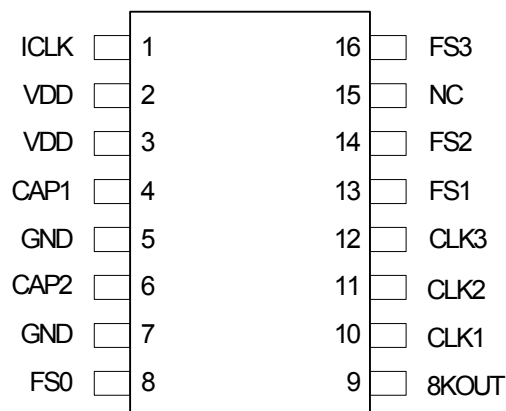
- Packaged in 16-pin SOIC
- Accepts 8 kHz input clock
- Output clock rates include T1, E1, T2, E2
- Available in commercial (0° to + 70°C) or industrial (-40 to +85°C) temperature ranges
- For jitter attenuation, use the MK2049

**NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

Block Diagram



## Pin Assignment



## Output Clocks Decoding Table

| Decode | Address | ICLK     | Multiplier | CLK1     | CLK2     | CLK3     |
|--------|---------|----------|------------|----------|----------|----------|
| FS3:0  | (Hex)   | pin1     | On-chip    | pin 10   | pin 11   | pin 12   |
| 0000   | 0       | Reserved | Reserved   | Reserved | Reserved | Reserved |
| 0001   | 1       | Reserved | Reserved   | Reserved | Reserved | Reserved |
| 0010   | 2       | Reserved | Reserved   | Reserved | Reserved | Reserved |
| 0011   | 3       | Reserved | Reserved   | Reserved | Reserved | Reserved |
| 0100   | 4       | 8.00 kHz | 2940       | 23.52    | 11.76    | 5.88     |
| 0101   | 5       | 8.00 kHz | 1960       | 15.68    | 7.84     | 3.92     |
| 0110   | 6       | 8.00 kHz | 2760       | 22.08    | 11.04    | 5.52     |
| 0111   | 7       | 8.00 kHz | 2640       | 21.12    | 10.56    | 5.28     |
| 1000   | 8       | 8.00 kHz | 1920       | 15.36    | 7.68     | 3.84     |
| 1001   | 9       | 8.00 kHz | 6480       | 51.84    | 25.92    | 12.96    |
| 1010   | A       | 8.00 kHz | 2112       | 16.896   | 8.448    | 4.224    |
| 1011   | B       | 8.00 kHz | 1578       | 12.624   | 6.312    | 3.156    |
| 1100   | C       | 8.00 kHz | 8192       | 65.536   | 32.768   | 16.384   |
| 1101   | D       | 8.00 kHz | 6176       | 49.408   | 24.704   | 12.352   |
| 1110   | E       | 8.00 kHz | 1024       | 8.192    | 4.096    | 2.048    |
| 1111   | F       | 8.00 kHz | 772        | 60176    | 3.088    | 1.544    |

0 = connect directly to ground, 1 = connect directly to VDD.

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description   |
|------------|----------|----------|---|
| 1          | ICLK     | Input    | Clock input. Connect to an 8 kHz clock input.   |
| 2          | VDD      | Power    | Connect to 3.3 V for 1574-01B, Connect to 5 V for 1574-01A.   |
| 3          | VDD      | Power    | Connect to 3.3 V for 1574-01B, Connect to 5 V for 1574-01A.   |
| 4          | CAP1     | Input    | Connect to a ceramic capacitor and a resistor in series between this pin and CAP2. Refer to the section “Loop Bandwidth and Loop Filter Component Selection”. |
| 5          | GND      | Power    | Connect to ground.  |
| 6          | CAP2     | Power    | Connect to a ceramic capacitor and a resistor in series between this pin and CAP1. Refer to the section “Loop Bandwidth and Loop Filter Component Selection”. |
| 7          | GND      | Power    | Connect to ground.  |
| 8          | FS0      | Input    | Frequency select 0. Determines CLK outputs per table above.   |
| 9          | 8KOUT    | Output   | Recovered 8 kHz output clock. Can be low jitter, better duty cycle than clock input.  |
| 10         | CLK1     | Output   | Clock 1 determined by status of FS3:0 per table above.  |
| 11         | CLK2     | Output   | Clock 2 determined by status of FS3:0 per table above.  |
| 12         | CLK3     | Output   | Clock 3 determined by status of FS3:0 per table above.  |
| 13         | FS1      | Input    | Frequency select 1. Determines CLK outputs per table above.   |
| 14         | FS2      | Input    | Frequency select 2. Determines CLK outputs per table above.   |
| 15         | NC       | —        | No connect. Do not connect anything to this pin.  |
| 16         | FS3      | Input    | Frequency select 3. Determines CLK outputs per table above.   |

## External Components

The MK1574-01A/B requires a minimum number of external components for proper operation. An RC network (see the section “Loop Bandwidth and Loop Filter Component Selection”) should be connected between CAP1 and CAP2 as close to the device as possible. Decoupling capacitors of 0.01 $\mu$ F should be connected between VDD and GND on pins 2, 3, 5 and 7, as close to the device as possible. A series termination resistor of 33 $\Omega$  may be used close to each clock output pin to reduce reflections.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1574-01A/B. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                                       | Rating              |
|--|---------------------|
| Supply Voltage, VDD (referenced to GND)    | -0.5 V to 7 V       |
| All Inputs and Outputs                     | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature (commercial) | 0 to +70° C         |
| Ambient Operating Temperature (industrial) | -40 to +85° C       |
| Storage Temperature                        | -65 to +150° C      |
| Junction Temperature                       | 150° C              |
| Soldering Temperature                      | 260° C              |

## Recommended Operation Conditions

| Parameter   | Min.  | Typ. | Max. | Units |
|---|-------|------|------|-------|
| Ambient Operating Temperature (commercial)        | 0     |      | +70  | °C    |
| Ambient Operating Temperature (industrial)        | -40   |      | +85  | °C    |
| Power Supply Voltage (measured in respect to GND) | +3.13 |      | +5.5 | V     |

## DC Electrical Characteristics

### MK1574-01A

VDD = 5 V, Ambient temperature 0 to +70° C, unless stated otherwise

| Parameter                | Symbol          | Conditions               | Min.    | Typ. | Max. | Units |
|--------------------------|-----------------|--------------------------|---------|------|------|-------|
| Operating Voltage        | VDD             |                          | 4.5     |      | 5.5  | V     |
| Input High Voltage       | V <sub>IH</sub> |                          | 2       |      |      | V     |
| Input Low Voltage        | V <sub>IL</sub> |                          |         |      | 0.8  | V     |
| Output High Voltage      | V <sub>OH</sub> | I <sub>OH</sub> = -4 mA  | VDD-0.4 |      |      | V     |
| Output High Voltage      | V <sub>OH</sub> | I <sub>OH</sub> = -25 mA | 2.4     |      |      | V     |
| Output Low Voltage       | V <sub>OL</sub> | I <sub>OL</sub> = 25 mA  |         |      | 0.4  | V     |
| Operating Supply Current | IDD             | No Load                  |         | 15   |      | mA    |
| Short Circuit Current    | I <sub>OS</sub> | Each output              |         | ±100 |      | mA    |
| Input Capacitance        | C <sub>IN</sub> |                          |         | 7    |      | pF    |

### MK1574-01B

VDD = 3.3 V, Ambient temperature 0 to +70° C, unless stated otherwise

| Parameter                | Symbol          | Conditions               | Min.    | Typ. | Max. | Units |
|--------------------------|-----------------|--------------------------|---------|------|------|-------|
| Operating Voltage        | VDD             |                          | 3.0     |      | 3.6  | V     |
| Input High Voltage       | V <sub>IH</sub> |                          | 2       |      |      | V     |
| Input Low Voltage        | V <sub>IL</sub> |                          |         |      | 0.8  | V     |
| Output High Voltage      | V <sub>OH</sub> | I <sub>OH</sub> = -4 mA  | VDD-0.4 |      |      | V     |
| Output High Voltage      | V <sub>OH</sub> | I <sub>OH</sub> = -25 mA | 2.4     |      |      | V     |
| Output Low Voltage       | V <sub>OL</sub> | I <sub>OL</sub> = 25 mA  |         |      | 0.4  | V     |
| Operating Supply Current | IDD             | No Load                  |         | 13   |      | mA    |
| Short Circuit Current    | I <sub>OS</sub> | Each output              |         | ±100 |      | mA    |
| Input Capacitance        | C <sub>IN</sub> |                          |         | 7    |      | pF    |

## AC Electrical Characteristics

### MK1574-01A

VDD = 5 V, Ambient Temperature 0 to +70°C, unless stated otherwise

| Parameter  | Symbol   | Conditions          | Min. | Typ.     | Max. | Units |
|--|----------|---------------------|------|----------|------|-------|
| Input Frequency                                    | $f_{IN}$ |                     |      | 8.000    |      | kHz   |
| Output Clock Rise Time                             | $t_{OR}$ | 0.8 to 2.0 V        |      |          | 1.5  | ns    |
| Output Clock Fall Time                             | $t_{OF}$ | 2.0 to 0.8 V        |      |          | 1.5  | ns    |
| Output Clock Duty Cycle, High time                 | $t_{DC}$ | At VDD/2            | 40   | 49 to 51 | 60   | %     |
| Absolute Clock Period Jitter                       |          |                     | 1    |          |      | ns    |
| Actual Mean Frequency Error Versus Target (note 1) |          | Any clock selection |      | 0        | 0    | ppm   |

### MK1574-01B

VDD = 3.3 V, Ambient Temperature 0 to +70°C, unless stated otherwise

| Parameter  | Symbol   | Conditions          | Min. | Typ.     | Max. | Units |
|--|----------|---------------------|------|----------|------|-------|
| Input Frequency                                    | $f_{IN}$ |                     |      | 8.000    |      | kHz   |
| Output Clock Rise Time                             | $t_{OR}$ | 0.8 to 2.0 V        |      |          | 1.5  | ns    |
| Output Clock Fall Time                             | $t_{OF}$ | 2.0 to 0.8 V        |      |          | 1.5  | ns    |
| Output Clock Duty Cycle, High time                 | $t_{DC}$ | At VDD/2            | 40   | 49 to 51 | 60   | %     |
| Absolute Clock Period Jitter                       |          |                     | 1    |          |      | ns    |
| Actual Mean Frequency Error Versus Target (note 1) |          | Any clock selection |      | 0        | 0    | ppm   |

Note 1: All multipliers as shown in the table on page two are exact, and are stored in ROM on the chip.

## Thermal Characteristics

| Parameter                              | Symbol        | Conditions     | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air      |      | 120  |      | °C/W  |
|  | $\theta_{JA}$ | 1 m/s air flow |      | 115  |      | °C/W  |
|  | $\theta_{JA}$ | 3 m/s air flow |      | 105  |      | °C/W  |
| Thermal Resistance Junction to Case    | $\theta_{JC}$ |                |      | 58   |      | °C/W  |

## Loop Bandwidth and Loop Filter Component Selection

The series-connected capacitor and resistor between CAP1 and CAP2 (pins 4 and 6) determine the dynamic characteristics of the phase-locked loop. The capacitor must have very low leakage, therefore a high quality ceramic capacitor is recommended. DO NOT use any type of polarized or electrolytic capacitor. The series connected capacitor and resistor between CAP1 and CAP2 (pins 4 and 6) determine the dynamic characteristics of the phase-locked loop. The capacitor must have very low leakage, therefore a high quality ceramic capacitor is recommended. DO NOT use any type of polarized or electrolytic capacitor. Ceramic capacitors should have COG or NP0 dielectric. Avoid high-K dielectrics like Z5U and X7R; these and other ceramics which have piezoelectric properties allow mechanical vibration in the system to increase the output jitter because the mechanical energy is converted directly to voltage noise on the VCO input.

The values of the RC network determine the bandwidth of the PLL. The values of the loop filter components are calculated using the constants K1 and K2 from the Loop Filter Constants table (page 7). The loop bandwidth is set by the capacitor C and the constant K1 using the formula:

$$BW \text{ (Hz)} = \frac{K1}{\sqrt{C}} \quad \text{Equation 1}$$

The loop damping is set by the resistor R, the capacitor C, and the constant K2 using the formula::

$$R = \frac{\zeta * K2}{\sqrt{C}} \quad \text{Equation 2; } \zeta \text{ (zeta) is the damping factor}$$

For example, to design the loop filter whewn generating 8.192 MHz from 8 kHz:

1. From the Output Clock Decoding table (page 2), the address is E. The Loop Filter Constants table (page 7) shows the constants K1 = 0.0516 and K2 = 6.2.
2. A good value for the loop bandwidth is 1/20 the input frequency; where 8 kHz/20 = 400 Hz. Using equation 1,

$$400 = \frac{K1}{\sqrt{C}}$$

Therefore,

$$C = \left( \frac{0.0516}{400} \right)^2 = 16.6 \text{ nF (16 nF nearest standard value)}$$

3. A good value for the damping factor  $\zeta$  is 0.707. From equation 2,

$$R = \frac{0.707 * 6.2}{\sqrt{16E-9}} = 34.7 \text{ k}\Omega \text{ (36 k}\Omega \text{ nearest standard value)}$$



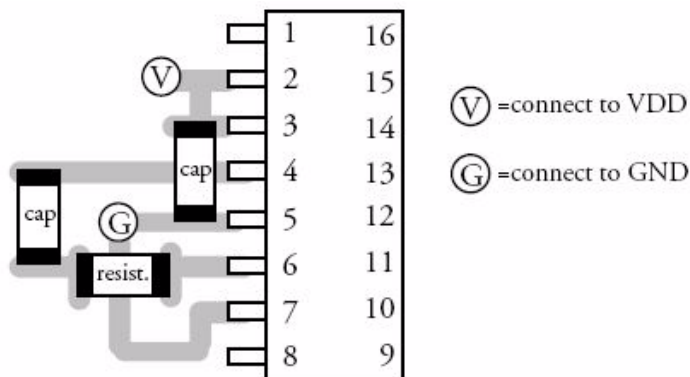
## Loop Filter Constants

This table shows the constants K1 and K2 that are used with the equations on page 6 to calculate the external loop filter components. Loop Filter Constants for MK1574-01A

| Decode | Address | Loop Filter Constants |          |
|--------|---------|-----------------------|----------|
| FS3:0  | (Hex)   | K1                    | K2       |
| 0000   | 0       | Reserved              | Reserved |
| 0001   | 1       | Reserved              | Reserved |
| 0010   | 2       | Reserved              | Reserved |
| 0011   | 3       | Reserved              | Reserved |
| 0100   | 4       | 0.0430                | 7.4      |
| 0101   | 5       | 0.0527                | 6.0      |
| 0110   | 6       | 0.0444                | 7.2      |
| 0111   | 7       | 0.0454                | 7.0      |
| 1000   | 8       | 0.0533                | 6.0      |
| 1001   | 9       | 0.0410                | 7.8      |
| 1010   | A       | 0.0508                | 6.3      |
| 1011   | B       | 0.0587                | 5.4      |
| 1100   | C       | 0.0365                | 8.7      |
| 1101   | D       | 0.0420                | 7.6      |
| 1110   | E       | 0.0516                | 6.2      |
| 1111   | F       | 0.0594                | 5.4      |

## PC Board Layout

A proper board layout is critical to the successful use of the MK1574-01A/B. In particular, the CAP1 and CAP2 pins are very sensitive to noise and leakage (CAP1 at pin 4 is the most sensitive). Traces must be as short as possible and the capacitor and resistor must be mounted next to the device as shown to the right. The capacitor connected between pins 3 and 5 is the power supply decoupling capacitor. The high frequency output clocks on may benefit from a series 33Ω resistor connected close to the pin (not shown).

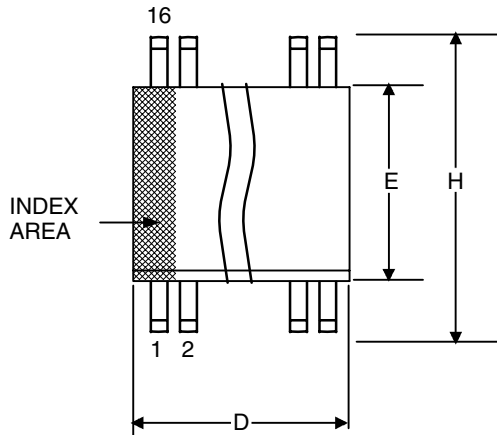


## Clock Multipliers/Accuracies

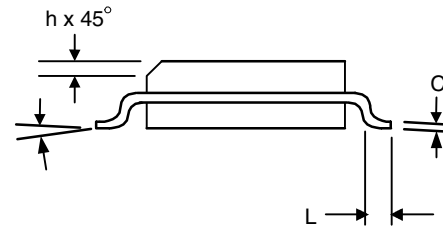
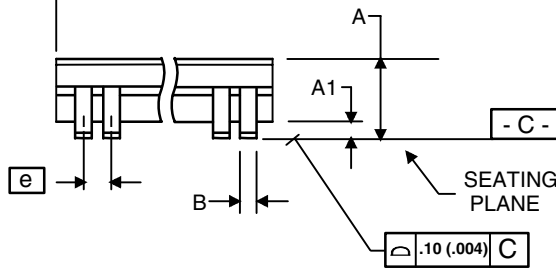
In the table on page 2 are the actual multipliers stored in the MK1574-01A/B ROM, which yield the exact values shown for the output clocks.

### Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol   | Millimeters |       | Inches      |       |
|----------|-------------|-------|-------------|-------|
|          | Min         | Max   | Min         | Max   |
| A        | 1.35        | 1.75  | .0532       | .0688 |
| A1       | 0.10        | 0.25  | .0040       | .0098 |
| B        | 0.33        | 0.51  | .013        | .020  |
| C        | 0.19        | 0.25  | .0075       | .0098 |
| D        | 9.80        | 10.00 | .3859       | .3937 |
| E        | 3.80        | 4.00  | .1497       | .1574 |
| e        | 1.27 BASIC  |       | 0.050 BASIC |       |
| H        | 5.80        | 6.20  | .2284       | .2440 |
| h        | 0.25        | 0.50  | .010        | .020  |
| L        | 0.40        | 1.27  | .016        | .050  |
| $\alpha$ | 0°          | 8°    | 0°          | 8°    |



## Ordering Information

| Part / Order Number | Marking      | Shipping Packaging | Package     | Temperature   |
|---------------------|--------------|--------------------|-------------|---------------|
| MK1574-01AS*        | MK1574-01AS  | Tubes              | 16-pin SOIC | 0 to +70° C   |
| MK1574-01ASTR*      | MK1574-01AS  | Tape and Reel      | 16-pin SOIC | 0 to +70° C   |
| MK1574-01ASI*       | MK1574-01ASI | Tubes              | 16-pin SOIC | -40 to +85° C |
| MK1574-01ASITR*     | MK1574-01ASI | Tape and Reel      | 16-pin SOIC | -40 to +85° C |
| MK1574-01BS*        | MK1574-01BS  | Tubes              | 16-pin SOIC | 0 to +70° C   |
| MK1574-01BSTR*      | MK1574-01BS  | Tape and Reel      | 16-pin SOIC | 0 to +70° C   |
| MK1574-01BSI*       | MK1574-01BSI | Tubes              | 16-pin SOIC | -40 to +85° C |
| MK1574-01BSITR*     | MK1574-01BSI | Tape and Reel      | 16-pin SOIC | -40 to +85° C |
| MK1574-01BSILF      | 157401BSILF  | Tubes              | 16-pin SOIC | -40 to +85° C |
| MK1574-01BSILFTR    | 157401BSILF  | Tape and Reel      | 16-pin SOIC | -40 to +85° C |

**\*NOTE: EOL of non-green parts to occur on 5/13/10 per PDN U-09-01.**

**Parts ordered with an "LF" suffix to the part number are the Pb-free configuration and RoHS compliant.**

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