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LOW EMI CLOCK GENERATOR

MK1707D

Description

The MK1707D generates a low EMI output clock from a crystal clock input. The part is designed to dither the LCD interface clock for flat panel graphics controllers. The device uses ICS' proprietary mix of analog and digital Phase-Locked Loop (PLL) technology to spread the frequency spectrum of the output, thereby reducing the frequency amplitude peaks by several dB.

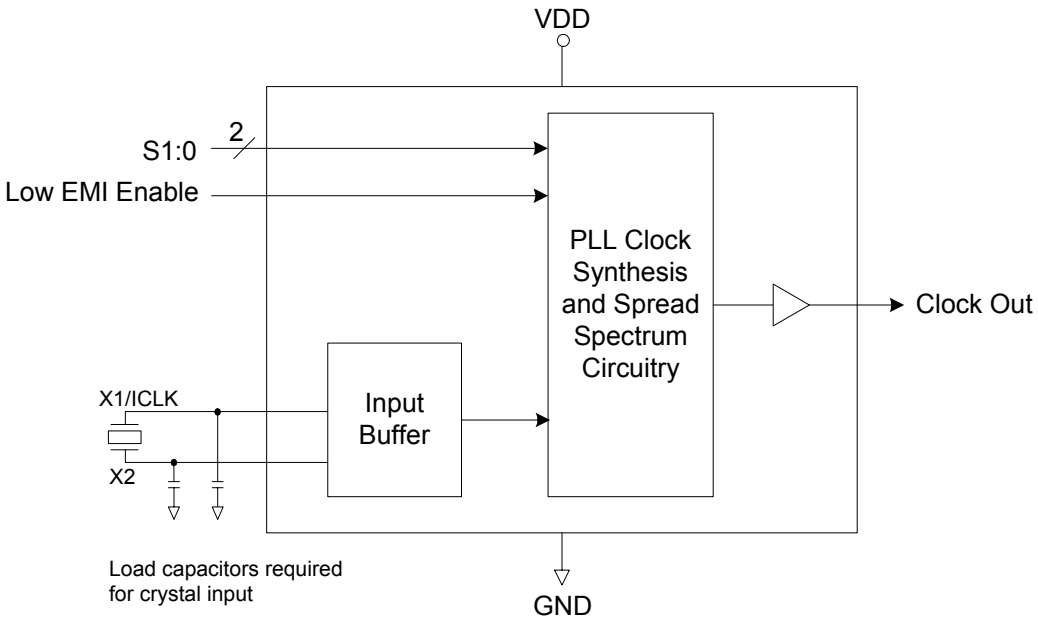
The MK1707D offers centered spread from a wide range of input clock frequencies.

ICS offers many other clocks for computers and computer peripherals. Consult ICS when you need to replace multiple crystals and oscillators from your board.

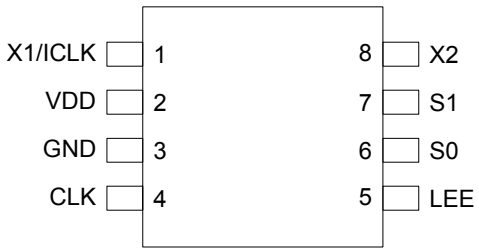
Features

- Packaged in 8-pin SOIC
- Available in Pb (lead) free package
- Provides a spread spectrum output clock
- Supports flat panel controllers
- Accepts a crystal or clock input to provide same frequency dithered output
- Input operating frequencies of 25-54 and 50-108 MHz
- Peak reduction by 7dB to 14dB typical on 3rd through 19th odd harmonics
- Low EMI feature can be disabled
- Includes power down
- Operating voltage of 3.3 V
- Industrial temperature range available
- Advanced, low-power CMOS process

Block Diagram



Pin Assignment



8 pin (150 mil) SOIC

Spread Selection Table (MHz)

S1 Pin 7	S0 Pin 6	Spread Direction	Spread (%)	Input Frequency
0	0	Center	±1.15	25-54
0	M	Center	±0.95	25-54
0	1	Center	±1.9	50-108
1	0	Center	±1.6	25-54
1	M	Center	±1.9	25-54
1	1	Center	±0.6	50-108

0 = connect to GND
M = unconnected (floating) has internal resistor network
Leave it open (unconnected)
1 = connect to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	Input	Crystal connection. Connect crystal or clock input.
2	VDD	Power	Connect to +3.3 V.
3	GND	Power	Connect to ground.
4	CLK	Output	Spread spectrum clock output per table above.
5	LEE	Input	Low EMI enable. Turns on spread spectrum when high. Internal pull-up resistor. Disables the spread spectrum feature when low.
6	S0	Input	Function select input. Selects spread amount and direction per table above. Internal mid-level.
7	S1	Input	Function select 1 input. Selects spread amount and direction per table above. Internal mid-level.
8	X2	XO	Crystal connection. Leave unconnected for clock input.

External Components

The MK1707D requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD and GND on pins 2 and 3, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output and the load is over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Select Pin Operation

The S1, S0 select pins are 2-level, meaning they have three separate states to make the selections shown in the table on page 2.

PCB layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the MK1707D. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1707D. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70°C
Ambient Operating Temperature (industrial)	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0		+70	°C
Ambient Operating Temperature (industrial)	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.135	3.3	+3.465	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135	3.3	3.465	V
Input Low Voltage	V_{IL}	S0, S1 pins			0.5	V
Input High Voltage	V_{IH}	S0, S1 pins	2.7			V
Supply Current	IDD	No load, at 3.3 V		20		mA
Input High Voltage	V_{IH}	LEE pins	2.0			V
Input Low Voltage	V_{IL}	LEE pins			0.5	V
Output High Voltage	V_{OH}	CMOS, I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = -12 mA			0.4	V
Input Capacitance	C_{IN}	S0, S1, LEE pins		5		pF

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

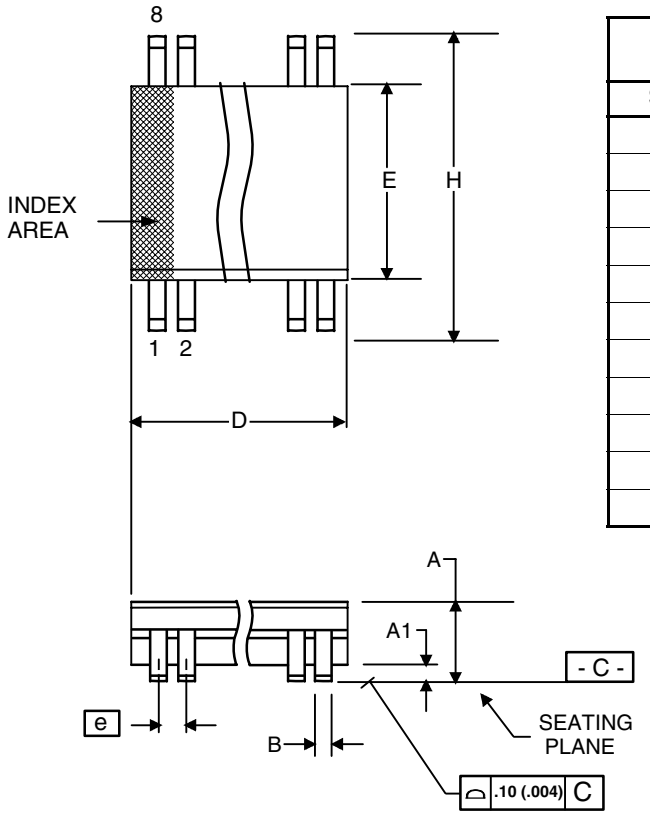
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input/Output Clock Frequency			25		108	MHz
Input Clock Duty Cycle		Time above VDD/2	20		80	%
Output Clock Duty Cycle		Time above 1.5 V	40	50	60	%
Output Rise Time	t_{OR}	0.8 to 2.0 V		1.5		ns
Output Fall Time	t_{OF}	2.0 to 0.8 V		1.5		ns
EMI Peak Frequency Reduction		3rd through 19th odd harmonics		7 to 14		dB

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK1707D	MK1707D	Tubes	8-pin SOIC	0 to +70° C
MK1707DTR	MK1707D	Tape and Reel	8-pin SOIC	0 to +70° C
MK1707DLF	1707DLF	Tubes	8-pin SOIC	0 to +70° C
MK1707DLFTR	1707DLF	Tape and Reel	8-pin SOIC	0 to +70° C
MK1707DI	1707DI	Tubes	8-pin SOIC	-40 to +85° C
MK1707DITR	1707DI	Tape and Reel	8-pin SOIC	-40 to +85° C
MK1707DILF	1707DIL	Tubes	8-pin SOIC	-40 to +85° C
MK1707DILFTR	1707DIL	Tape and Reel	8-pin SOIC	-40 to +85° C

“LF” denotes Pb (lead) free packaging.

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800-345-7015
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Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339

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