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# SPREAD SPECTRUM MULTIPLIER CLOCK
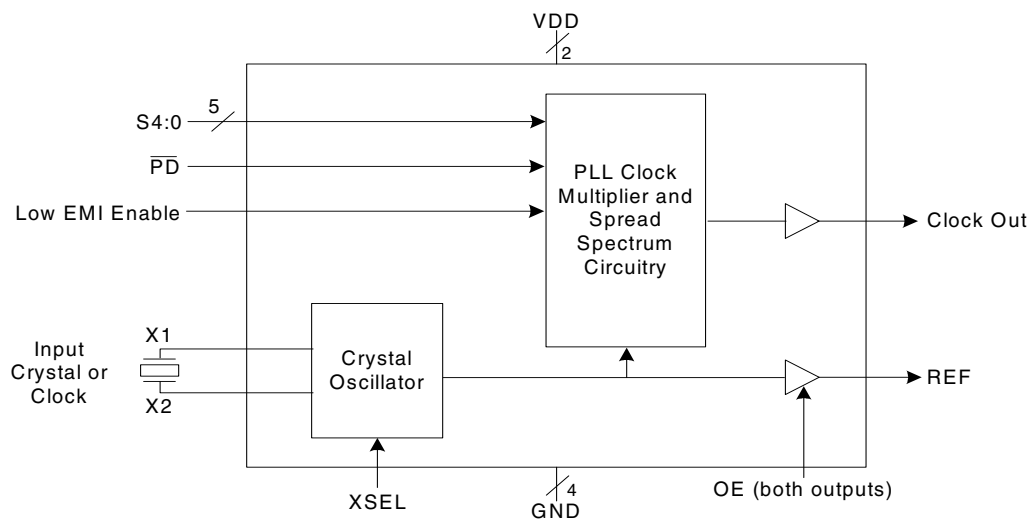
# MK1714-02

## Description

The MK1714-02 is a low cost, high performance clock synthesizer with selectable multipliers and percentages of spread designed to generate high frequency clocks with low EMI. Using analog/digital Phase Locked Loop (PLL) techniques, the device accepts an inexpensive, fundamental mode, parallel resonant crystal or clock input to produce a spread or dithered output. This reduces the EMI amplitude peaks at the odd harmonics by several dB. The OE pin puts both outputs into a high impedance state for board level testing. The $\overline{PD}$ pin powers down the entire chip and the outputs are held low.
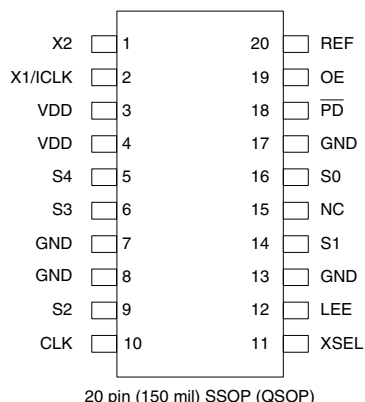
## Features

- Packaged in 20-pin tiny SSOP
- Available in Pb (lead) free package
- Operating voltage of 3.3 V or 5 V
- Multiplier modes of x1, x2, x3, x4, x5, and x6
- Inexpensive 10 - 25 MHz crystal or clock input
- OE pin tri-states the outputs for board testing
- Power down pin stops the outputs low
- Selectable frequency spread
- Spread can be turned on or off
- Advanced, low power CMOS process
- Duty cycle of 40/60
- Industrial temperature range available

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01***

## Block Diagram

# Pin Assignment

```
            X2  ▢ 1        20 ▢  REF
       X1/ICLK  ▢ 2        19 ▢  OE
           VDD  ▢ 3        18 ▢  PD
           VDD  ▢ 4        17 ▢  GND
            S4  ▢ 5        16 ▢  S0
            S3  ▢ 6        15 ▢  NC
           GND  ▢ 7        14 ▢  S1
           GND  ▢ 8        13 ▢  GND
            S2  ▢ 9        12 ▢  LEE
           CLK  ▢ 10       11 ▢  XSEL
```
20 pin (150 mil) SSOP (QSOP)

# Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | X2 | XO | Crystal connection. Connect to parallel mode crystal. Leave open for clock. |
| 2 | X1 | XI | Crystal connection. Connect to parallel mode crystal or clock. |
| 3 | VDD | Power | Connect to VDD. Must be same value as other VDD. |
| 4 | VDD | Power | Connect to VDD. Must be same value as other VDD. |
| 5 | S4 | Input | Select pin 4. Determines multiplier and spread amount per table on following page. Internal pull-down. |
| 6 | S3 | Input | Select pin 3. Determines multiplier and spread amount per table on following page. Internal pull-up. |
| 7 | GND | Power | Connect to ground. |
| 8 | GND | Power | Connect to ground. |
| 9 | S2 | Input | Select pin 2. Determines multiplier and spread amount per table on following page. Internal pull-up. |
| 10 | CLK | Output | Clock output dependent on input, multiplier, and spread amount per table on following page. |
| 11 | XSEL | Input | Connect to VDD for crystal input, or GND for CLK input. Internal pull-down. |
| 12 | LEE | Input | Low EMI Enable. Turns on spread spectrum on CLK when high. Internal pull-up. |
| 13 | GND | Power | Connect to ground. |
| 14 | S1 | Input | Select pin 1. Determines multiplier and spread amount per table on following page. Internal pull-up. |
| 17 | GND | Power | Connect to ground. |
| 18 | $\overline{PD}$ | Input | Power down. Turns off chip when low. Outputs stop low. Leave open or connected to VDD if power down is not required. |
| 19 | OE | Input | Output enable. Tri-states all outputs when low. Internal pull-up. |
| 20 | REF | Output | Reference clock output from crystal oscillator. This clock is not spread. |

Note: When changing the input frequency, the LEE pin must be set low for minimum of 10µs to allow the PLL to lock to the new frequency. Alternatively, the $\overline{PD}$ pin may be set low while changing frequencies.

# Clock Output Select Table (MHz)

| S4 | S3 | S2 | S1 | S0 | Input Range | Multiplier | Output Range | Direction | Amount (%) | 3.3/5V |
|----|----|----|----|----|-------------|------------|--------------|-----------|------------|--------|
| 0 | 0 | 0 | 0 | 0 | 40 - 80 | x1 | 40 - 80 | C | ±0.75 | Both |
| 0 | 0 | 0 | 0 | 1 | 60 - 120 | x1 | 60 -120 | DC | +0.25, -0.75 | Both |
| 0 | 0 | 0 | 1 | 0 | 40 - 80 | x1 | 40 - 80 | C | ±1.25 | Both |
| 0 | 0 | 0 | 1 | 1 | 80 - 150 | x1 | 80 - 150 | C | ±0.75 | Both |
| 0 | 0 | 1 | 0 | 0 | 10 - 30 | x2 | 20 - 60 | C | ±0.75 | Both |
| 0 | 0 | 1 | 0 | 1 | 20 - 60 | x2 | 40 - 120 | C | ±0.5 | Both |
| 0 | 0 | 1 | 1 | 0 | 10 - 25 | x2 | 20 - 50 | DC | +0.25, -1.5 | Both |
| 0 | 0 | 1 | 1 | 1 | 20 - 60 | x2 | 40 - 120 | DC | +0.5, -1 | Both |
| 0 | 1 | 0 | 0 | 0 | 20 - 30 | x3 | 60 - 90 | C | ±0.5 | Both |
| 0 | 1 | 0 | 0 | 1 | 40 - 75 | x2 | 80 - 150 | C | ±0.75 | Both |
| 0 | 1 | 0 | 1 | 0 | 40 - 100 | x1 | 40 - 100 | DC | +0.25, -1.5 | Both |
| 0 | 1 | 0 | 1 | 1 | 40 - 75 | x2 | 80 - 150 | DC | +0.25, -1.5 | Both |
| 0 | 1 | 1 | 0 | 0 | 20 - 40 | x1 | 20 - 40 | DC | +0.5, -2.0 | 3.3V |
| 0 | 1 | 1 | 0 | 1 | 20 - 60 | x1 | 20 - 60 | DC | +0.25, -1.5 | Both |
| 0 | 1 | 1 | 1 | 0 | 10 - 20 | x1 | 10 - 20 | DC | +0.5, -2.0 | Both |
| 0 | 1 | 1 | 1 | 1 | 10 - 30 | x1 | 10 - 30 | DC | +0.25, -1.5 | Both |
| 1 | 0 | 0 | 0 | 0 | 20 - 37.5 | x4 | 80 - 150 | DC | +0.25, -1.25 | Both |
| 1 | 0 | 0 | 0 | 1 | 20 - 40 | x3 | 60 - 120 | DC | +0.25, -1.5 | Both |
| 1 | 0 | 0 | 1 | 0 | 10 - 30 | x1 | 10 - 30 | C | ±0.75 | Both |
| 1 | 0 | 0 | 1 | 1 | 20 - 30 | x1 | 20 - 30 | D | -0.5 | Both |
| 1 | 0 | 1 | 0 | 0 | 5 - 20 | x2 | 10 - 40 | DC | +0.25, -2.25 | 3.3V |
| 1 | 0 | 1 | 0 | 1 | 20 - 50 | x3 | 60 - 150 | D | -0.25, -2.25 | Both |
| 1 | 0 | 1 | 1 | 0 | 20 - 37.5 | x4 | 80 - 150 | C | ±0.75 | Both |
| 1 | 0 | 1 | 1 | 1 | 80 - 150 | x1 | 80 - 150 | DC | +0.25, -1.25 | Both |
| 1 | 1 | 0 | 0 | 0 | 10 - 25 | x4 | 40 - 100 | C | ±0.75 | Both |
| 1 | 1 | 0 | 0 | 1 | 10 - 20 | x5 | 50 - 100 | C | ±0.75 | Both |
| 1 | 1 | 0 | 1 | 0 | 10 - 20 | x6 | 60 - 120 | C | ±0.75 | Both |
| 1 | 1 | 0 | 1 | 1 | 20 - 50 | x1 | 20 - 50 | C | ±0.75 | Both |
| 1 | 1 | 1 | 0 | 0 | 10 - 25 | x4 | 40 - 100 | DC | +0.25, -1.5 | Both |
| 1 | 1 | 1 | 0 | 1 | 10 - 20 | x5 | 50 - 100 | DC | +0.25, -1.25 | Both |
| 1 | 1 | 1 | 1 | 0 | 10 - 20 | x6 | 60 - 120 | D | -1.5 | Both |
| 1 | 1 | 1 | 1 | 1 | 10 - 30 | x1 | 10 - 30 | C | ±0.75 | Both |

For S4:S0, 0 = connect to GND, 1 = connect to VDD.

Direction: C = center spread, D = down spread, DC = down + center spread. Amount = spread amount. For example, for a 40 MHz output clock spread down 1%, the lowest frequency is 39.60 MHz.

**Contact IDT with your exact output frequency for details on spread direction and amount.**

# External Components

The MK1714-02 requires a minimum number of external components for proper operation.

## Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD and GND, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

## Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

## Crystal Tuning Load Capacitors

### Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) been the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal $(C_L-6)*2$. In this equation, $C_L$ = crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be

$[16 - 6]*2 = 20$ pF.

## PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the MK1714-02. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

## Powerup Considerations

To insure proper operation of the spread spectrum generation circuit, some precautions must be taken in the implementation of the MK1714-02.

1) An input signal should not be applied to ICLK until VDD is stable (within 10% of its final value). This requirement can be easily met by operating the MK1714-02 and the ICLK source from the same power supply.

2) LEE should not be enabled (taken high) until after the power supplies and input clock are stable. This requirement can be met by direct control of LEE by system logic; for example, a "power good" signal. Another solution is to leave LEE unconnected to anything but a 0.01µF capacitor to ground. The pull-up resistor on LEE will charge the capacitor and provide approximately a 700µs delay until spread spectrum is enabled.

3) If the input frequency is changed during operation, disable spread spectrum until the input clock stabilizes at the new frequency.

# Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1714-02. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage, VDD | 7V |
| All Inputs and Outputs | -0.5V to VDD+0.5V |
| Ambient Operating Temperature | -40 to +85° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 175° C |
| Soldering Temperature | 260° C |

# Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Ambient Operating Temperature | 0 | | +70 | ° C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | +5.5 | V |

# DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V or 5 V**, Ambient Temperature -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 3.0 | | 5.5 | V |
| Supply Current | IDD | No load, at 3.3 V | | 26 | | mA |
| | IDD | No load, at 5 V | | 40 | | mA |
| Input High Voltage | $V_{IH}$ | Select inputs, OE, $\overline{PD}$ | 2 | | | V |
| Input Low Voltage | $V_{IL}$ | Select inputs, OE, $\overline{PD}$ | | | 0.8 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -8 mA | VDD-0.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8 mA | | | 0.4 | V |
| Short Circuit Current | $I_{OS}$ | Each output | | ±50 | | mA |
| On Chip Pull-up Resistor, inputs | $R_{PU}$ | Except X1 | | 500 | | kΩ |
| On-Chip Pull-down Resistor, outputs | $R_{PD}$ | S4 pin only | | 500 | | kΩ |
| Input Capacitance | | Except X1, X2 | | 7 | | pF |

## AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V or 5 V**, Ambient Temperature -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input Crystal Frequency | | | 10 | | 25 | MHz |
| Input Clock Frequency | | | 10 | | 150 | MHz |
| Output Rise Time | $t_{OR}$ | 0.8 to 2.0 V | | | 1.5 | ns |
| Output Fall Time | $t_{OF}$ | 2.0 to 0.8 V | | | 1.5 | ns |
| One Sigma Jitter | | CLK | | 40 | | ps |
| Absolute Jitter | | CLK | | ±160 | | |
| Output Clock Duty Cycle | | at VDD/2 | 40 | 50 | 60 | % |
| Output Frequency | | | 2 | | 200 | MHz |
| Output Frequency Synthesis Error | | | | 1 | | ppm |

## Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air | | 135 | | ° C/W |
| | $\theta_{JA}$ | 1 m/s air flow | | 93 | | ° C/W |
| | $\theta_{JA}$ | 3 m/s air flow | | 78 | | ° C/W |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | | | 60 | | ° C/W |

# Package Outline and Package Dimensions (20 pin SSOP, 150 Mil. Body)
Package dimensions are kept current with JEDEC Publication No. 95
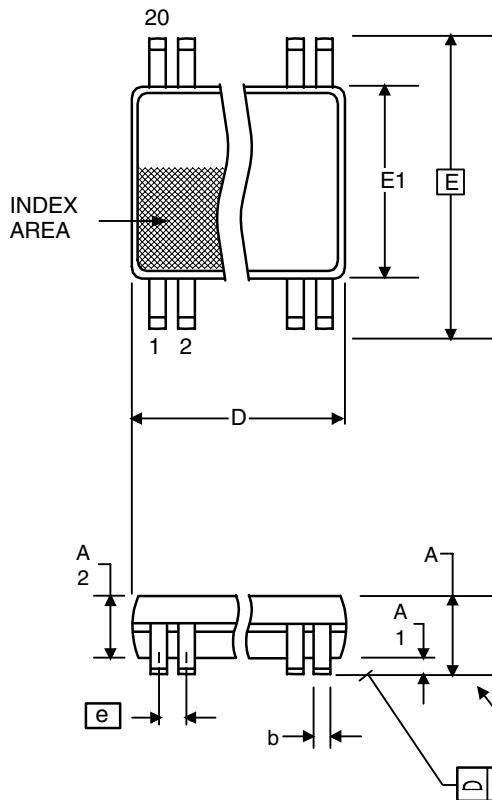


| Symbol | Millimeters | | Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | .053 | .069 |
| A1 | 0.10 | 0.25 | .0040 | .010 |
| A2 | -- | 1.50 | -- | .059 |
| b | 0.20 | 0.30 | 0.008 | 0.012 |
| C | 0.18 | 0.25 | .007 | .010 |
| D | 8.55 | 8.75 | .337 | .344 |
| E | 5.80 | 6.20 | .228 | .244 |
| E1 | 3.80 | 4.00 | .150 | .157 |
| e | 0.635 Basic | | 0.025 Basic | |
| L | 0.40 | 1.27 | .016 | .050 |
| α | 0° | 8° | 0° | 8° |

# Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---|---|---|---|---|
| MK1714-02R* | MK1714-02R | Tubes | 20-pin SSOP | 0 to +70° C |
| MK1714-01RTR* | MK1714-02R | Tape and Reel | 20-pin SSOP | 0 to +70° C |
| MK1714-02RI* | MK1714-02RI | Tubes | 20-pin SSOP | -40 to 85 ° C |
| MK1714-02RITR* | MK1714-02RI | Tape and Reel | 20-pin SSOP | -40 to 85 ° C |
| MK1714-02RLF | MK1714-02RL | Tubes | 20-pin SSOP | 0 to +70° C |
| MK1714-01RLFTR | MK1714-02RL | Tape and Reel | 20-pin SSOP | 0 to +70° C |
| MK1714-02RILF | MK171402RIL | Tubes | 20-pin SSOP | -40 to 85 ° C |
| MK1714-02RILFTR | MK171402RIL | Tape and Reel | 20-pin SSOP | -40 to 85 ° C |

**\*NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

**Parts that are ordered  with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.**

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