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VCXO PLUS AUDIO CLOCK FOR STB

MK3724

Description

The MK3724 is a low cost, low jitter, high performance VCXO and PLL clock synthesizer designed to replace expensive discrete VCXOs and multipliers. The patented on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3.3 V input voltage to cause the output clocks to vary by ±115 ppm. Using IDT's analog/digital Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 27 MHz pullable crystal input to produce a reference output and a selectable audio clock.

IDT manufactures the largest variety of VCXO based timing devices for all applications. Consult IDT to eliminate VCXOs, crystals, and oscillators from your board.

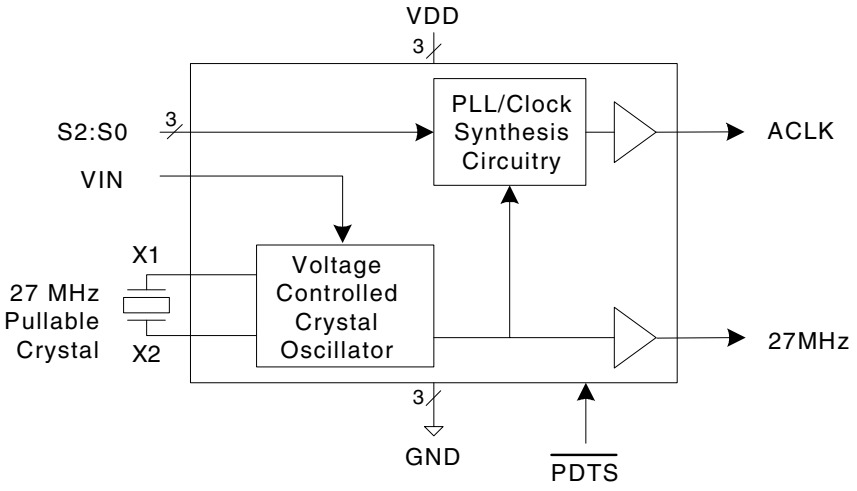
The frequency of the on-chip VCXO is adjusted by an external control voltage connected to VIN. Because VIN is a high impedance input, it can be driven directly from an PWM RC integrator circuit.

Features

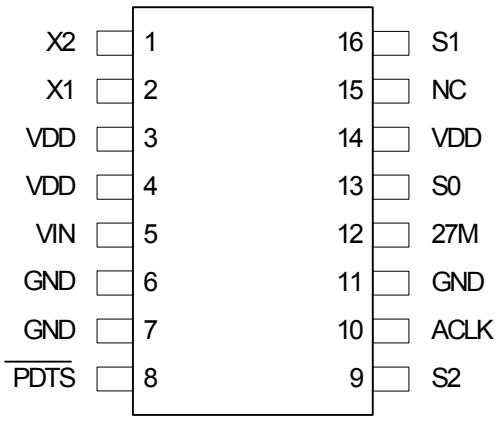
- Packaged in 16-pin TSSOP
- Available in Pb free packaging
- Replaces a VCXO and oscillator
- Operating voltage of 3.3 V
- Provides output of 27 MHz plus audio clock
- Uses an inexpensive 27 MHz pullable crystal
- On-chip patented VCXO with pull range of 230 ppm (minimum)
- VCXO tuning voltage of 0 to 3.3 V
- Advanced, low power, sub-micron CMOS process
- Industrial temperature range available
- For other standard audio frequencies see the MK3722

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-0

Block Diagram



Pin Assignment



16-pin TSSOP

Audio Clock Select Table

S2	S1	S0	ACLK (MHz)
0	0	0	3.072
0	0	1	4.096
0	1	0	6.144
0	1	1	8.192
1	0	0	12.288
1	0	1	24.576
1	1	0	33.8688
1	1	1	73.728

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X2	Output	Crystal connection. Connect to a 27 MHz fundamental mode pullable crystal.
2	X1	Input	Crystal connection. Connect to a 27 MHz fundamental mode pullable crystal.
3	VDD	Power	Connect to +3.3 V.
4	VDD	Power	Connect to +3.3 V.
5	VIN	Input	Voltage input to VCXO. Changing the voltage between 0 to 3.3 V controls the VCXO frequency.
6	GND	Power	Connect to ground.
7	GND	Power	Connect to ground.
8	$\overline{\text{PDTS}}$	Power	Power Down Tri-state. This pin powers down entire chip and tri-states the outputs when low. Internal pull-up resistor.
9	S2	Input	Select input S2. Selects ACLK per table above. Internal pull-up resistor.
10	ACLK	Output	Audio clock output per table above.
11	GND	Power	Connect to ground.
12	27M	Output	27 MHz reference clock output.
13	S0	Input	Select input S0. Selects ACLK per table above. Internal pull-up resistor.
14	VDD	Power	Connect to +3.3 V.
15	NC	--	No connect. Do not connect anything to this pin.
16	S1	Input	Select input S1. Selects ACLK per table above. Internal pull-up resistor.

External Component Selection

The MK3724 requires a minimum number of external components for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 μF should be connected between VDD and GND on pins 3 and 4, pins 6 and 7, and pins 11 and 14 as close to the MK3724 as possible. For optimum device performance, the decoupling capacitors should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB traces between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50 Ω trace (a commonly used trace impedance), place a 33 Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 Ω

Quartz Crystal

The MK3724 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device meeting IDT' recommended parameters must be used, and the layout guidelines discussed in the following section must be followed.

See Application Note MAN05 for a full list of crystal parameters.

The frequency of oscillation of a quartz crystal is determined by its "cut" and by the load capacitors connected to it. The MK3724 incorporates on-chip variable load capacitors that "pull" (change) the frequency of the crystal. The crystal specified for use with the MK3724 is designed to have zero frequency error when the total of on-chip + stray capacitance is 14 pF.

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the MK3724. There should be no via's between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal.

Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. Stuffing of these capacitors on the PCB is optional. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

To determine the need for and value of the crystal adjustment capacitors, you will need a PC board of your final layout, a frequency counter capable of about 1 ppm resolution and accuracy, two power supplies, and samples of the crystals which you plan to use in production. You will also need measured initial accuracy for each crystal at the specified crystal load capacitance (C_L).

To determine the value of the crystal capacitors:

1. Connect VDD to 3.3 V. Connect pin 5 to the second power supply. Adjust the voltage on pin 5 to 0V. Measure and record the frequency of the CLK output.

2. Adjust the voltage on pin 5 to 3.3 V. Measure and record the frequency of the same output.

To calculate the centering error:

$$Error = 10^6 x\left[\frac{(f_{3.3(3.0)V} - f_{target}) + (f_{0V} - f_{target})}{f_{target}}\right] - error_{xtal}$$

Where:

f_{target} = nominal crystal frequency

$error_{xtal}$ =actual initial accuracy (in ppm) of the crystal being measured

If the centering error is less than ±25 ppm, no adjustment is needed. If the centering error is more than 25 ppm negative, the PC board has excessive stray capacitance and a new PCB layout should be considered to reduce stray capacitance. (Alternately, the crystal may be re-specified to a higher load capacitance. Contact IDT for details.) If the centering error is more than 25 ppm positive, add identical fixed centering capacitors from each crystal pin to ground. The value for each of these caps (in pF) is given by:

External Capacitor =

2 x (centering error)/(trim sensitivity)

Trim sensitivity is a parameter which can be supplied by your crystal vendor. If you do not know the value, assume it is 30 ppm/pF. After any changes, repeat the measurement to verify that the remaining error is acceptably low (typically less than ±25 ppm).

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK3724. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature, Commercial	0 to +70° C
Ambient Operating Temperature, Industrial	-40 to +85° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature, Commercial	0		+70	° C
Ambient Operating Temperature, Industrial	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.135		+3.465	V
Reference crystal parameters	Refer to page 3			

DC Electrical Characteristics

VDD=3.3 V ±5% , Ambient temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output Low Voltage (CMOS Level)	V_{OL}	I_{OH} = +4 mA			0.375	V
Input High Voltage (S1:S0)	V_{IH}		2.0			V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage (S2)	V_{IH}		2.5			V
Input Low Voltage (S1:S0)	V_{IL}				0.8	V
Input Low Voltage (S2)	V_{IL}				0.5	V
Input High Current	I_{IH}	at 3.3V, Sx, $\overline{PDTS}$		0.1		µA
Input Low Current	I_{IL}	at 0V, Sx, $\overline{PDTS}$		-8.5		µA
Operating Supply Current	IDD	No load		11		mA
Short Circuit Current	I_{OS}			±50		mA
VIN, VCXO Control Voltage	V_{IA}		0		3.3	V
On Chip Pull-up Resistor, inputs	R_{PU}	Input selects		360		kΩ
Input Capacitance	C_{IN}	Input selects		5		pF
Nominal Output Impedance	Z_{OUT}			20		Ω

AC Electrical Characteristics

VDD = 3.3 V ±5%, Ambient Temperature -40 to +85° C, unless stated otherwise

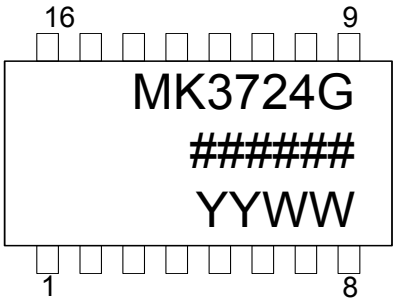
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Crystal Pullability	f_P	0V≤ VIN ≤ 3.3 V, Note 1	± 100	± 150		ppm
VCXO Gain		VIN = VDD/2 ± 1 V, Note 1		150		ppm/V
Output Rise Time	t_{OR}	20% to 80%, C_L=15 pF		1.2	2.0	ns
Output Fall Time	t_{OF}	80% to 20%, C_L=15 pF		1.2	2.0	ns
Output Clock Duty Cycle	t_D	Measured at 1.65 V, C_L=15 pF	40	50	60	%
Maximum Output Jitter, short term	t_J	C_L=15 pF		±150		ps
Changing Frequency Setting Time					1	ms
Power-up time		PLL lock time from power-up up to ±1% of final frequency			10	ms
		$\overline{PDTS}$ goes high until stable CLK output up to 1% of final frequency			2	ms

Note 1: External crystal device must conform with Pullable Crystal Specifications listed on page 3.

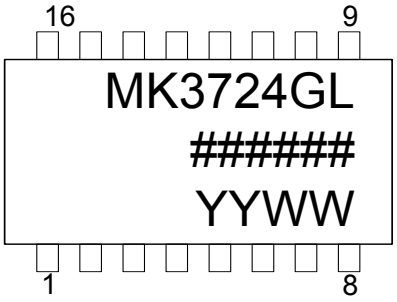
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

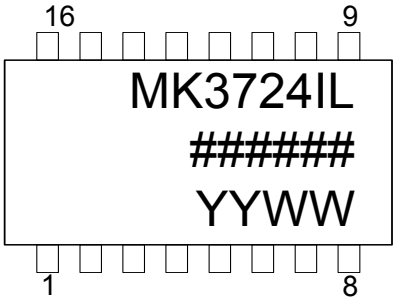
Marking Diagram



Non Lead-Free



Lead-Free



Industrial Temp., Lead-Free

Notes:

1. ###### is the lot code.

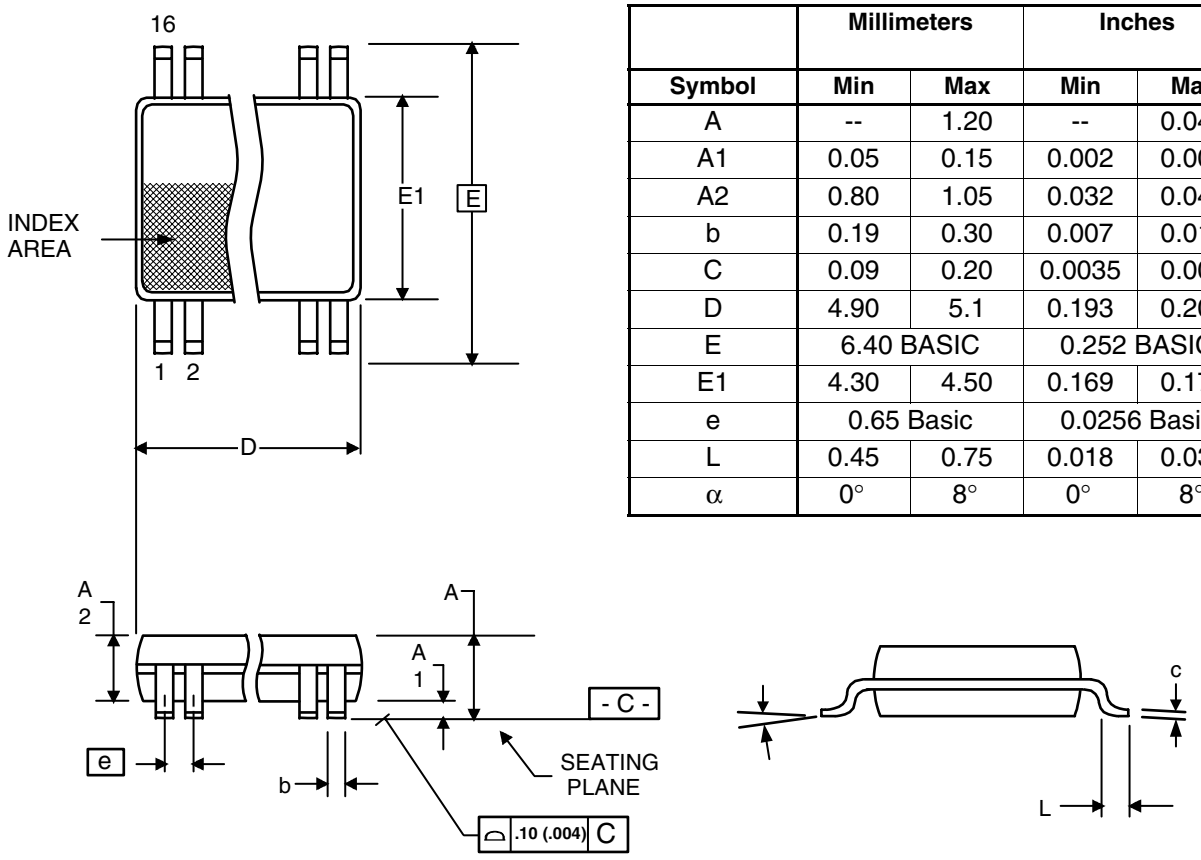
2. YYWW is the last two digits of the year, and the week number that the part was assembled.

3. “L” designates Pb (lead) free.

4. Bottom mark denotes country of origin if not USA.

Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95Ordering Information



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK3724G*	MK3724G	Tubes	16-pin TSSOP	0 to +70° C
MK3724GTR*	MK3724G	Tape and Reel	16-pin TSSOP	0 to +70° C
MK3724GLF	MK3724GL	Tubes	16-pin TSSOP	0 to +70° C
MK3724GLFTR	MK3724GL	Tape and Reel	16-pin TSSOP	0 to +70° C
MK3724GILF	MK3724IL	Tubes	16-pin TSSOP	-40 to +85° C
MK3724GILFTR	MK3724IL	Tape and Reel	16-pin TSSOP	-40 to +85° C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-0**

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