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VERSACLOCK® LOW POWER CLOCK GENERATOR IDT5P49EE605

Description

The IDT5P49EE605 is a programmable clock generator intended for low power, battery operated consumer applications. There are four internal PLLs, each individually programmable, allowing for four unique non-integer-related frequencies. The frequencies are generated from a single reference clock. The reference clock can come from either a TCXO or input clock. An additional 32.768kHz crystal oscillator is available to provide a real time clock or non-critical performance MHz processor clock.

Two buffered reference Sine wave output clocks are supported with amplitude of 750 mV to 1V, peak to peak.

The IDT5P49EE605 can be programmed through the use of the I^2C interfaces. The programming interface enables the device to be programmed when it is in normal operation or what is commonly known as in system programmable. An internal EEPROM allows the user to save and restore the configuration of the device without having to reprogram it on power-up.

Each of the four PLLs has an 8-bit reference divider and a 11-bit feedback divider. This allows the user to generate four unique non-integer-related frequencies. The PLL loop bandwidth is programmable to allow the user to tailor the PLL response to the application. For instance, the user can tune the PLL parameters to minimize jitter generation or to maximize jitter attenuation.

Spread spectrum generation is supported on one of the PLLs. The device is specifically designed to work with display applications to ensure that the spread profile remains consistent for each HSYNC in order to reduce ROW noise.

There are total six 8-bit output dividers. The outputs are connected to the PLLs via the switch matrix. The switch matrix allows the user to route the PLL outputs to any output bank. This feature can be used to simplify and optimize the board layout. In addition, each output's slew rate and enable/disable function can be programmed.

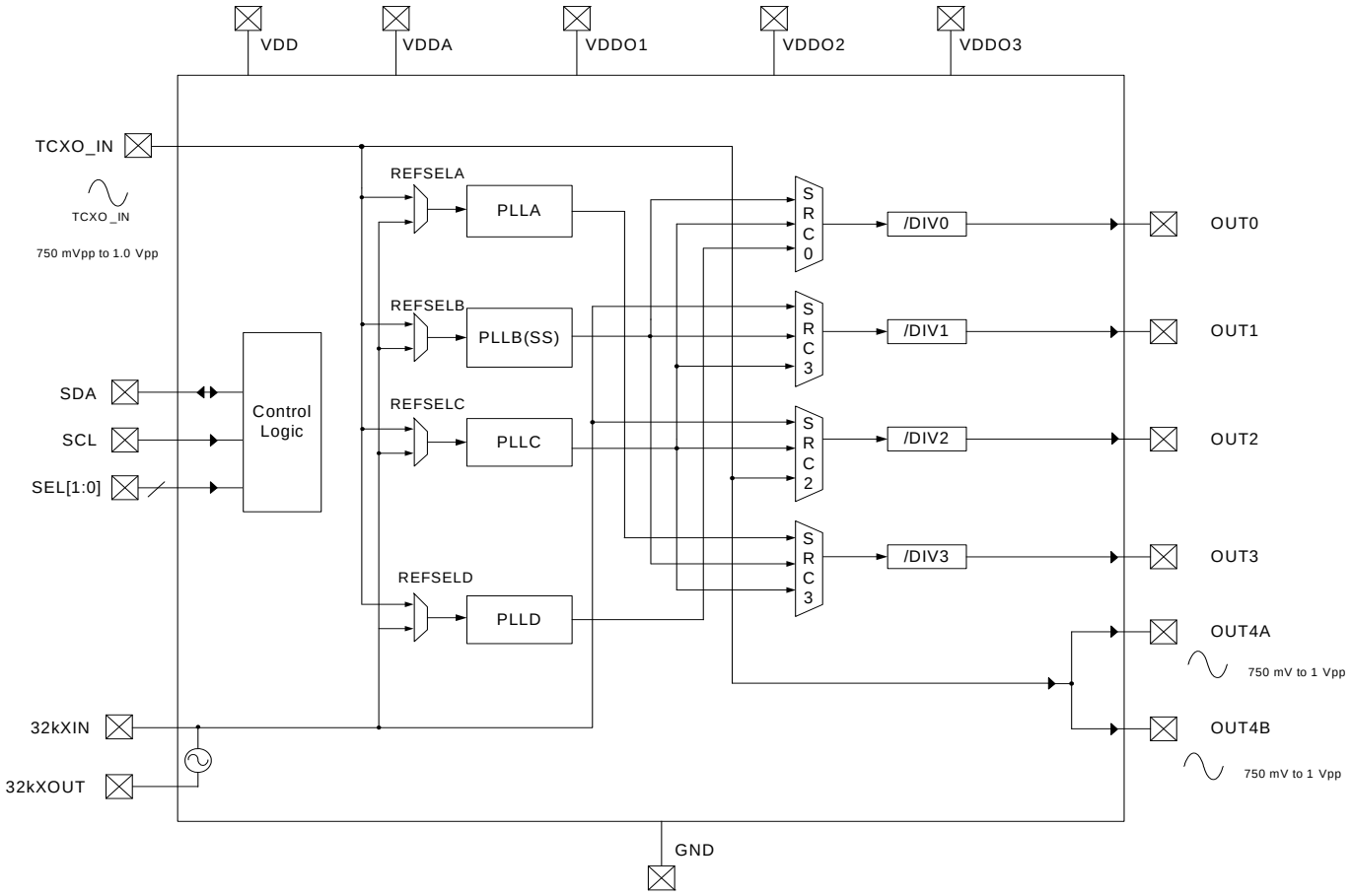
Target Applications

- Smart Mobile Handset
- Personal Navigation Device (PND)
- Camcorder
- DSC
- Portable Game Console
- Personal Media Player

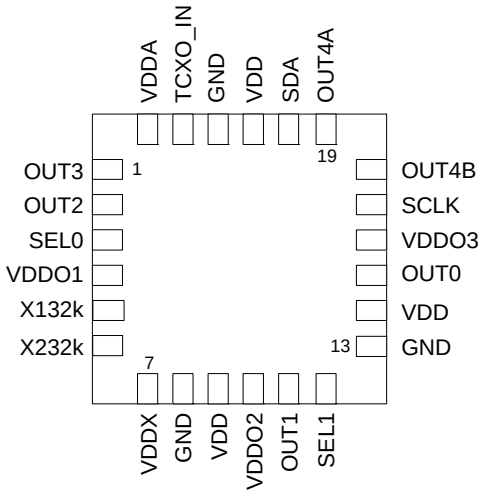
Features

- Four internal PLLs
- Internal non-volatile EEPROM
  - Internal I^2C EEPROM master interface
- FAST (400kHz) mode I^2C serial interfaces
- Input Frequencies
  - TCXO: 10 MHz to 40 MHz
  - RTC Crystal: 32.768 kHz
- Two buffered Sine wave outputs at 750 mV to 1Vpp
- Output Frequency Ranges: kHz to 120 MHz
- Each PLL has an 8-bit reference divider and a 11-bit feedback-divider
- 8-bit output-divider blocks
- One of the PLLs support Spread Spectrum generation capable of configuration to pixel rate, with adjustable modulation rate and amplitude to support video clock with no visible artifacts
- I/O Standards:
  - Outputs - 1.8V/2.5V/3.3 V LVTTL/ LVCMOS
- 3 independent adjustable VDDO groups.
- Programmable Slew Rate Control
- Programmable Loop Bandwidth Settings
- Programmable output inversion to reduce bimodal jitter
- Individual output enable/disable
- Power-down/Sleep mode
  - 10µA max in power down mode
  - 32kHz clock output active sleep mode
  - 100µA max in sleep mode
- 1.8V VDD Core Voltage
- Available in 24pin 4x4mm QFN packages
- -40 to +85 C Industrial Temp operation

Functional Block Diagram



Pin Assignment



24- pin QFN

Pin Descriptions

Pin Name	Pin #	I/O	Pin Type	Pin Description
OUT3	1	O	Adjustable	Configurable clock output 3. Single-ended output voltage levels are register controlled by either VDDO1, VDDO2 or VDDO3.
OUT2	2	O	Adjustable	Configurable clock output 2. Single-ended output voltage levels are register controlled by either VDDO1, VDDO2 or VDDO3.
SEL0*	3	I	LVTTL	Configuration select pin. Weak internal pull down resistor.
VDDO1	4		Power	Device power supply. Connect to 1.8 to 3.3V. Using register settings, select output voltage levels for OUT0-OUT3. VDDO1 must be greater than or equal to both VDDO2 and VDDO3.
X132k	5	I	LVTTL	32kHz CRYSTAL_IN -- Reference crystal input
X232k	6	O	LVTTL	32kHz CRYSTAL_OUT -- Reference crystal feedback.
VDDx	7		Power	Crystal oscillator power supply. Connect to 1.8V. Use filtered analog power supply if available.
GND	8		Power	Connect to Ground.
VDD	9		Power	Device power supply. Connect to 1.8V.
VDDO2	10		Power	Device power supply. Connect to 1.8 to 3.3V. Using register settings, select output voltage levels for OUT0-OUT3. VDDO2 must be equal or less than VDDO1.
OUT1	11	O	Adjustable	Configurable clock output 1. Single-ended output voltage levels are register controlled by either VDDO1, VDDO2 or VDDO3.
SEL1*	12	I	LVTTL	Configuration select pin. Weak internal pull down resistor.

GND	13		Power	Connect to Ground.
VDD	14		Power	Device power supply. Connect to 1.8V.
OUT0	15	O	Adjustable	Configurable clock output 0. Single-ended output voltage levels are register controlled by either VDDO1, VDDO2 or VDDO3.
VDDO3	16		Power	Device power supply. Connect to 1.8 to 3.3V. Using register settings, select output voltage levels for OUT0-OUT3. VDDO3 must be equal or less than VDDO1.
SCLK	17	I	LVTTL	I^2C clock. Logic levels set by VDDO1. 5V tolerant.
OUT4B	18	O	Output	Buffered reference Sine wave clock output. Single-ended output voltage levels are controlled by VDDA. Output high-Z when disabled. AC couple wiht 0.1µF capacitor.
OUT4A	19	O	Output	Buffered reference Sine wave clock output. Single-ended output voltage levels are controlled by VDDA. Output high-Z when disabled. AC couple wiht 0.1µF capacitor.
SDA	20	I/O	Open Drain	Bidirectional I^2C data. Logic levels set by VDDO1. 5V tolerant.
VDD	21		Power	Device power supply. Connect to 1.8V.
GND	22		Power	Connect to Ground.
TCXO_IN	23	I	Input	TCXO input or external reference clock input.
VDDA	24	--	Power	Filtered analog power supply. Connect to 1.8V.

Note *: SEL pins should be controlled by 1.8V LVTTL logic; 3.3V tolerant.

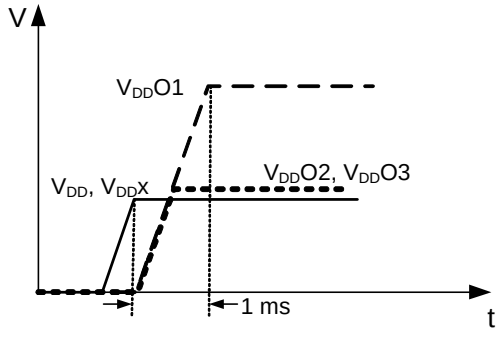
Note 1: Outputs are user programmable to drive single-ended 1.8V/2.5V/3.3V LVTTL as indicated above.

Note 2: Default configuration CLK3=Buffered Reference output. All other outputs are off.

Note 3: Do not power up with SEL[1:0] = 00 (in Power down/Sleep mode).

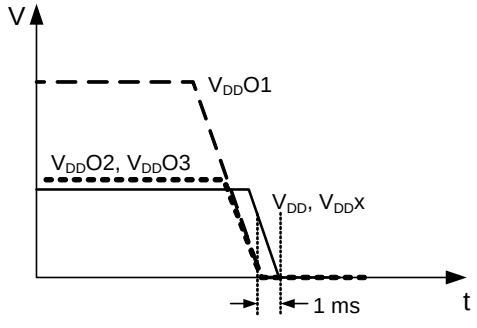
Ideal Power Up Sequence

1) V_{DD} and $V_{DD}x$ must come up first, followed by $V_{DD}O$
2) $V_{DD}O1$ must come up within 1ms after VDD and VDDX come up
3) $V_{DD}O2/3$ must be equal to, or lower than, $V_{DD}O1$
4) V_{DD} and $V_{DD}x$ have approx. the same ramp rate
5) $V_{DD}O1$ and $V_{DD}O2/3$ have approx. same ramp rate

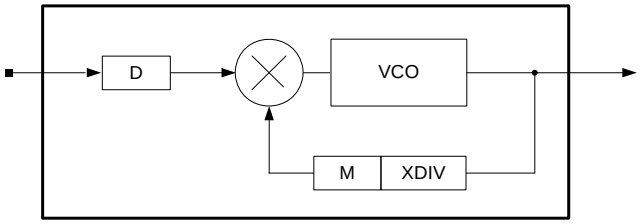


Ideal Power Down Sequence

1) $V_{DD}O$ must drop first, followed by V_{DD} and $V_{DD}x$
2) V_{DD} and $V_{DD}x$ must come down within 1ms after $V_{DD}O1$ comes down
3) $V_{DD}O2/3$ must be equal to, or lower than, $V_{DD}O1$
4) V_{DD} and $V_{DD}x$ have approx. the same ramp rate
5) $V_{DD}O1$ and $V_{DD}O2/3$ have approx. same ramp rate



PLL Features and Descriptions



PLL Block Diagram

	Ref-Divider (D) Values	Feedback Pre-Divider (XDIV) Values	Feedback (M) Values	Programmable Loop Bandwidth	Spread Spectrum Generation Capability
PLLA	1 - 255	1 or 4	6 - 2047	Yes	No
PLLB	1 - 255	4	6 - 2047	Yes	Yes
PLLC	1 - 255	1 or 8 bit divide	6 - 2047	Yes	No
PLLD	1 - 255	1 or 4	6 - 2047	Yes	No

Crystal Input (XIN/REF)

The crystal oscillators should be fundamental mode quartz crystals; overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 50Ω maximum equivalent series resonance. 0

ONXTALB=0 bit needs to be set for XIN/REF.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The crystal cpacitors are internal to the device and have an effective value of 4pF.

Reference Pre-Divider, Reference Divider, Feedback-Divider and Post-Divider

Each PLL incorporates an 8-bit reference-scaler and a 11-bit feedback divider which allows the user to generate four unique non-integer-related frequencies. PLLA and PLLD each have a feedback pre-divider that provides additional multiplication for kHz reference clock applications. Each output divider supports 8-bit post-divider. The following equation governs how the output frequency is calculated.

$$F_{OUT} = \frac{F_{IN} * \left(\frac{XDIV*M}{D}\right)}{ODIV} \quad \text{(Eq. 2)}$$

Where F_{IN} is the reference frequency, XDIV is the feedback pre-divider value, M is the feedback-divider value, D is the reference divider value, ODIV is the total post-divider value, and F_{OUT} is the resulting output frequency. Programming any of the dividers may cause glitches on the outputs.

SPREAD SPECTRUM GENERATION (PLLB)

PLLB has spread spectrum generation capability, which users have the option of turning on and off. Spread spectrum profile, frequency, and spread are fully programmable (within limits). The programmable spread spectrum generation parameters are NC[10:0], MOD[12:0], and NSS[10:0] bits. To enable spread spectrum, set SSENB_B=0.

The spread spectrum circuitry was specifically developed to accommodate video display applications. The spread modulation frequency can be defined to exactly equal the horizontal line frequency (HSYNC)

NC[10:0]

These bits are used to determine the number of pulses per spread spectrum cycle. For video applications, NC is the number of pixels on the horizontal display row (or integer multiple of displayed pixels in a row). By matching the spread period to the screen, no tearing or “shimmer” will be apparent.

NC must be an even number to insure that the upward spread transition has the same number of steps as the downward spread transition.

For non-video applications, this can also be seen as the number of clock cycles for a complete spread spectrum period.

MOD[12:0]

These bits relate the reference frequency to the target average spread output frequency (F_{MID}). F_{MID} is the midpoint between F_{MAX} (maximum frequency) and F_{MIN} (minimum frequency).

$F_{MID} = (F_{MAX} + F_{MIN}) / 2$

$MOD = (F_{REF} * NC) / (2 * F_{MID})$

NSS[10:0]

These bits control the amplitude of the spread modulation.

$NSS = (NC / 2) + (NC / 8) * (F_{MAX} - F_{MIN}) / F_{MID}$

Modulation frequency:

$F_{MOD} = F_{MID} / NC$ (Eq. 11)

Video Example

F_{REF} = 25MHz, F_{OUT} = 27 MHz, 640 pixels per line, center spread of ±1%. Find the necessary spread spectrum register settings.

$F_{MID} = F_{OUT}$

NC = 640 or 320 or 160 (integer number of spread periods/screen)

MOD = (25MHz * 640)/(2 * 27MHz) = 296

NSS = (640/2)+(640/8)*(27.27MHz-26.73MHz)/27MHz = 322.

F_{MOD} = 27MHz/640 = 42.2kHz.

Non-Video Example

F_{REF} = 25MHz, F_{OUT} = 27 MHz, 32kHz modulation rate, center spread of ±1%. Find the necessary spread spectrum register settings.

$F_{MID} = F_{OUT}$

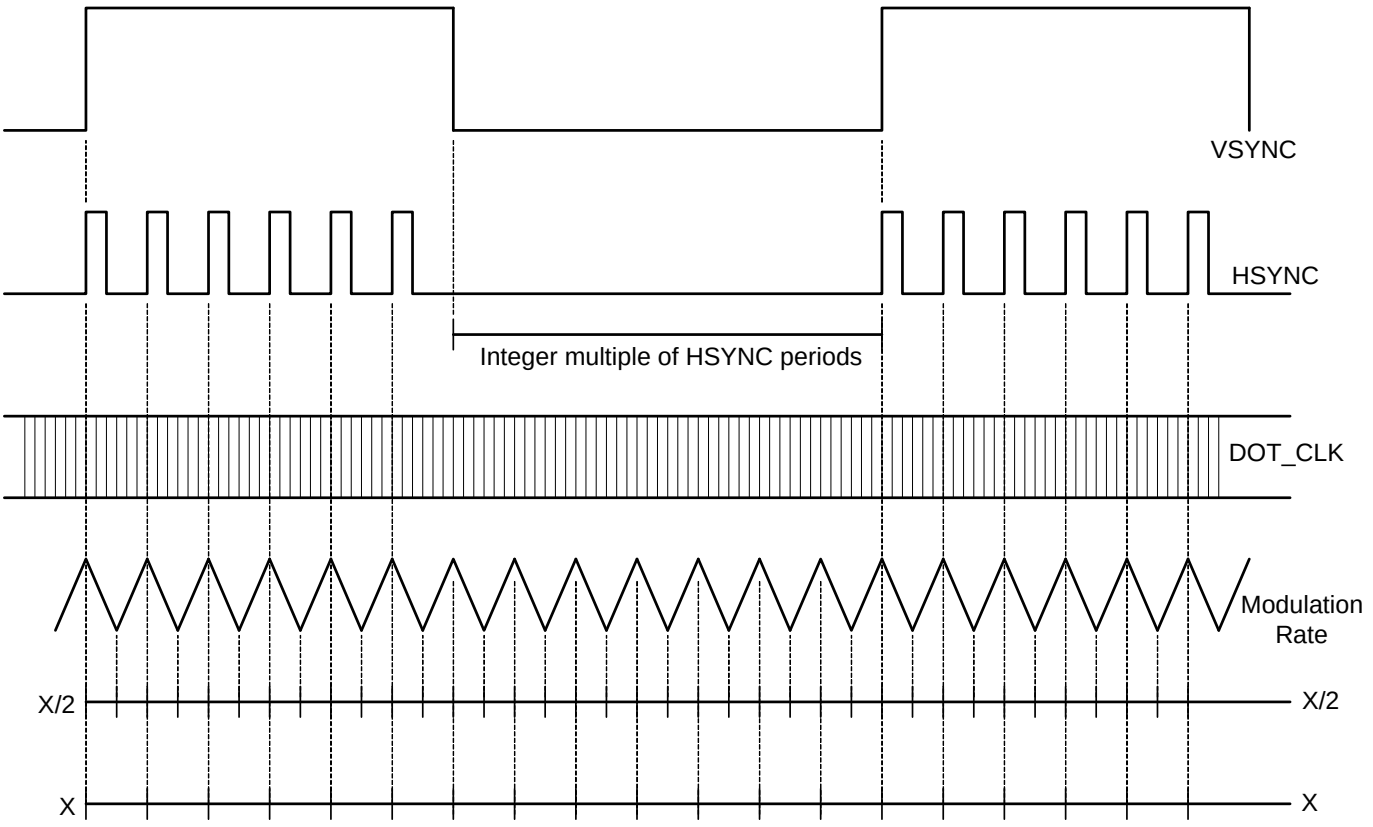
F_{MOD} = 32kHz = 27MHz/NC.

NC = 844

MOD = (25MHz * 844)/(2 * 27MHz) = 391

NSS = (844/2)+(844/8)*(27.27MHz-26.73MHz)/27MHz = 424.

VSYNC, HSYNC, DOT_CLK – Modulation Rate Relationship



X = Number of cycles of DOT_CLK per HSYNC period.

X/2 = Number of cycles of DOT_CLK that the modulation edge rises/falls.

LOOP FILTER

The loop filter for each PLL can be programmed to optimize the jitter performance. The low-pass frequency response of the PLL is the mechanism that dictates the jitter transfer characteristics. The loop bandwidth can be extracted from the jitter transfer. A narrow loop bandwidth is good for jitter attenuation while a wide loop bandwidth is best for low jitter generation. The specific loop filter components that can be programmed are the resistor via the RZ[4:0] bits, zero capacitor via the CZ[2:0] bits, pole capacitor via the CP[1:0] bits, and the charge pump current via the IP#[2:0] bits.

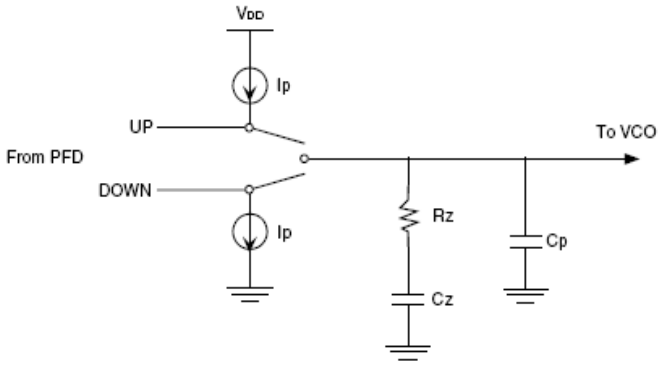
The following equations govern how the loop filter is set:

Zero capacitor (Cz) = 280pF

Pole capacitor (Cp) = 30pF

Charge pump (Ip) = IP#[2:0] uA

VCO gain (K_{VCO}) = 300MHz/V * 2π



PLL Loop Bandwidth:

Charge pump gain ($K\phi$) = Ip / 2π

VCO gain (K_{VCO}) = 350MHz/V * 2π

M = Total multiplier value (See the PRE-SCALERS, FEEDBACK-DIVIDERS, POST-DIVIDERS section for more detail)

$\omega c = (Rz * K\phi * K_{VCO} * Cz)/(M * (Cz + Cp))$

$Fc = \omega c / 2\pi$

Note, the phase/frequency detector frequency (F_{PFD}) is typically seven times the PLL closed-loop bandwidth (Fc) but too high of a ratio will reduce your phase margin thus compromising loop stability.

To determine if the loop is stable, the phase margin (ϕm) would need to be calculated as follows.

Phase Margin:

$\omega z = 1 / (Rz * Cz)$

$\omega p = (Cz + Cp)/(Rz * Cz * Cp)$

$\phi m = (360 / 2\pi) * [\tan^{-1}(\omega c/ \omega z) - \tan^{-1}(\omega c/ \omega p)]$

To ensure stability in the loop, the phase margin is recommended to be > 60° but too high will result in the lock time being excessively long. Certain loop filter parameters would need to be compromised to not only meet a required loop bandwidth but to also maintain loop stability.

Damping Factor:

$\zeta = Rz/2 * (K_{VCO} * Ip * Cz)^{1/2}/M$

Example

Fc = 150KHz is the desired loop bandwidth. The total A*M value is 160. The ζ(damping factor) target should be 0.7, meaning the loop is critically damped. Given Fc and A*M, an optimal loop filter setting needs to be solved for that will meet both the PLL loop bandwidth and maintain loop stability.

Choose a mid-range charge pump from register table

Icp= 11.9uA.

$K\phi * K_{VCO}$ = 350MHz/V * 40uA = 12000A/Vs

$\omega c = 2\pi * Fc = 9.42x10^5\ s^{-1}$

$\omega p = (Cz + Cp)/(Rz * Cz * Cp) = \omega z\ (1 + Cz / Cp)$

Solving for Rz, the best possible value Rz=30kOhms (RZ[1:0]=10) gives

ζ= 1.4 (Ideal range for ζ is 0.7 to 1.4)

Solving back for the PLL loop bandwidth, Fc=149kHz.

The phase margin must be checked for loop stability.

$\phi m = (360 / 2\pi) * [\tan^{-1}(9.42x10^5\ s^{-1} / 1.19x10^5 s^{-1})$
$- \tan^{-1}(9.42x10^5\ s^{-1} / 1.23x10^6\ s^{-1})] = 45°$

The phase margin would be acceptable with a fairly stable loop.

SEL[1:0] Function

The IDT5P49EE605 can support up to three unique configurations. Users may pre-program all configurations, selected using SEL[1:0] pins. Alternatively, users may use I2C interface to configure these registers on- the-fly.

Power Down/Sleep Mode is selected by the No_PD bit. No_PD=0 enables Power Down mode with no outputs. No_PD=1 enables sleep mode with 32kHz output on OUT2.
.

Always power with SEL1=1 and/or SEL0=1.

SEL1	SEL0	Configuration Selections
0	0	Power Down/Sleep Mode
0	1	Select CONFIG0
1	0	Select CONFIG1
1	1	Select CONFIG2

Configuration OUTx IO Standard

Users can configure the individual output IO standard from a single 3.3V power supply. Each output can support 1.8V/ 2.5V or 3.3V LVCMOS. VDDO1 must have the highest voltage of any pin on the device. VDDO2 and VDDO3 may have any value between 1.8V and VDDO1.

Programming the Device

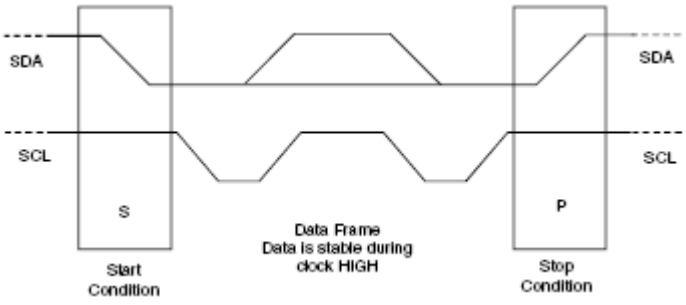
I^2C may be used to program the IDT5P49EE605.

– Device (slave) address = 7'b1101010

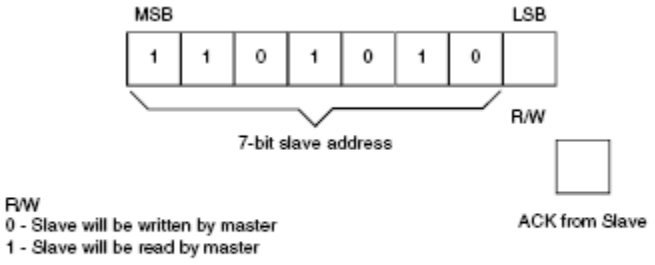
I^2C Programming

The IDT5P49EE605 is programmed through an I^2C-Bus serial interface, and is an I^2C slave device. The read and write transfer formats are supported. The first byte of data after a write frame to the correct slave address is interpreted as the register address; this address auto-increments after each byte written or read.

The frame formats are shown in the following illustration.



Framing



The first byte transmitted by the Master is the Slave Address followed by the R/W bit.
The Slave acknowledges by sending a "1" bit.

First Byte Transmitted on I^2C Bus

External I²C Interface Condition

KEY:

From Master to Slave

From Master to Slave, but can be omitted if followed by the correct sequence
Normally data transfer is terminated by a STOP condition generated by the Master. However, if the Master still wishes to communicate on the bus, it can generate a repeated START condition, and address another Slave address without first generating a STOP condition.

From Slave to Master

SYMBOLS:

ACK - Acknowledge (SDA LOW)
NACK - Not Acknowledge (SDA HIGH)
Sr - Repeated Start Condition
S - START Condition
P - STOP Condition

EEPROM Interface

The IDT5P49EE605 can store its configuration in an internal EEPROM. The contents of the device's internal programming registers can be saved to the EEPROM by issuing a save instruction (ProgSave) and can be loaded back to the internal programming registers by issuing a restore instruction (ProgRestore).

To initiate a save or restore using I²C, only two bytes are transferred. The Device Address is issued with the read/write bit set to “0”, followed by the appropriate command code. The save or restore instruction executes after the STOP condition is issued by the Master, during which time the IDT5P49EE605 will not generate Acknowledge bits. The IDT5P49EE605 will acknowledge the instructions after it has completed execution of them. During that time, the I²C bus should be interpreted as busy by all other users of the bus.

On power-up of the IDT5P49EE605, an automatic restore is performed to load the EEPROM contents into the internal programming registers. The IDT5P49EE605 will be ready to accept a programming instruction once it acknowledges its 7-bit I²C address.

Progwrite

S	Address	R/W	ACK	Command Code	ACK	Register	ACK	Data	ACK	P
	7-bits	0	1-bit	8-bits: xxxxxx00	1-bit	8-bits	1-bit	8-bits	1-bit	

Progwrite Command Frame

Writes can continue as long as a Stop condition is not sent and each byte will increment the register address.

Progread

Note: If the expected read command is not from the next higher register to the previous read or write command, then set a known “read” register address prior to a read operation by issuing the following command:

S	Address	R/W	ACK	Command Code	ACK	Register	ACK	P
	7-bits	0	1-bit	8-bits: xxxxxx00	1-bit	8-bits	1-bit	

Prior to Progread Command Set Register Address

The user can ignore the STOP condition above and use a repeated START condition instead, straight after the slave acknowledgement bit (i.e., followed by the Progread command):

S	Address	R/$\overline{W}$	ACK	ID Byte	ACK	Data_1	ACK	Data_2	ACK	Data_last	NACK	P
	7-bits	1	1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit	

Progread Command Frame

Progsave

S	Address	R/W	ACK	Command Code	ACK	P
	7-bits	0	1-bit	8-bits:xxxxxx01	1-bit	

Note:
PROGWRITE is for writing to the IDT5P49EE605 registers.
PROGREAD is for reading the IDT5P49EE605 registers.
PROGSAVE is for saving all the contents of the IDT5P49EE605 registers to the EEPROM.
PROGRESTORE is for loading the entire EEPROM contents to the IDT5P49EE605 registers.

Progrestore

S	Address	R/W	ACK	Command Code	ACK	P
	7-bits	0	1-bit	8-bits:xxxxxx10	1-bit	

I²C Bus DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Level		0.7xVDDO1		5.5	V
V_{IL}	Input LOW Level				0.3xVDDO1	V
V_{HYS}	Hysteresis of Inputs		0.05xVDDO1			V
I_{IN}	Input Leakage Current	V_{DD} = 0V			±1.0	µA
V_{OL}	Output LOW Voltage	I_{OL} = 3 mA			0.4	V

I²C Bus AC Characteristics for Standard Mode

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	Serial Clock Frequency (SCL)	0		100	kHz
t_{BUF}	Bus free time between STOP and START	4.7			µs
$t_{SU:START}$	Setup Time, START	4.7			µs
$t_{HD:START}$	Hold Time, START	4			µs
$t_{SU:DATA}$	Setup Time, data input (SDA)	250			ns
$t_{HD:DATA}$	Hold Time, data input (SDA) [1]	0			µs
t_{OVD}	Output data valid from clock			3.45	µs
C_B	Capacitive Load for Each Bus Line			400	pF
t_R	Rise Time, data and clock (SDA, SCLK)			1000	ns
t_F	Fall Time, data and clock (SDA, SCLK)			300	ns
t_{HIGH}	HIGH Time, clock (SCLK)	4			µs
t_{LOW}	LOW Time, clock (SCLK)	4.7			µs
$t_{SU:STOP}$	Setup Time, STOP	4			µs

Note 1: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}MIN of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.

I^2C Bus AC Characteristics for Fast Mode

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	Serial Clock Frequency (SCL)	0		400	kHz
t_{BUF}	Bus free time between STOP and START	1.3			µs
$t_{SU:START}$	Setup Time, START	0.6			µs
$t_{HD:START}$	Hold Time, START	0.6			µs
$t_{SU:DATA}$	Setup Time, data input (SDA)	100			ns
$t_{HD:DATA}$	Hold Time, data input (SDA) [1]	0			µs
t_{OVD}	Output data valid from clock			0.9	µs
C_B	Capacitive Load for Each Bus Line			400	pF
t_R	Rise Time, data and clock (SDA, SCL)	$20 + 0.1xC_B$		300	ns
t_F	Fall Time, data and clock (SDA, SCL)	$20 + 0.1xC_B$		300	ns
t_{HIGH}	HIGH Time, clock (SCL)	0.6			µs
t_{LOW}	LOW Time, clock (SCL)	1.3			µs
$t_{SU:STOP}$	Setup Time, STOP	0.6			µs

Note 1: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}MIN of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5P49EE605. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Symbol	Description	Max	Unit
V_{DD}	Internal Power Supply Voltage	-0.5 to +4.6	V
V_I	Input Voltage	-0.5 to +4.6	V
V_O	Output Voltage (not to exceed 4.6 V)	-0.5 to V_{DD}+0.5	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to +150	°C

Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}, V_{DD}x, V_{DD}A	Power supply voltage for core VDD	1.71	1.8	1.89	V
V_{DDOX}	Power supply voltage for outputs VDDO1/2/3	1.71	1.8	1.89	V
		2.375	2.5	2.625	V
		3.135	3.3	3.465	V
T_A	Operating temperature, ambient	-40		+85	°C
C_{LOAD_OUT}	Maximum load capacitance (3.3V LVTTL only)			15	pF
C_{LOAD_OUT}	Maximum load capacitance (1.8V or 2.5V LVTTL only)			8	pF
F_{IN}	External reference clock TCXO_IN	10		40	MHz
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05		5	ms
V_{IH}	Input HIGH Voltage	0.75*VDD		VDDO1	V
V_{IL}	Input LOW Voltage			0.3*VDD	V

Capacitance (T_A = +25 °C, f = 1 MHz, V_{IN} = 0V)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Input Capacitance		3		pF
TCXO Specifications					
TCXO_FREQ	TCXO frequency	10		40	MHz
TCXO_V_{PP}	Input voltage swing (peak-to-peak, nominal)	0.75		1.0	V

DC Electrical Characteristics for 3.3 Volt LVTTL [1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = 33mA	2.4		VDDO	V
V_{OL}	Output LOW Voltage	I_{OH} = 33mA			0.4	V
I_{OZDD}	Output Leakage Current	3-state outputs			5	µA

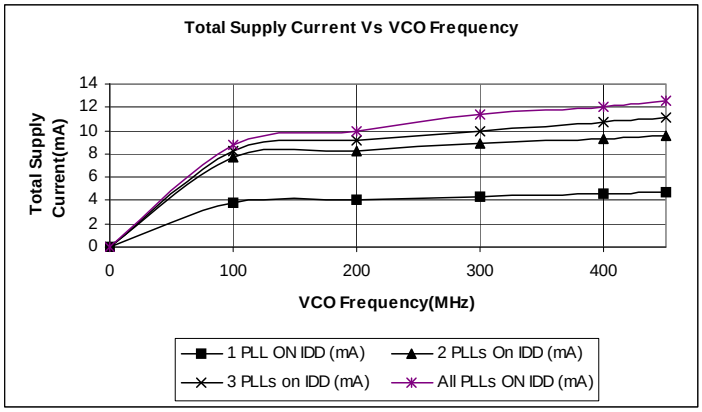
DC Electrical Characteristics for 2.5Volt LVTTL [1]

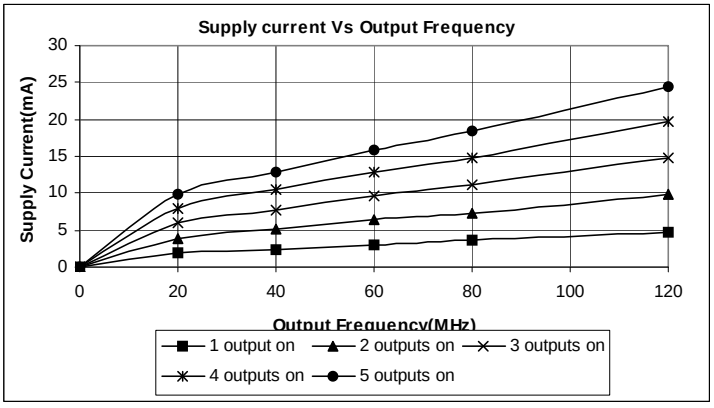
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = 25mA	2.1		VDDO	V
V_{OL}	Output LOW Voltage	I_{OH} = 25mA			0.4	V
I_{OZDD}	Output Leakage Current	3-state outputs			5	µA

DC Electrical Characteristics for 1.8Volt LVTTL [1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} =18mA	0.65*VDDO		VDDO	V
V_{OL}	Output LOW Voltage	I_{OH} = 18mA			0.35*VDDO	V
V_{IH}	Input HIGH Voltage	SEL[1:0], 3.3V tolerant	0.75VDD			V
V_{IL}	Input LOW Voltage	SEL[1:0], 3.3V tolerant			0.25VDD	V
I_{OZDD}	Output Leakage Current	3-state outputs			5	µA

Power Supply Characteristics for LVTTL Outputs





Note 1: See “Recommended Operating Conditions” table.

AC Timing Electrical Characteristics

(Spread Spectrum Generation = OFF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
1 / t1	Output Frequency	Single Ended Clock output limit (LVTTL) 3.3V	0.001		130	MHz
		Single Ended Clock output limit (LVTTL) 2.5V			120	MHz
		Single Ended Clock output limit (LVTTL) 1.8V			80	MHz
f_{VCO}	VCO Frequency	VCO operating Frequency Range	100		500	MHz
f_{PFD}	PFD Frequency	PFD operating Frequency Range	0.5 [1]		40	MHz
f_{BW}	Loop Bandwidth	Based on loop filter resistor and capacitor values	0.01		10	MHz
t2	Input Duty Cycle	Duty Cycle for Input	40		60	%
t3	Output Duty Cycle	Measured at VDD/2	45		55	%
t4	Slew Rate, SLEWx(bits) = 00	Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		5.1		V/ns
	Slew Rate, SLEWx(bits) = 01	Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		4.4		
	Slew Rate, SLEWx(bits) = 10	Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		2.8		
	Slew Rate, SLEWx(bits) = 11	Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		1.8		
t5	Clock Jitter	Peak-to-peak period jitter, CLK outputs measured at VDD/2; f_{PFD} >= 10 MHz Single output frequency only.			60	ps
		Peak-to-peak period jitter, CLK outputs measured at VDD/2; f_{PFD} >= 10 MHz Multiple output frequencies switching.			100	ps
t6	Output Skew	Skew between output to output on the same bank			75	ps
		Skew between any output (Same freq and IO type, FOUT >10MHz)			200	ps
t7	Lock Time	PLL Lock Time from Power-up (using MHz reference clock)[1]		5	20	ms
		PLL Lock Time from Power-up using 32.768kHz reference clock)		1	3	s
		PLL Lock time from shutdown mode		5	10	ms

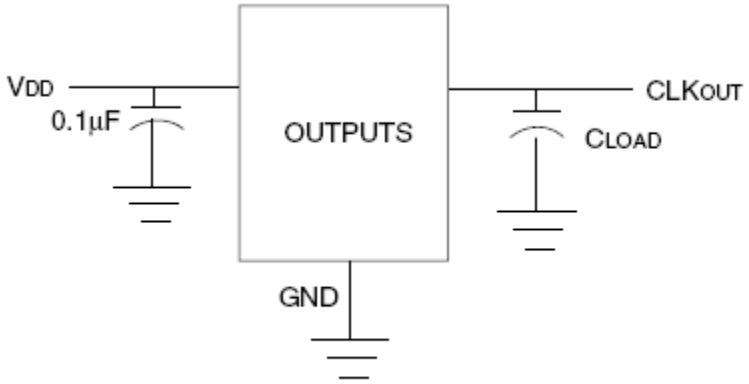
1.Time from supply voltage crosses VDD=1.62V to PLLs are locked.

Spread Spectrum Generation Specifications

Symbol	Parameter	Description	Min	Typ	Max	Unit
f_{IN}	Input Frequency	Input Frequency Limit	1 [1]		40	MHz
f_{MOD}	Mod Frequency	Modulation Frequency	32		120	kHz
f_{SPREAD}	Spread Value	Amount of Spread Value (programmable) - Down Spread	Programmable			$\%f_{OUT}$
		Amount of Spread Value (programmable) - Center Spread	Programmable			
		Total Spread Value	0.5		4.0	

Note 1: Practical lower frequency is determined by loop filter settings.

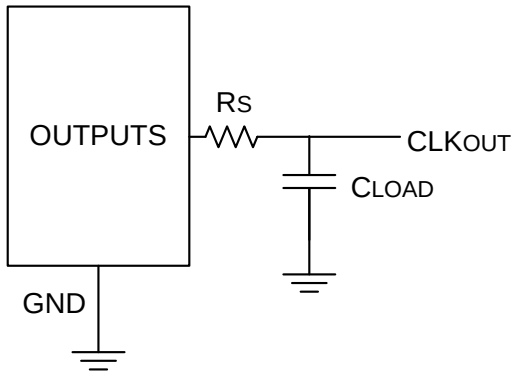
Test Circuits and Conditions [1]



NOTE:
1. All VDD pins must be tied together.

Test Circuits for DC Outputs

Other Termination Scheme (Block Diagram)



LVTTL: ~7pF for each output

Programming Registers Table

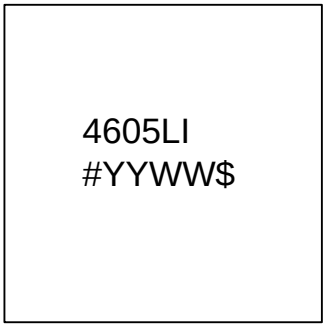
Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x00	00	Reserved	CSX2[1:0]		CSX1[1:0]		XTAL32ONB	Reserved		CSX2 [1:0]- internal 32kHz crystal cap2 00 - 18pF; 10 - 30pF 01 - 24pF; 11 - 36pF CSX1 [1:0] - Internal 32kHz crystal cap1 00 - 0pF; 10 - 6pF 01 - 3pF; 11 - 9pF XTAL32ONB - 32k crystal active low
0x01	00	INV[0]	SLEW0[0:1]		No_PD	PS0[2:1]		Reserved		No_PD - Enables/Disables 32kHz clock output on Config 00. No_PD=0 - 32kHz is off. No_PD=1 - 32kHz remains active. INV[#] - Invert output# SLEW#[0:1] - output# slew setting 0 0 - 5.1V/ns 0 1 - 4.4V/ns 1 0 - 2.8V/ns 1 1 - 1.8V/ns PS#[2:1] -Power Select 00 - Reserved 01 - CLK# connects to VDDO1 10 - CLK# connects to VDDO2 11 - CLK# connects to VDDO31
0x02	00	Reserved								
0x03	00	Reserved								
0x04	00	INV[1]	SLEW1[0:1]		Reserved	PS1[2:1]		Reserved		
0x05	00	Reserved								
0x06	00	Reserved								
0x07	00	INV[2]	SLEW2[0:1]		Reserved	PS22:1]		Reserved		
0x08	00	INV[3]	SLEW3[0:1]		Reserved	PS3[2:1]		Reserved		
0x09	00	Reserved								
0x0A	00	Reserved								
0x0B	00	Reserved								
0x0C	00	Reserved								
0x0D	00	Reserved								
0x0E	00	REFA[7:0]								**Configuration0** REFA[7:0] - Reference Divide PLLA
0x0F	00	FBA[10:3]								FBA[10:0] - Feedback Divide PLLA
0x10	00	Reserved					FBA[2:0]			
0x11	00	Reserved	XDIVA	RZA[1:0]		IPA[2:0]			REFSELA	XDIVA - FB predivide PLLA; 0 - /1; 1 - /4 RZA[1:0] - Zero Resistor PLLA 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPA[2:0] - charge Pump Current PLLA 100 - 6.3uA 101 -11.9 uA 110 - 17.7 uA 111 - 22.7uA REFSELA - Clock input PLLA 0 - MHz input 1 - 32kHz input
0x12	00	REFB[7:0]								REFB[7:0] - Reference Divide PLLB
0x13	00	FBB[10:3]								FBB[10:0] - Feedback Divide PLLB
0x14	00	MOD[4:0]					FBB[2:0]			PLLB Spread Parameters MOD[12:0] NC[10:0] NSS[12:0]
0x15	00	MOD[12:5]								
0x16	00	NC[10:3]								
0x17	00	NSS[4:0]					NC[2:0]			
0x18	00	NSS[12:5]								

Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x19	40	Reserved			IPB[2:0]			RZB[1:0]		RZB[1:0] - Zero Resistor PLLB 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPB[2:0] - charge Pump Current PLLB 000 - 0.37nA, 100 - 6.3nA 001 - 1.1nA, 101 - 11.9nA 010 - 1.8 nA, 110 - 17.7nA 011 - 3.4nA, 111 - 22.7nA REFSELB - Clock input PLLB 0 - MHz input 1 - 32kHz input
0x1A	00	Reserved						REFSELB	SSENB_B	
0x1B	00	REFC[7:0]								REFC[7:0] - Reference Divide PLLC
0x1C	00	FBC[10:3]								FBC[10:0] - Feedback Divide PLLC
0x1D	00	Reserved					FBC[2:0]			
0x1E	00	FBC2[7:0]								FBC2 - Feedback Predivide PLLC Turn on using XDIVC=1
0x1F	00	IPC[2:0]			RZC[1:0]		Reserved	XDIVC	REFSELC	RZC[1:0] - Zero Resistor PLLC 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPC[2:0] - charge Pump Current PLLC 100 - 6.3uA 101 -11.9 uA 110 - 17.7 uA 111 - 22.7uA REFSELC 0 - MHz input 1 - 32kHz input
0x20	00	REFD[7:0]								REFD[7:0] - Reference Divide PLLD
0x21	00	FBD[10:3]								FBD[10:0] - Feedback Divide PLLD
0x22	00	Reserved					FBD[2:0]			
0x23	00	XDIVD	RZD[1:0]		IPD[2:0]			REFSELD[1:0]		XDIVD - FB predivide PLLD; 0 - /1; 1 - /4 RZD[1:0] - Zero Resistor PLLD 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPD[2:0] - charge Pump Current PLLD 100 - 6.3uA 101 -11.9 uA 110 - 17.7 uA 111 - 22.7uA REFSELD[1:0] 00 - MHz input 11 - 32kHz input Others - Reserved
0x24	00	OD0[7:0]								OD#[7:0] - Output Divide#
0x25	00									
0x26	00	Reserved								
0x27	00	OD1[7:0]								
0x28	00	Reserved								
0x29	00	Reserved								
0x2A	00	OD2[7:0]								
0x2B	00	OD3[7:0]								
0x2C	00	Reserved								
0x2D	00	Reserved			SCR3[1:0]		SCR2[1:0]		Reserved	SRC3[1:0] - OD3 source 00 - off; 10 - PLLA 01 - PLLC; 11 - PLLB SRC2[1:0] - OD2 source 00 - off; 10 - MHz Reference 01 - PLLC; 11 - 32kHz Reference

Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x2E	00	Reserved		SCR1[1:0]		Reserved		Reserved		SRC1[1:0] - OD1 source 00 - off; 10 - PLLB 01 - 32kHz Reference; 11 - PLLD
0x2F	01	SCR0[1:0]		Reserved						SRC0[1:0] - OD0 source 00 - off; 10 - PLLC 01 - PLLB; 11 - PLLD
0x30	FF	Reserved								
0x31	00	PDB[4]	Reserved	OE[4B]	OE[4A]	Reserved				PDB[#] - Powerdown OUT#. PDB#=0, OUT# driven low OE[#] - Output enable OUT#. OE#=0, OUT# tri-stated. If PDB#=OE#=0, OUT# driven low
0x32	00	OE[3]	OE[2]	Reserved		OE[1]	Reserved		OE[0]	
0x33	00	PDB[3]	PDB[2]	Reserved		PDB[1]	Reserved		PDB[0]	
0x34	00	REFA[7:0]								**Configuration1** (See definitions from Configuration0 above)
0x35	00	FBA[10:3]								
0x36	00	Reserved					FBA[2:0]			
0x37	00	Reserved		RZA[1:0]		IPA[2:0]			REFSELA	
0x38	00	REFB[7:0]								
0x39	00	FBB[10:3]								
0x3A	00	MOD[4:0]					FBB[2:0]			
0x3B	00	MOD[12:5]								
0x3C	00	NC[10:3]								
0x3D	00	NSS[4:0]					NC[2:0]			
0x3E	00	NSS[12:5]								
0x3F	40	Reserved			IPB[2:0]			RZB[1:0]		
0x40	00	Reserved						REFSELB	SSENB_B	
0x41	00	REFC[7:0]								
0x42	00	FBC[10:3]								
0x43	00	Reserved					FBC[2:0]			
0x44	00	FBC2[7:0]								
0x45	00	IPC[2:0]			RZC[1:0]		Reserved	XDIV	REFSELC	
0x46	00	REFD[7:0]								
0x47	00	FBD[10:3]								
0x48	00	Reserved					FBD[2:0]			
0x49	00	Reserved	RZD[1:0]		IPD[2:0]			REFSELD[1:0]		
0x4A	00	OD0[7:0]								
0x4B	00	Reserved								
0x4C	00	Reserved								
0x4D	00	OD1[7:0]								
0x4E	00	Reserved								
0x4F	00	Reserved								
0x50	00	OD2[7:0]								
0x51	00	OD3[7:0]								
0x52	00	Reserved								
0x53	00	Reserved		SCR3[1:0]		SCR21:0]		Reserved		
0x54	00	Reserved		SCR1[1:0]		Reserved				
0x55	01	SCR0[1:0]		Reserved						
0x56	FF	Reserved								
0x57	00	PDB[4]	Reserved	OE[4B]	OE[4A]	Reserved				
0x58	00	OE[3]	OE[2]	Reserved		OE[1]	Reserved		OE[0]	
0x59	00	PDB[3]	PDB[2]	Reserved		PDB[1]	Reserved		PDB[0]	

Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x5A	00	REFA[7:0]								**Configuration2** (See definitions from Configuration0 above)
0x5B	00	FBA[10:3]								
0x5C	00	Reserved					FBA[2:0]			
0x5D	00	Reserved		RZA[1:0]		IPA[2:0]			REFSELA	
0x5E	00	REFB[7:0]								
0x5F	00	FBB[10:3]								
0x60	00	MOD[4:0]					FBB[2:0]			
0x61	00	MOD[12:5]								
0x62	00	NC[10:3]								
0x63	00	NSS[4:0]					NC[2:0]			
0x64	00	NSS[12:5]								
0x65	40	Reserved			IPB[2:0]			RZB[1:0]		
0x66	00	Reserved						REFSELB	SSENB_B	
0x67	00	REFC[7:0]								
0x68	00	FBC[10:3]								
0x69	00	Reserved					FBC[2:0]			
0x6A	00	FBC2[7:0]								
0x6B	00	IPC[2:0]			RZC[1:0]		Reserved	XDIV	REFSELC	
0x6C	00	REFD[7:0]								
0x6D	00	FBD[10:3]								
0x6E	00	Reserved					FBD[2:0]			
0x6F	00	XDIVD	RZD[1:0]		IPD[2:0]			REFSELD[1:0]		
0x70	00	OD0[7:0]								
0x71	00	Reserved								
0x72	00	Reserved								
0x73	00	OD1[7:0]								
0x74	00	Reserved								
0x75	00	Reserved								
0x76	00	OD2[7:0]								
0x77	00	OD3[7:0]								
0x78	00	Reserved								
0x79	00	Reserved		SCR3[1:0]		SCR2[1:0]		Reserved		
0x7A	00	Reserved		SCR1[1:0]		Reserved				
0x7B	01	SCR0[1:0]		Reserved						
0x7C	FF	Reserved								
0x7D	00	PDB[4]	Reserved	OE[4B]	OE[4A]	Reserved				
0x7E	00	OE[3]	OE[2]	Reserved		OE[1]	Reserved		OE[0]	
0x7F	00	PDB[3]	PDB[2]	Reserved		PDB[1]	Reserved		PDB[0]	

Marking Diagram (NL24)



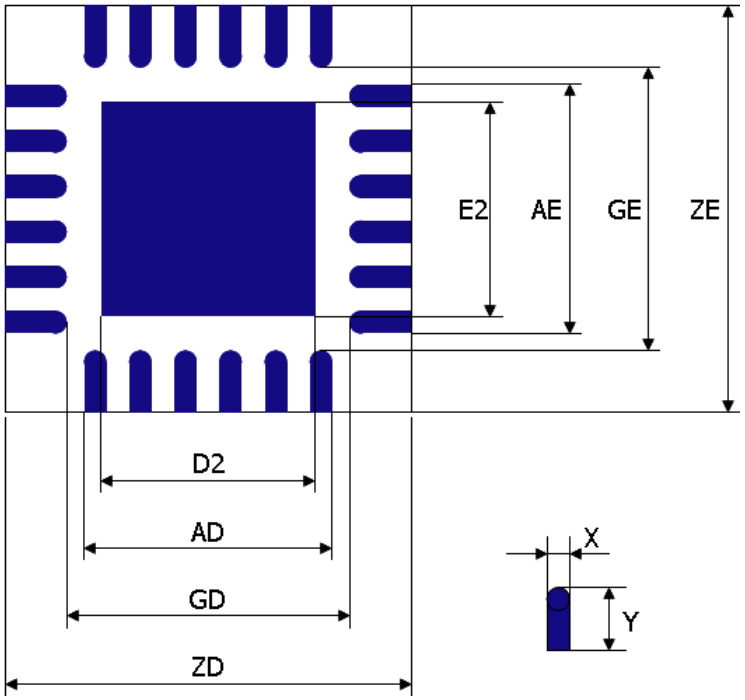
Notes:

1. "#" is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "$" is the assembly mark code.
4. "I" indicates industrial temperature range.
5. Bottom marking: country of origin if not USA.

Thermal Characteristics for 24QFN

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		50.1		°C/W
	θ_{JA}	1 m/s air flow		43.1		°C/W
	θ_{JA}	2.5 m/s air flow		39.4		°C/W
Thermal Resistance Junction to Case	θ_{JC}			61.7		°C/W

Landing Pattern

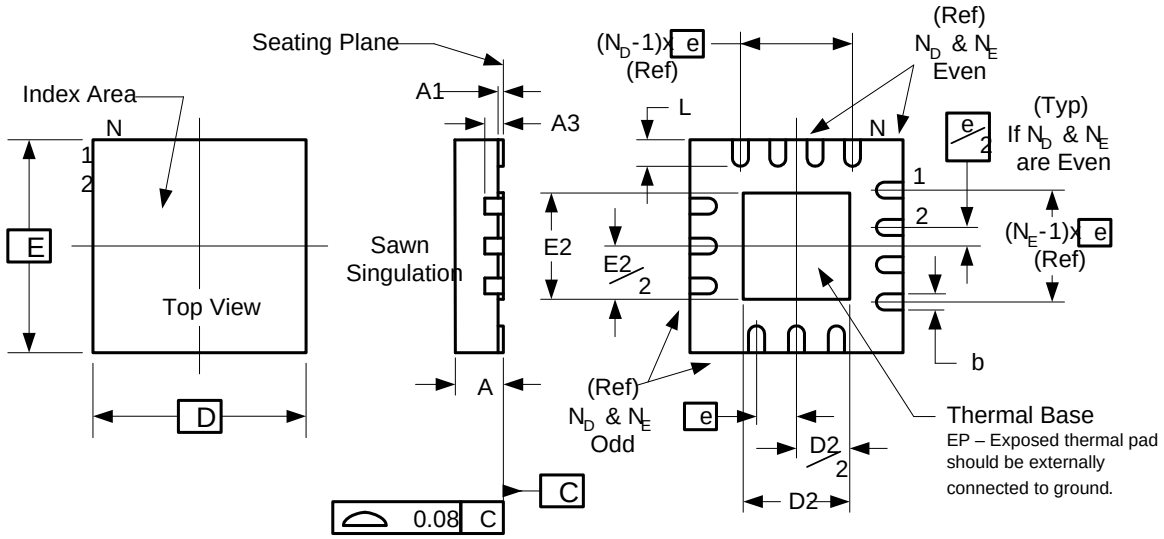


Dimensions	
X(max)	0.28
Yref	0.69
A(max)	2.78
G(min)	2.93
Z(max)	4.31
E2/D2(max)	2.63

Unit : mm

Package Outline and Package Dimensions (24-pin 4mm x 4mm QFN)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N	24	
N_D	6	
N_E	6	
D x E BASIC	4.00 x 4.00	
D2	2.3	2.55
E2	2.3	2.55
L	0.30	0.50

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5P49EE605NLGI	see page 22	Tubes	24pin VFQFPN	-40 to +85° C
5P49EE605NLGI8		Tape and Reel	24pin VFQFPN	-40 to +85° C

"G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A	R.Willner	6/02/10	Preliminary Datasheet release.
B	R.Willner	9/08/10	Updated thermal pad and dimensions on package drawing. Power ramp sequence.
C	R. Willner	10/29/10	Typographical changes. Loop filter calculations. Default register bit corrections.
D	R. Willner	01/19/11	Corrected notes on top-side marking.
E	R. Willner	04/13/11	1. Updated SCLK and SDA pin descriptions 2. Updated DC Electrical Char table for 1.8V LVTTL; added VIH and VIL. 3. Updated “Lock Time/PLL Lock Time from shutdown mode” Typ. and Max. specs in AC Timing Electrical Char table.
F	R. Willner	05/04/11	Added Landing Pattern diagram.
G	A.T.	09/30/11	Updated Power-up/Power-down Sequence notes.
H	R. Willner	10/17/11	1. Added VDDOx specs to Recommended Operations table 2. Updated Power-up/down Sequence diagrams

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