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ASM5P2304A

3.3 V Zero Delay Buffer

Description

ASM5P2304A is a versatile, 3.3 V zero−delay buffer designed to distribute high−speed clocks in PC, workstation, datacom, telecom and other high−performance applications. It is available in 8−pin package. The part has an on−chip PLL which locks to an input clock presented on the REF. The PLL feedback is required to be driven to FBK pin, and can be obtained from one of the outputs. The input−to−output propagation delay is guaranteed to be less than ±250 pS, and the output−to−output skew is guaranteed to be less than 200 pS.

ASM5P2304A has two banks of two outputs each. Multiple ASM5P2304A devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 500 pS.

ASM5P2304A is available in two different configurations. Refer to *ASM5P2304A Configurations Table*. The ASM5P2304A−1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path. The ASM5P2304A−1H is the high−drive version of the −1 and the rise and fall times on this device are faster.

ASM5P2304A−2 allows the user to obtain REF and 1/2x or 2x frequencies on each output bank. The exact configuration and output frequencies depend on which output drives the feedback pin.

Features

- Zero Input−Output Propagation Delay, Adjustable by Capacitive Load on FBK Input
- Multiple Configurations −
    Refer to *ASM5P2304A Configurations Table*
- Input Frequency Range: 10 MHz to 133 MHz
    − Multiple Low−skew Outputs
    − Output−Output Skew less than 200 pS
    − Device−Device Skew less than 500 pS
    − Two Banks of Two Outputs Each
- Less than 200 pS Cycle−to−Cycle Jitter
    (−1, −1H, −2, −2H)
- 8−pin SOIC Package
- 3.3 V Operation
- Commercial and Industrial Temperature Range
- Advanced 0.35 !! CMOS Technology
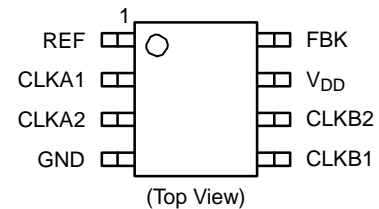- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

ON Semiconductor®

http://onsemi.com

SOIC−8
S SUFFIX
CASE 751BD

PIN CONFIGURATION

REF	1	FBK
CLKA1		V$_{DD}$
CLKA2		CLKB2
GND		CLKB1

(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.
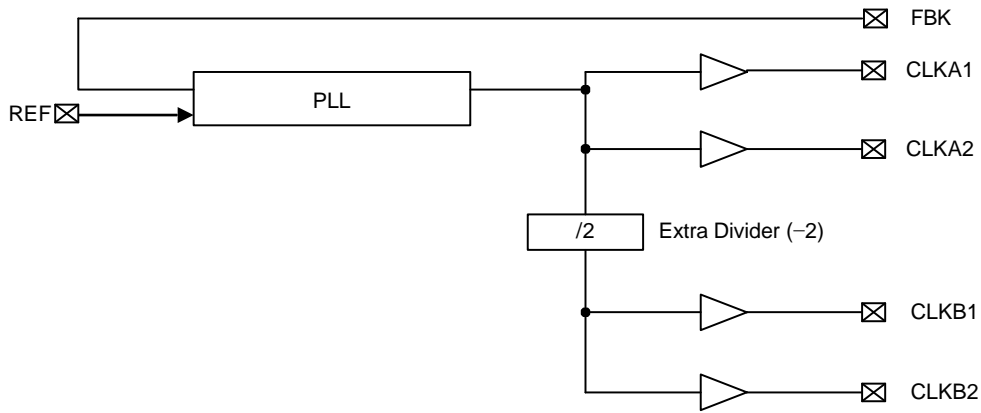
ASM5P2304A

Figure 1. Block Diagram

Table 1. ASM5P2304A CONFIGURATIONS

Device	Feedback From	Bank A Frequency	Bank B Frequency
ASM5P2304A (−1, 1H)	Bank A or Bank B	Reference	Reference
ASM5P2304A (−2, −2H)	Bank A	Reference	Reference /2
ASM5P2304A (−2, −2H)	Bank B	2 x Reference	Reference

Zero Delay and Skew Control

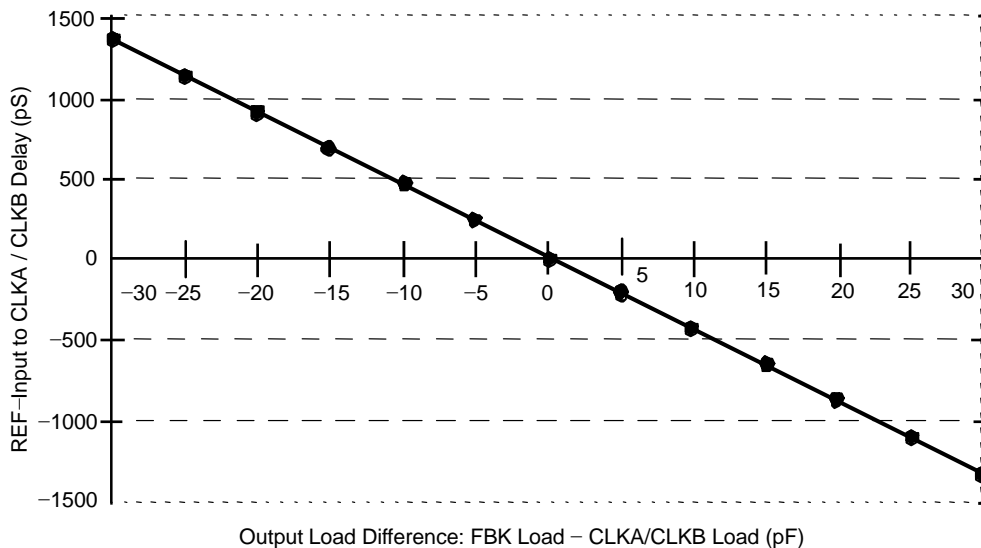For applications requiring zero input−output delay, all outputs must be equally loaded.

Figure 2. REF Input to CLKA/CLKB Delay vs. Difference in Loading between FBK Pin and CLKA/CLKB Pins

To close the feedback loop of the ASM5P2304A, the FBK pin can be driven from any of the four available clock outputs. The output driving the FBK pin will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input−output delay. This is shown in the above graph.

For applications requiring zero input−output delay, all outputs including the one providing feedback should be equally loaded. If input−output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs. For zero output−output skew, be sure to load outputs equally.

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Table 2. PIN DESCRIPTION

Pin #	Pin Name	Description
1	REF (Note 1)	Input reference clock frequency, 5 V tolerant input
2	CLKA1 (Note 2)	Buffered clock output, bank A
3	CLKA2 (Note 2)	Buffered clock output, bank A
4	GND	Ground
5	CLKB1 (Note 2)	Buffered clock output, bank B
6	CLKB2 (Note 2)	Buffered clock output, bank B
7	V_{DD}	3.3 V supply
8	FBK	PLL feedback input

1. Weak pull−down.
2. Weak pull−down on all outputs.

Table 3. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	−0.5	+4.6	V
DC Input Voltage (Except REF)	−0.5	V_{DD} + 0.5	V
DC Input Voltage (REF)	−0.5	7	V
Storage Temperature	−65	+150	°C
Max. Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (As per JEDEC STD22− A114−B)		2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Table 4. OPERATING CONDITIONS

Parameter	Description		Min	Max	Unit
V_{DD}	Supply Voltage		3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	Commercial temperature	0	70	°C
		Industrial temperature	−40	85	
C_L	Load Capacitance, below 100 MHz			30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz			15	pF
C_{IN}	Input Capacitance (Note 3)			7	pF

3. Applies to both Ref Clock and FBK.

Table 5. ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions		Min	Max	Unit
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage			2.2		V
I_{IL}	Input LOW Current	$V_{IN} = 0\ V$			50	!!A
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$			100	!!A
V_{OL}	Output LOW Voltage (Note 4)	$I_{OL} = 8\ mA\ (−1, −2)$ $I_{OL} = 12\ mA\ (−1H, −2H)$			0.4	V
V_{OH}	Output HIGH Voltage (Note 4)	$I_{OH} = −8\ mA\ (−1, −2)$ $I_{OH} = −12\ mA\ (−1H, −2H)$		2.4		V
I_{DD}	Supply Current	Unloaded outputs @ 100 MHz	Commercial temp.		35	mA
			Industrial temp.		40	
		Unloaded outputs @ 66 MHz, (−1, −1H, −2, −2H)	Commercial temp.		25	
			Industrial temp.		30	
		Unloaded outputs @ 33 MHz, (−1, −1H, −2, −2H)	Commercial temp.		16	
			Industrial temp.		20	

4. Parameter is guaranteed by design and characterization. Not 100% tested in production.

ASM5P2304A

Table 6. SWITCHING CHARACTERISTICS (Notes 5, 6)

Parameter	Test Conditions		Min	Typ	Max	Unit
Output Frequency	30 pF load	(−1, −1H) devices	10		100	MHz
		(−2, −2H) devices	12		100	
	15 pF load	(−1, −1H) devices	10		133	
		(−2, −2H) devices	12		133	
Duty Cycle (Note 7) (−1, −2, −1H, −2H)	Measured at 1.4 V, F_{OUT} < 66.66 MHz, 30 pF load		40	50	60	%
Duty Cycle (Note 7) (−1, −2,−1H, −2H)	Measured at 1.4 V, F_{OUT} ≤ 50 MHz, 15 pF load		45	50	55	%
Output Rise Time (Note 7) (−1, −2)	Measured between 0.8 V and 2.0 V, 30 pF load	Commercial temp.			2.2	nS
		Industrial temp.			2.5	
Output Rise Time (Note 7) (−1H, −2H)	Measured between 0.8 V and 2.0 V, 30 pF load	Commercial temp., Industrial temp.		1.5	2	nS
Output Rise Time (Note 7) (−1, −2)	Measured between 0.8 V and 2.0 V, 15 pF load				1.5	nS
Output Fall Time (Note 7) (−1, −2)	Measured between 2.0 V and 0.8 V, 30 pF load	Commercial temp.			2.2	nS
		Industrial temp.			2.5	
Output Fall Time (Note 7) (−1H, −2H)	Measured between 2.0 V and 0.8 V, 30 pF load	Commercial temp., Industrial temp.		1.25	1.5	nS
Output Fall Time (Note 7) (−1, −2)	Measured between 2.0 V and 0.8 V, 15 pF load				1.5	nS
Output−to−output skew on same bank (−1, −1H, −2, −2H) (Note 7)	All outputs equally loaded				200	pS
Output bank A −to− output bank B skew (−1, −1H)	All outputs equally loaded				200	
Output bank A to output Bank B skew (−2, −2H) (Note 7)	All outputs equally loaded				400	
Delay, REF Rising Edge to FBK Rising Edge (Note 7)	Measured at V_{DD} /2			0	±250	pS
Device−to−Device Skew (Note 7)	Measured at V_{DD}/2 on the FBK pins of the device			0	500	pS
Cycle−to−Cycle Jitter (Note 7)	(−1, −1H)	Measured at 66.67 MHz, loaded outputs, 15 pF load			180	pS
		Measured at 66.67 MHz, loaded outputs, 30 pF load			200	
		Measured at 133 MHz, loaded outputs, 15 pF load			125	
	(−2, −2H)	Measured at 66.67 MHz, loaded outputs, 15 pF load			380	
		Measured at 66.67 MHz, loaded outputs, 30 pF load			400	
PLL Lock Time (Note 7)	Stable power supply, valid clock presented on REF and FBK pins				1.0	mS

5. For all measurements use Test Circuit #1.
6. All parameters are specified at Commercial and Industrial temperature unless stated otherwise.
7. Parameter is guaranteed by design and characterization. Not 100% tested in production.
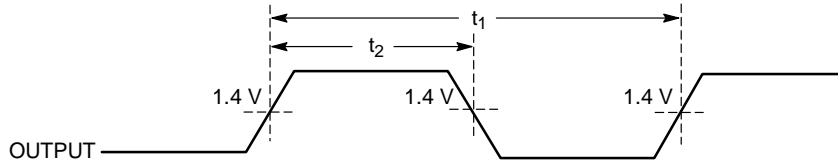
ASM5P2304A

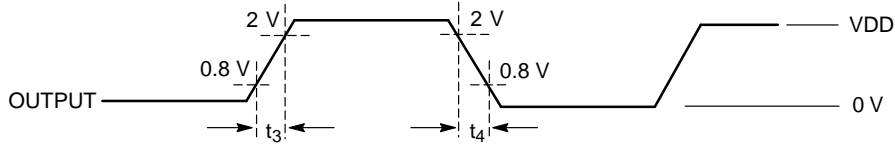**Switching Waveforms**

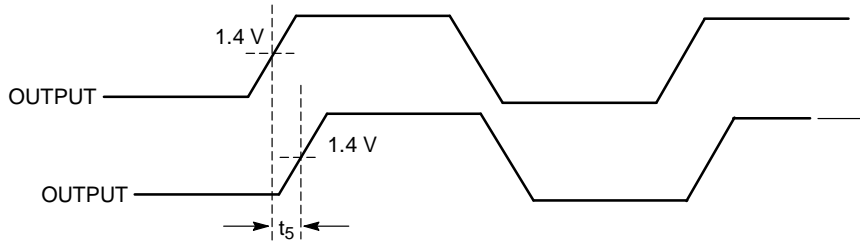**Figure 3. Duty Cycle Timing**

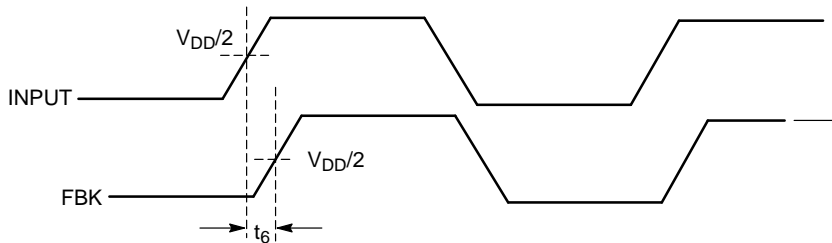**Figure 4. All Outputs Rise/Fall Time**

Figure 5. Output−Output Skew
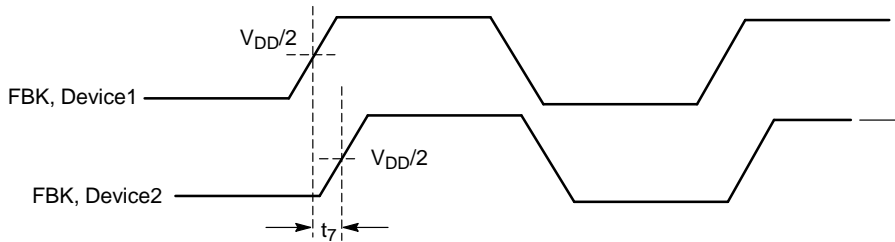

Figure 6. Input−Output Propagation Delay
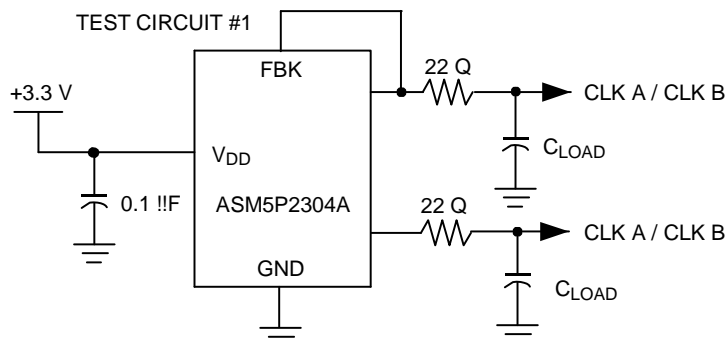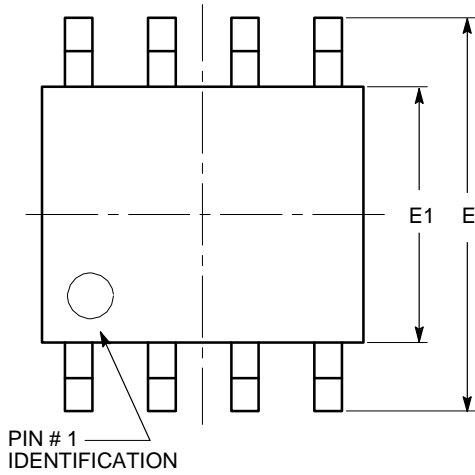

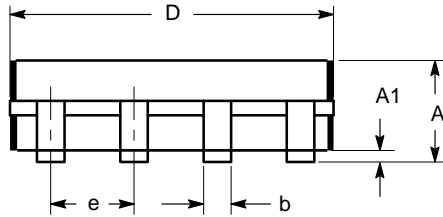
Figure 7. Device−Device Skew

Figure 8. Test Circuit

ASM5P2304A

PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

PIN # 1
IDENTIFICATION

TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º

SIDE VIEW
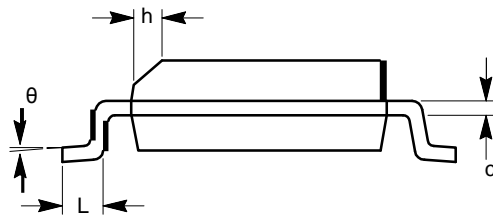
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

ASM5P2304A

Part Number	Marking	Package Type	Temperature
P5P2304AF−1−08SR	5P2304AF−1	8−pin 150−mil SOIC−TAPE & REEL, Pb free	Commercial
ASM5P2304AF−1−08−ST	5P2304AF−1	8−pin 150−mil SOIC−TUBE, Pb free	Commercial
ASM5I2304AF−1−08−SR	5I2304AF−1	8−pin 150−mil SOIC−TAPE & REEL, Pb free	Industrial
ASM5I2304AF−1−08−ST	5I2304AF−1	8−pin 150−mil SOIC−TUBE, Pb free	Industrial
P5P2304AF−1H08SR	5P2304AF−1H	8−pin 150−mil SOIC−TAPE & REEL, Pb free	Commercial
ASM5P2304AF−1H−08−ST	5P2304AF−1H	8−pin 150−mil SOIC−TUBE, Pb free	Commercial
P5I2304AF−1H08SR	5I2304AF−1H	8−pin 150−mil SOIC−TAPE & REEL, Pb free	Industrial
ASM5I2304AF−1H−08−ST	5I2304AF−1H	8−pin 150−mil SOIC−TUBE, Pb free	Industrial
P5P2304AF−2−08SR	5P2304AF−2	8−pin 150−mil SOIC−TAPE & REEL, Pb free	Commercial
P5P2304AF−2−08ST	5P2304AF−2	8−pin 150−mil SOIC−TUBE, Pb free, Pb free	Commercial
ASM5I2304AF−2−08−SR	5I2304AF−2	8−pin 150−mil SOIC−TAPE & REEL, Pb free	Industrial
P5I2304AF−2−08ST	5I2304AF−2	8−pin 150−mil SOIC−TUBE, Pb free	Industrial
ASM5P2304AF−2H−08−SR	5P2304AF−2H	8−pin 150−mil SOIC−TAPE & REEL, Pb free	Commercial
ASM5P2304AF−2H−08−ST	5P2304AF−2H	8−pin 150−mil SOIC−TUBE, Pb free	Commercial
ASM5I2304AF−2H−08−SR	5I2304AF−2H	8−pin 150−mil SOIC−TAPE & REEL, Pb free	Industrial
ASM5I2304AF−2H−08−ST	5I2304AF−2H	8−pin 150−mil SOIC−TUBE, Pb free	Industrial