

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

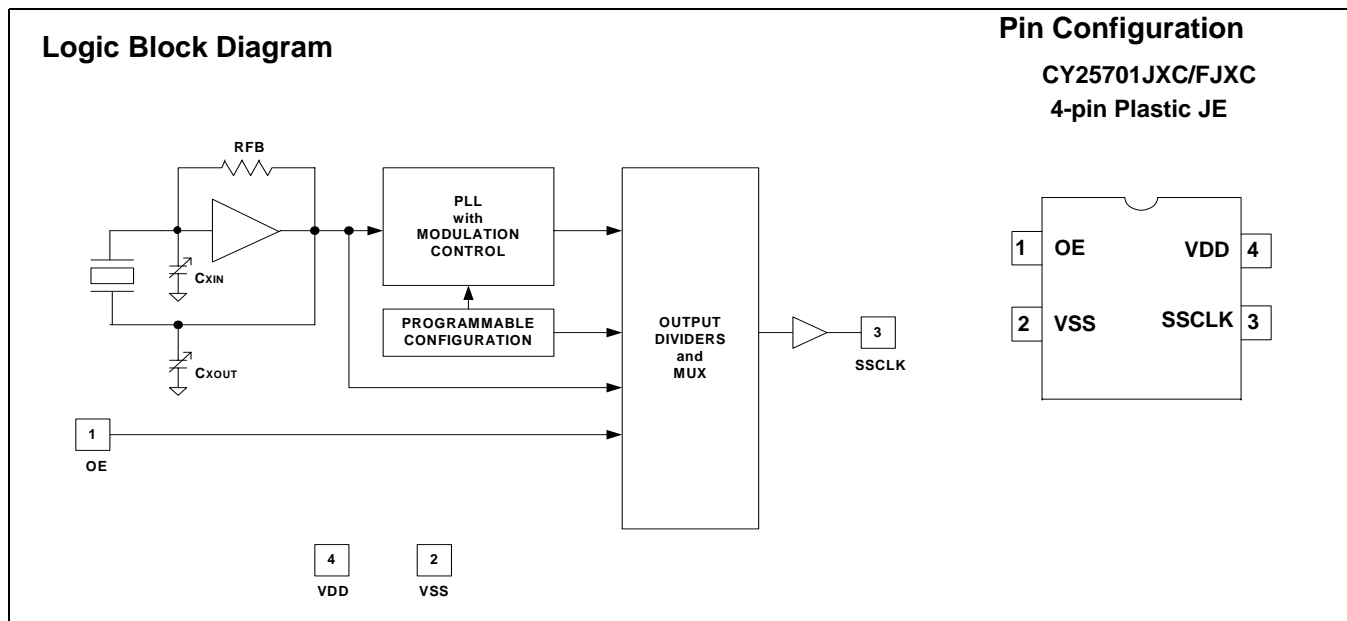
Programmable High-Frequency Crystal Oscillator with Spread Spectrum (SSXO) and No-Spread Spectrum (XO) Option

Features

- Crystal Oscillator with Spread Spectrum Clock (SSXO)
- No-Spread Spectrum (XO) Option
- Wide operating output clock frequency range of 10–166 MHz
- Programmable spread spectrum with nominal 31.5-kHz modulation frequency
- Center spread: $\pm 0.25\%$ to $\pm 2.0\%$
- Down spread: -0.5% to -4.0%
- No spread: $\pm 0.0\%$
- Integrated phase-locked loop (PLL)
- 85 ps typical cycle-to-cycle Jitter with SSCLK = 133MHz
- 3.3V operation
- Output Enable function
- Package available in 4-pin Plastic JE
- Pb-free package

Benefits

- Provides wide range of spread percentages for maximum electromagnetic interference (EMI) reduction, to meet regulatory agency electromagnetic compliance (EMC) requirements. Reduces development and manufacturing costs and time-to-market.
- This versatile programming feature enables the users to switch between SSXO (with Spread) and XO (without Spread) functions with ease.
- Internal PLL to generate up to 166-MHz output.
- Suitable for most PC, consumer, and networking applications
- Application compatibility in standard and low-power systems
- In-house programming of samples and prototype quantities is available using the CY3672 programming kit and CY3613 (JEC package) socket adapters. Production quantities are available through Cypress' value-added distribution partners or by using third-party programmers from BP Microsystems, HiLo Systems, and others.



Pin Definition

Pin	Name	Description
1	OE	Output Enable pin: Active HIGH. If OE = 1, SSCLK is enabled.
2	VSS	Power supply ground.
3	SSCLK	Spread spectrum clock output (with or without spread).
4	VDD	3.3V power supply.

Functional Description

The CY25701JXC/FJXC is a Spread Spectrum Crystal Oscillator (SSXO) IC used for the purpose of reducing EMI found in today's high-speed digital electronic systems.

The device uses a Cypress proprietary PLL and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the embedded input crystal. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies are greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency (EMC) requirements and improve time-to-market without degrading system performance.

The CY25701JXC/FJXC uses a programmable configuration memory array to synthesize output frequency and spread%.

The spread% is programmed to either center spread or down spread with various spread percentages. The range for center spread is from $\pm 0.25\%$ to $\pm 2.00\%$. The range for down spread is from -0.5% to -4.0% . Contact the factory for smaller or larger spread% amounts if required. Refer to *Table 2* for spread selection and no-spread values.

The frequency modulated SSCLK output can be programmed from 10–166 MHz.

The CY25701JXC/FJXC is available in a 4-pin plastic package with operating temperature range of -20 to 70°C .

Programming Description

Field/Factory-Programmable CY25701JXC/FJXC

Field/Factory programming is available for samples and manufacturing by Cypress and its distributors. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. Once the request has been processed, you will receive a new part number, samples, and data sheet with the programmed values. This part number will be used for additional sample requests and production orders.

Additional information on the CY25701JXC/FJXC can be obtained from the Cypress web site at www.cypress.com.

Output Frequency, SSCLK Output (SSCLK, pin 3)

The modulated frequency at the SSCLK output is produced by synthesizing from the embedded crystal oscillator frequency input. The range of synthesized clock is from 10–166 MHz.

Spread Percentage (SSCLK, pin 3)

The SSCLK spread can be programmed to various spread percentage values from $\pm 0.25\%$ to $\pm 2.0\%$ for Center Spread and from -0.5% to -4.0% for Down Spread. Refer to *Table 2* for available spread options. Enter $\pm 0.0\%$ (No spread) for XO (Crystal Oscillator) without spread option.

Frequency Modulation (SSCLK, pin 3)

The frequency modulation is programmed at 31.5 kHz for all SSCLK frequencies from 10 to 166 MHz. Contact the factory if a higher-modulation frequency is required.

Table 1. Programming Data Requirement

Pin Function	Output Frequency	Spread Percent Code ^[1]	Frequency Modulation
Pin Name	SSCLK	SSCLK	SSCLK
Pin#	3	3	3
Units	MHz	%	kHz
Program Value	ENTER DATA	ENTER DATA	31.5

Table 2. Spread Percent Selection

Center Spread	Code	A	B	C	D	E	F	Z
	Percentage	$\pm 0.25\%$	$\pm 0.5\%$	$\pm 0.75\%$	$\pm 1.0\%$	$\pm 1.5\%$	$\pm 2.0\%$	$\pm 0.0\%$
Down Spread	Code	G	H	J	K	L	M	Z
	Percentage	-0.5%	-1.0%	-1.5%	-2.0%	-3.0%	-4.0%	$\pm 0.0\%$

Note:

1. $\pm 0.0\%$ or Code "Z" for XO (No-Spread) option.

Absolute Maximum Rating

Supply Voltage (VDD) -0.5V to +7.0V
 DC Input Voltage -0.5V to V_{DD} + 0.5V

Storage Temperature (Non-condensing) -55°C to +100°C
 Junction Temperature -40°C to +125°C
 Data Retention @ T_j = 125°C > 10 years
 Package Power Dissipation 350 mW

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	3.00	3.30	3.60	V
T _A	Ambient Temperature	-20	-	70	°C
C _{LOAD}	Max. Load Capacitance @ pin 3	-	-	15	pF
F _{SSCLK}	SSCLK output frequency, C _{LOAD} = 15 pF	10	-	166	MHz
F _{MOD}	Spread Spectrum Modulation Frequency	30.0	31.5	33.0	kHz
T _{PU}	Power-up time for VDD to reach minimum specified voltage (power ramp must be monotonic)	0.05	-	500	ms

DC Electrical Characteristics

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
I _{OH}	Output High Current (pin 3)	V _{OH} = V _{DD} - 0.5, V _{DD} = 3.3V (source)	10	12	-	mA
I _{OL}	Output Low Current (pin 3)	V _{OL} = 0.5, V _{DD} = 3.3V (sink)	10	12	-	mA
V _{IH}	Input High Voltage (pin 1)	CMOS levels, 70% of V _{DD}	0.7V _{DD}	-	V _{DD}	V
V _{IL}	Input Low Voltage (pin 1)	CMOS levels, 30% of V _{DD}	V _{SS}	-	0.3V _{DD}	V
I _{IH}	Input High Current (pin 1)	V _{in} = V _{DD}	-	-	10	μA
I _{IL}	Input Low Current (pin 1)	V _{in} = V _{SS}	-	-	10	μA
I _{OZ}	Output Leakage Current (pin 3)	Three-state output, OE = 0	-10	-	10	μA
C _{IN} ^[2]	Input Capacitance (pin 1)	Pin 1, or OE	-	5	7	pF
I _{VDD}	Supply Current	V _{DD} = 3.3V, SSCLK = 10 to 166 MHz, C _{LOAD} = 0, OE = V _{DD}	-	-	50	mA
Δf	Aging	T _A = 25°C, First year	-5	-	5	ppm

AC Electrical Characteristics^[2]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	SSCLK, Measured at V _{DD} /2	45	50	55	%
t _R	Output Rise Time	20%–80% of V _{DD} , C _L = 15 pF	-	-	2.7	ns
t _F	Output Fall Time	20%–80% of V _{DD} , C _L = 15 pF	-	-	2.7	ns
T _{CCJ1} ^[3]	Cycle-to-Cycle Jitter SSCLK (Pin 3)	SSCLK ≥ 133 MHz, Measured at V _{DD} /2	-	85	200	ps
		25 MHz ≤ SSCLK < 133 MHz, Measured at V _{DD} /2	-	215	400	ps
		SSCLK < 25 MHz, Measured at V _{DD} /2	-	-	1% of 1/SSCK	s
T _{OE1}	Output Disable Time (pin1 = OE)	Time from falling edge on OE to stopped outputs (Asynchronous)	-	150	350	ns
T _{OE2}	Output Enable Time (pin1 = OE)	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	-	150	350	ns
T _{LOCK}	PLL Lock Time	Time for SSCLK to reach valid frequency	-	-	10	ms

Notes:

- Guaranteed by characterization, not 100% tested.
- Jitter is configuration dependent. Actual jitter is dependent on output frequencies, spread percentage, temperature, and output load. For more information, refer to the application note, "Jitter in PLL Based Systems: Causes, Effects, and Solutions" available at <http://www.cypress.com/clock/appnotes.html>, or contact your local Cypress Field Application Engineer.

Application Circuit

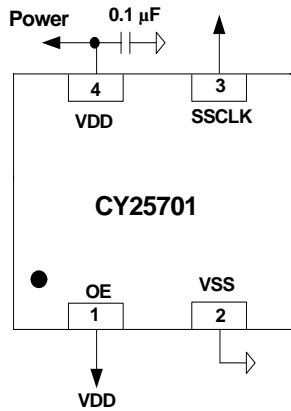


Figure 1. Application Circuit Diagram

Switching Waveforms

Duty Cycle Timing ($DC = t_{1A}/t_{1B}$)

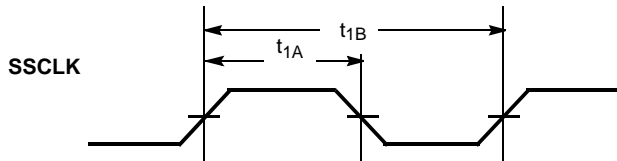
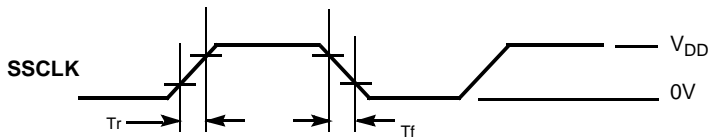


Figure 2. Duty Cycle Waveform

Output Rise/Fall Time



Output Rise time ($T_r = (0.6 \times V_{DD})/SR1$ (or SR3)
 Output Fall time ($T_f = (0.6 \times V_{DD})/SR2$ (or SR4)
 Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

Figure 3. Output Rise/Fall Time Waveform

Output Enable/Disable Timing

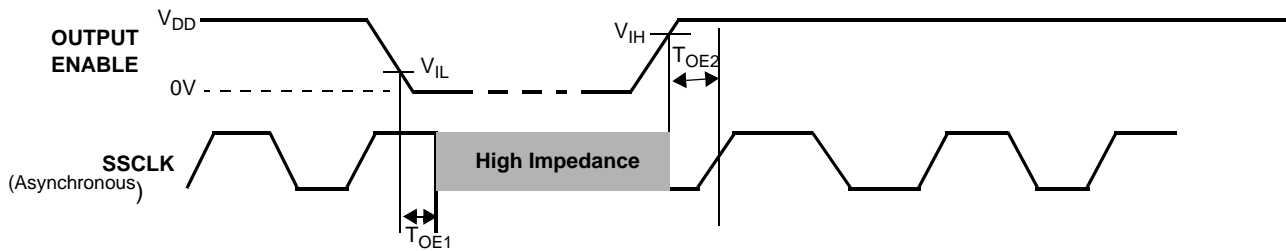
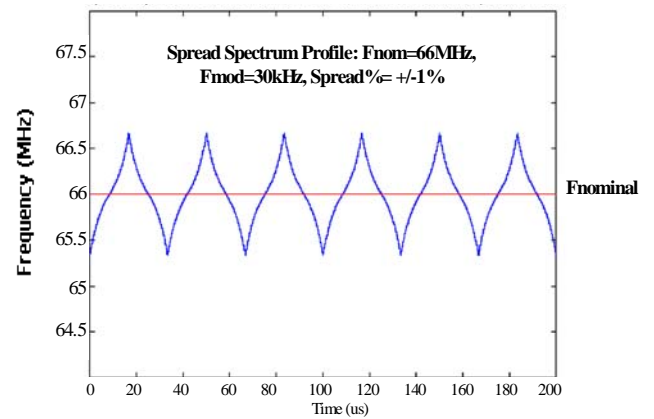
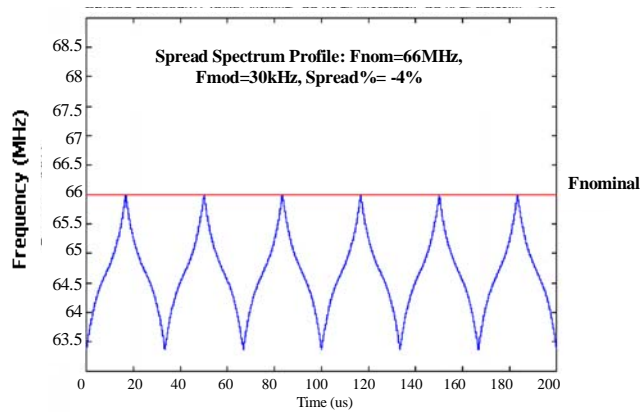
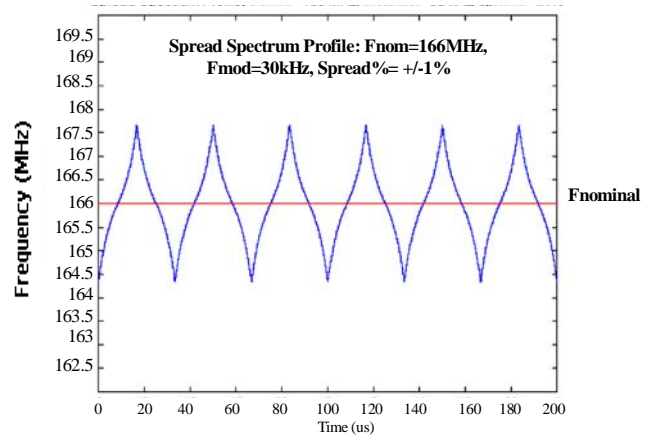
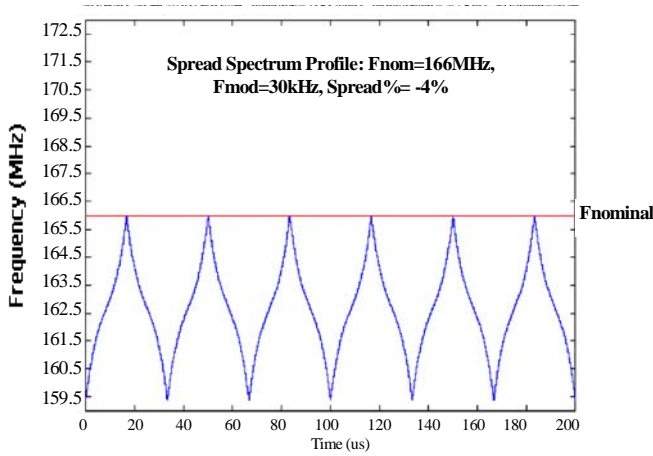


Figure 4. Output Enable/Disable Timing Waveforms

Informational Graphs [4]



Ordering Information

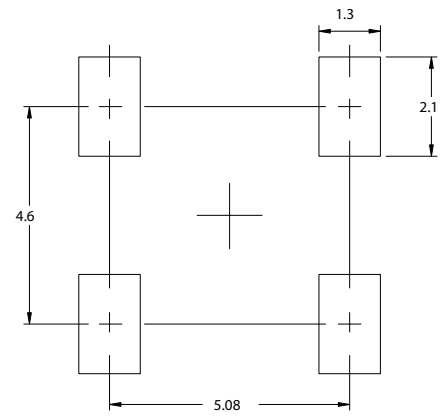
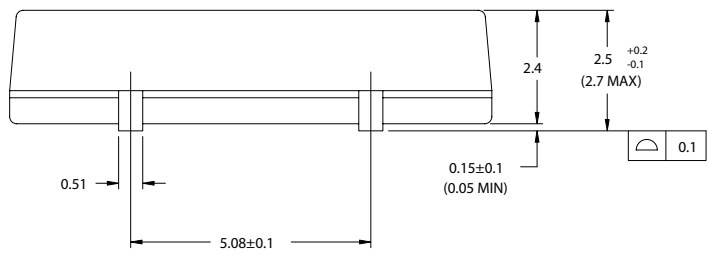
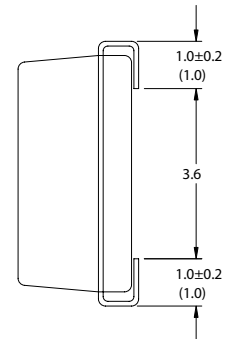
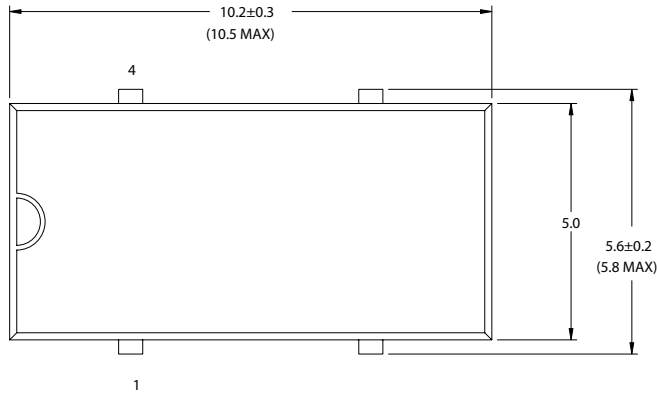
Part Number ^[5,6]	Package description	Product Flow
Lead-free (Pb-free)		
CY25701JXC-ZZZ	4-Lead Plastic JE SMD	Commercial, -20° to 70°C
CY25701JXC-ZZZT	4-Lead Plastic JE SMD - Tape and Reel	Commercial, -20° to 70°C
CY25701FJXC	4-Lead Plastic JE SMD	Commercial, -20° to 70°C
CY25701FJXCCT	4-Lead Plastic JE SMD - Tape and Reel	Commercial, -20° to 70°C

Notes:

- The "Informational Graphs" are meant to convey the typical performance levels. No performance specifications is implied or guaranteed. Refer to the tables on pages 4 and 5 for device specifications.
- "ZZZ" denotes the assigned product dash number. This number will be assigned by factory after the output frequency and spread percent programming data is received from the customer.
- "FJXC" suffix is used for products programmed in field by Cypress distributors.

Package Drawings and Dimensions

4-Lead (10.2x5.6mm) JEC JE04A



DIMENSIONS IN MILLIMETERS
 REFERENCE JEDEC: N/A
 PKG. WEIGHT: 0.24 gms

RECOMMENDED SOLDERING PATTERN

51-85204-*A

All product and company names mentioned in this document are the trademarks of their respective holders.

Document History Page

Document Title: CY25701JXC/FJXC Programmable High-Frequency Crystal Oscillator with Spread Spectrum (SSXO) and No-Spread Spectrum (XO) Option
Document Number: 38-07684

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	224108	See ECN	RGL	New data sheet
*A	258974	See ECN	RGL	Corrected the product suffix (lead-free) in the ordering information table Added note 4
*B	279379	See ECN	RGL	Added ordering part numbers
*C	392505	See ECN	RGL	Added 4pin LCC SMD package
*D	414085	See ECN	RGL	Added Spread OFF (XO) programming function Edited CY3724 socket adapter
*E	436961	See ECN	RGL	Changed the Marketing part number from CY25701 to CY25701JXC/FJXC Removed all Ceramic Package references