

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

NBVSPA015 Series

3.3 V, LVDS Voltage-Controlled Clock Oscillator (VCXO) PureEdge™ Product Series

The NBVSPXXXX voltage-controlled crystal oscillator (VCXO) devices are designed to meet today's requirements for 3.3 V LVDS clock generation applications. These devices use a high Q fundamental mode crystal and Phase Locked Loop (PLL) multiplier to provide a wide range of frequencies from 60 MHz to 700 MHz (factory configurable per user specifications) with a pullable range of ± 100 ppm and a frequency stability of ± 50 ppm. The silicon-based PureEdge™ products design provides users with exceptional frequency stability and reliability. They produce an ultra low jitter and phase noise LVDS differential output.

The NBVSPXXXX series devices are a member of ON Semiconductor's PureEdge™ clock family that provides accurate and precision clock generation solutions.

Available in the industry standard 5.0 x 7.0 x 1.8 mm and in a new smaller 3.2 x 5.0 x 1.2 mm SMD (CLCC) package on 16 mm tape and reel in quantities of 1,000.

Features

- LVDS Differential Output
- Uses High Q Fundamental Mode Crystal
- Ultra Low Jitter and Phase Noise – 0.5 ps (12 kHz – 20 MHz)
- Factory Configurable Frequencies from 60 MHz to 700 MHz (see Standard Frequencies in the Ordering Information Table on page 6)
- Pullable Range Minimum of ± 100 ppm
- Frequency Stability of ± 50 ppm
- Control Voltage with Positive Slope
- Voltage Control Linearity of $\pm 10\%$
- Hermetically Sealed Ceramic SMD Packages of size 5.0 x 7.0 x 1.8 mm and 3.2 x 5.0 x 1.2 mm
- Operating Range: 3.3 V $\pm 10\%$
- These Devices are Pb-Free and are RoHS Compliant

Applications

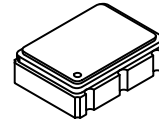
- Networking
- SONET
- 10 Gigabit Ethernet
- Networking Base Stations
- Broadcasting



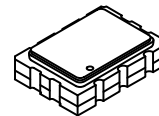
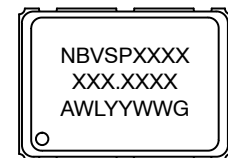
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS



6 PIN CLCC
LN SUFFIX
CASE 848AB



6 PIN CLCC
LU SUFFIX
CASE 848AC



NBVSPXXXX = NBVSPXXXX (± 50 ppm)
XXX.XXXX = Output Frequency (MHz)
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NBVSPA015 Series

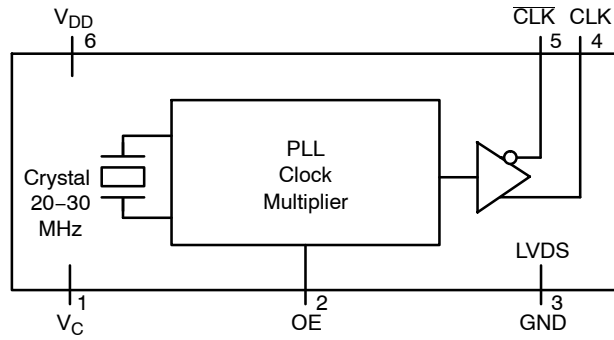


Figure 1. Simplified Logic Diagram

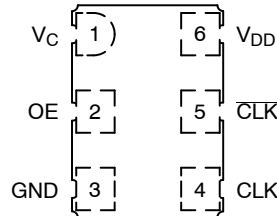


Figure 2. Pin Connections (Top View)

Table 1. PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	V_C (Note 1)	Analog Input	Analog control voltage input pin that adjusts output oscillation frequency. $f_0 = V_C = 1.65 \text{ V}$
2	OE	LVTTL/LVCMOS Control Input	Output Enable Pin. When left floating pin defaults to logic HIGH and output is active. See OE pin description Table 2.
3	GND	Power Supply	Ground at 0 V. Electrical and Case Ground.
4	CLK	LVDS Output	Non-Inverted Clock Output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
5	$\overline{\text{CLK}}$	LVDS Output	Inverted Clock Output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
6	V_{DD}	Power Supply	Positive Power Supply Voltage. Voltage should not exceed 3.3 V $\pm 10\%$.

1. Control voltage has a positive slope with a typical linearity of $\pm 10\%$; $V_C = 1.65 \text{ V} \pm 1 \text{ V}$.

Table 2. OUTPUT ENABLE TRI-STATE FUNCTION

OE Pin	Output Pins
Open	Active
HIGH Level	Active
LOW Level	High Z

Table 3. ATTRIBUTES

Characteristic	Value
Input Default State Resistor	170 k Ω
ESD Protection	Human Body Model Machine Model
	2 kV 200 V
Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test	

2. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

NBVSPA015 Series

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{DD}	Positive Power Supply	GND = 0 V		4.6	V
V _{IN}	Control Input (V _C and OE)		V _{IN} ≤ V _{DD} + 200 mV V _{IN} ≥ GND - 200 mV		V
I _{OSC}	Output Short Circuit Current CLK to $\overline{\text{CLK}}$ CLK or $\overline{\text{CLK}}$ to GND	Continuous Continuous		12 24	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-55 to +120	°C
T _{sol}	Wave Solder	See Figure 4		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. DC CHARACTERISTICS (V_{DD} = 3.3 V ±10%, GND = 0 V, T_A = -40°C to +85°C) (Note 3)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Units
I _{DD}	Power Supply Current			75	100	mA
V _{IH}	OE and FSEL Input HIGH Voltage		2000		V _{DD}	mV
V _{IL}	OE and FSEL Input LOW Voltage		GND - 300		800	mV
I _{IH}	Input HIGH Current OE		-100		+100	μA
I _{IL}	Input LOW Current OE		-100		+100	μA
ΔV _{OD}	Change in Magnitude of V _{OD} for Complementary Output States	(Note 4)	0	1	25	mV
V _{OS}	Offset Voltage		1125		1375	mV
ΔV _{OS}	Change in Magnitude of V _{OS} for Complementary Output States	(Note 4)	0	1	25	mV
V _{OH}	Output HIGH Voltage			1425	1600	mV
V _{OL}	Output LOW Voltage		900	1075		mV
V _{OD}	Differential Output Voltage		250		450	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Measurement taken with outputs terminated with 100 ohm across differential pair. See Figure 3.
4. Parameter guaranteed by design verification not tested in production.

NBVSPA015 Series

Table 6. AC CHARACTERISTICS ($V_{DD} = 3.3 \pm 10\%$, $GND = 0 V$, $T_A = -40^\circ C$ to $+85^\circ C$) (Note 5)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Units
f_{CLKOUT}	Output Clock Frequency	NBVSPA019		125.00		MHz
		NBVSPA027		148.50		
		NBVSPA018		155.52		
		NBVSPA017		156.25		
		NBVSPA024		160.00		
		NBVSPA015		200.00		
		NBVSPA042		74.25		
Δf	Frequency Stability – NBVSPAXXX	(Note 6)			± 50	ppm
$t_{jit}(\phi)$	RMS Phase Jitter	12 kHz to 20 MHz		0.4	0.9	ps
t_{jitter}	Cycle to Cycle, RMS	1000 Cycles		3	8	ps
	Cycle to Cycle, Peak-to-Peak	1000 Cycles		15	30	ps
	Period, RMS	10,000 Cycles		2	4	ps
	Period, Peak-to-Peak	10,000 Cycles		10	20	ps
$t_{OE/OD}$	Output Enable/Disable Time				200	ns
F_P	Crystal Pullability (Note 7)	$0 V \leq V_C \leq 3.3 V$	± 100			ppm
$V_{C(bw)}$	Control Voltage Bandwidth	-3 dB	20			KHz
t_{DUTY_CYCLE}	Output Clock Duty Cycle (Measured at Cross Point)		45	50	55	%
t_R	Output Rise Time (20% and 80%)			245	400	ps
t_F	Output Fall Time (80% and 20%)			245	400	ps
t_{start}	Start-up Time			1	5	ms
	Aging	1 st Year			3	ppm
		Every Year After 1 st			1	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Measurement taken with outputs terminated with 100 ohm across differential pair. See Figure 3.
6. Parameter guarantees 10 years of aging. Includes initial stability at 25°C, shock, vibration and first year aging.
7. Gain transfer is positive with a rate of 130 ppm/V.

Table 7. PHASE NOISE PERFORMANCE FOR NBVSPXXXX

Parameter	Characteristic	Condition	74.25 MHZ	125.00 MHZ	148.50 MHZ	155.52 MHZ	156.25 MHZ	160.00 MHZ	200.00 MHZ	Units
ϕ_{NOISE}	Output Phase-Noise Performance	100 Hz of Carrier	-94	-90	-90	-90	-90	-90	-91	dBc/Hz
		1 kHz of Carrier	-122	-117	-116	-116	-116	-116	-117	dBc/Hz
		10 kHz of Carrier	-132	-128	-126	-126	-126	-126	-127	dBc/Hz
		100 kHz of Carrier	-132	-128	-126	-126	-126	-126	-127	dBc/Hz
		1 MHz of Carrier	-142	-136	-136	-134	-134	-135	-135	dBc/Hz
		10 MHz of Carrier	-160	-159	-159	-159	-159	-159	-159	dBc/Hz

NBVSPA015 Series

Table 8. RELIABILITY COMPLIANCE

Parameter	Standard	Method
Shock	Mechanical	MIL-STD-833, Method 2002, Condition B
Solderability	Mechanical	MIL-STD-833, Method 2003
Vibration	Mechanical	MIL-STD-833, Method 2007, Condition A
Solvent Resistance	Mechanical	MIL-STD-202, Method 215
Thermal Shock	Environment	MIL-STD-833, Method 1011, Condition A
Moisture Level Sensitivity	Environment	MSL1 260°C per IPC/JEDEC J-STD-020D

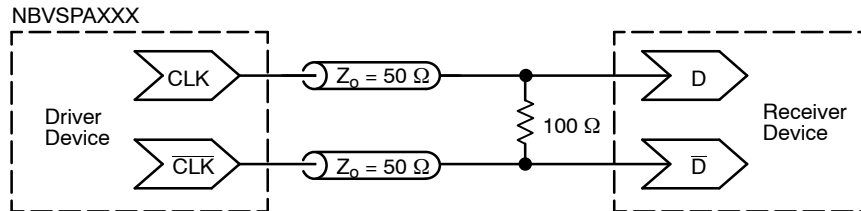


Figure 3. Typical Termination for Output Driver and Device Evaluation

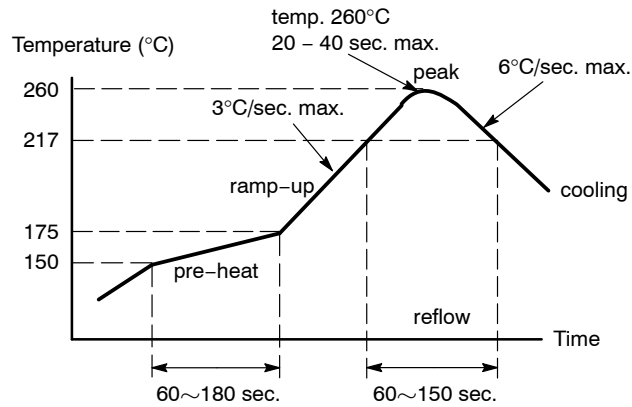


Figure 4. Recommended Reflow Soldering Profile

NBVSPA015 Series

Table 9. ORDERING INFORMATION

Device	Output Frequency (MHz)	Package	Shipping [†]
5.0 x 7.0 x 1.8 mm			
NBVSPA017LN1TAG	156.2500	CLCC-6, Pb-Free	1000 / Tape & Reel
NBVSPA018LN1TAG	155.5200	CLCC-6, Pb-Free	1000 / Tape & Reel
NBVSPA024LN1TAG	160.0000	CLCC-6, Pb-Free	1000 / Tape & Reel
NBVSPA015LN1TAG	200.0000	CLCC-6, Pb-Free	1000 / Tape & Reel
NBVSPA027LN1TAG	148.5000	CLCC-6, Pb-Free	1000 / Tape & Reel
NBVSPA019LN1TAG	125.0000	CLCC-6, Pb-Free	1000 / Tape & Reel
NBVSPA042LN1TAG	74.2500	CLCC-6, Pb-Free	1000 / Tape & Reel
3.2 x 5.0 x 1.2 mm			
NBVSPA017LU1TAG*	156.2500	CLCC-6, Pb-Free	1000 / Tape & Reel
NBVSPA018LU1TAG*	155.5200	CLCC-6, Pb-Free	1000 / Tape & Reel
NBVSPA024LU1TAG*	160.0000	CLCC-6, Pb-Free	1000 / Tape & Reel
NBVSPA015LU1TAG*	200.0000	CLCC-6, Pb-Free	1000 / Tape & Reel
NBVSPA027LU1TAG*	148.5000	CLCC-6, Pb-Free	1000 / Tape & Reel
NBVSPA019LU1TAG*	125.0000	CLCC-6, Pb-Free	1000 / Tape & Reel
NBVSPA042LU1TAG*	74.2500	CLCC-6, Pb-Free	1000 / Tape & Reel

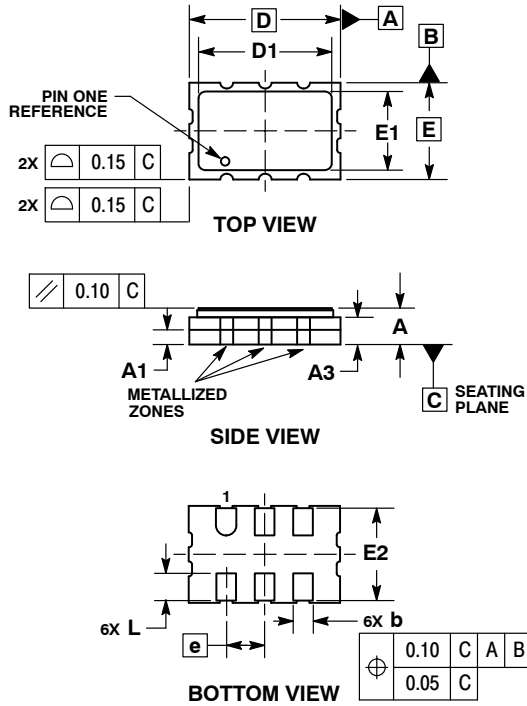
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our tape and Reel Packaging Specification Brochure, BRD8011/D

*Consult factory for availability.

NBVSPA015 Series

PACKAGE DIMENSIONS

6 PIN CLCC, 5x3.2, 1.27P
CASE 848AC-01
ISSUE O

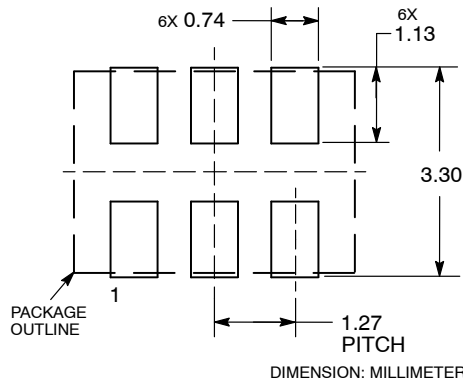


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

DIM	MILLIMETERS	
	MIN	MAX
A	1.05	1.35
A1	0.35	0.65
A3	0.90 REF	
b	0.50	0.80
D	5.00 BSC	
D1	4.25	4.55
E	3.20 BSC	
E1	2.45	2.75
E2	2.90	3.20
e	1.27 BSC	
L	0.75	1.05

SOLDERING FOOTPRINT*

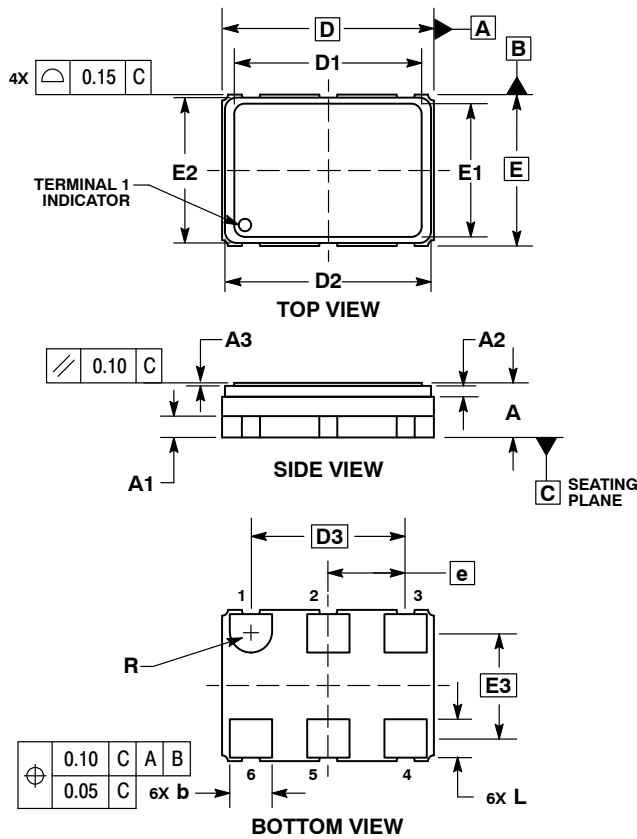


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NBVSPA015 Series

PACKAGE DIMENSIONS

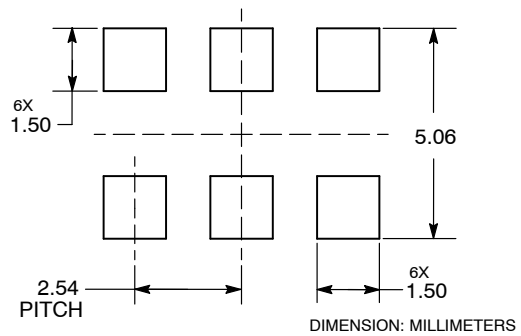
6 PIN CLCC, 7x5, 2.54P
CASE 848AB-01
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.70	1.80	1.90
A1	0.70 REF		
A2	0.36 REF		
A3	0.08	0.10	0.12
b	1.30	1.40	1.50
D	7.00 BSC		
D1	6.17	6.20	6.23
D2	6.66	6.81	6.96
D3	5.08 BSC		
E	5.00 BSC		
E1	4.37	4.40	4.43
E2	4.65	4.80	4.95
E3	3.49 BSC		
e	2.54 BSC		
L	1.17	1.27	1.37
R	0.70 REF		

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative