

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .



AFE1103

HDSL/MDSL ANALOG FRONT END

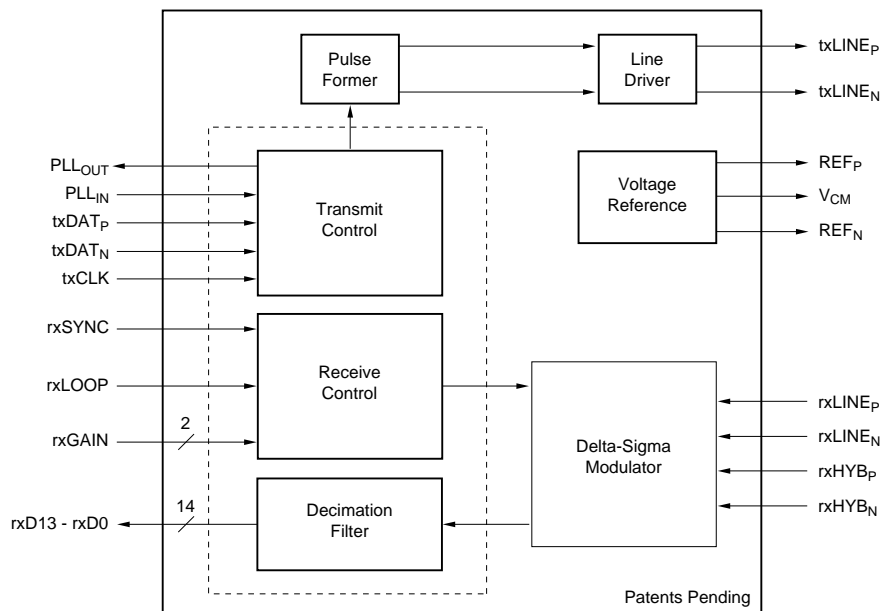
FEATURES

- COMPLETE ANALOG INTERFACE
- T1, E1, AND MDLS OPERATION
- CLOCK SCALEABLE SPEED
- SINGLE CHIP SOLUTION
- +5V ONLY (5V OR 3.3V DIGITAL)
- 250mW POWER DISSIPATION
- 48-PIN SSOP
- -40°C TO +85°C OPERATION
- SECOND SOURCED BY BROOKTREE Bt8921

DESCRIPTION

Burr-Brown's Analog Front End greatly reduces the size and cost of an HDSL or MDLS system by providing all of the active analog circuitry needed to connect the Brooktree Bt8952 HDSL digital signal processor to an external compromise hybrid and a 1:2 HDSL line transformer. All internal filter responses as well as the pulse former output scale with clock frequency—allowing the AFE1103 to operate over a range of bit rates from 196kbps to 1.168Mbps.

Functionally, this unit is separated into a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section filters and digitizes the symbol data received on the telephone line and passes it to the Bt8952. The HDSL Analog Interface is a monolithic device fabricated on 0.6 μ C MOS. It operates on a single +5V supply. It is housed in a 48-pin SSOP package. This unit is second sourced by Brooktree's Bt8921.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

Typical at 25°C, AV_{DD} = +5V, DV_{DD} = +3.3V, f_{ix} = 584kHz (E1 rate), unless otherwise specified.

PARAMETER	COMMENTS	AFE1103E			UNITS
		MIN	TYP	MAX	
RECEIVE CHANNEL					
Number of Inputs	Differential	2			
Input Voltage Range	Balanced Differential ⁽¹⁾		±3.0		V
Common-Mode Voltage	1.5V CMV Recommended		+1.5		V
Input Impedance	All Inputs	See Typical Performance Curves			
Input Capacitance			10		pF
Input Gain Matching	Line Input vs Hybrid Input		±2		%
Resolution		14			Bits
Programmable Gain	Four Gains: 0dB, 3.25dB, 6dB, and 9dB	0		9	dB
Settling Time for Gain Change			6		Symbol Periods
Gain + Offset Error	Tested at Each Gain Range		5		%FSR ⁽²⁾
Output Data Coding		Offset Binary			
Output Data Rate, rxSYNC ⁽³⁾		98		584	kHz
TRANSMIT CHANNEL					
Transmit Symbol Rate, f _{ix}		98		584	kHz
T1 Transmit -3dB Point	Bellcore TA-NWT-3017 Compliant		196		kHz
T1 Rate Power Spectral Density ⁽⁴⁾		See Typical Performance Curves			
E1 Transmit -3dB Point	ETSI RTR/TM-03036 Compliant		292		kHz
E1 Rate Power Spectral Density ⁽⁴⁾		See Typical Performance Curves			
Transmit Power ^(4, 5)		13		14	dBm
Pulse Output		See Typical Performance Curves			
Common-Mode Voltage, V _{CM}			AV _{DD} /2		V
Output Resistance ⁽⁶⁾	DC to 1MHz		1		Ω
TRANSCEIVER PERFORMANCE					
Uncancelled Echo ⁽⁷⁾	rxGAIN = 0dB, Loopback Enabled			-67	dB
	rxGAIN = 0dB, Loopback Disabled			-67	dB
	rxGAIN = 3.25dB, Loopback Disabled			-69	dB
	rxGAIN = 6dB, Loopback Disabled			-71	dB
	rxGAIN = 9dB, Loopback Disabled			-73	dB
DIGITAL INTERFACE⁽⁶⁾					
Logic Levels					
V _{IH}	I _{IH} < 10μA	DV _{DD} -1		DV _{DD} +0.3	V
V _{IL}	I _{IL} < 10μA	-0.3		+0.8	V
V _{OH}	I _{OH} = -20μA	DV _{DD} -0.5			V
V _{OL}	I _{OL} = 20μA			+0.4	V
Transmit/Receive Channel Interface					
t _{tx1}	txCLK Period	1.7		10.2	μs
t _{tx2}	txCLK Pulse Width	t _{tx1} /16		15t _{tx1} /16	ns
POWER					
Analog Power Supply Voltage	Specification		5		V
Analog Power Supply Voltage	Operating Range	4.75		5.25	V
Digital Power Supply Voltage	Specification		3.3		V
Digital Power Supply Voltage	Operating Range	3.15		5.25	V
Power Dissipation ^(4, 5, 8)	DV _{DD} = 3.3V		250		mW
Power Dissipation ^(4, 5, 8)	DV _{DD} = 5V		300		mW
PSRR		60			dB
TEMPERATURE RANGE					
Operating ⁽⁶⁾		-40		+85	°C

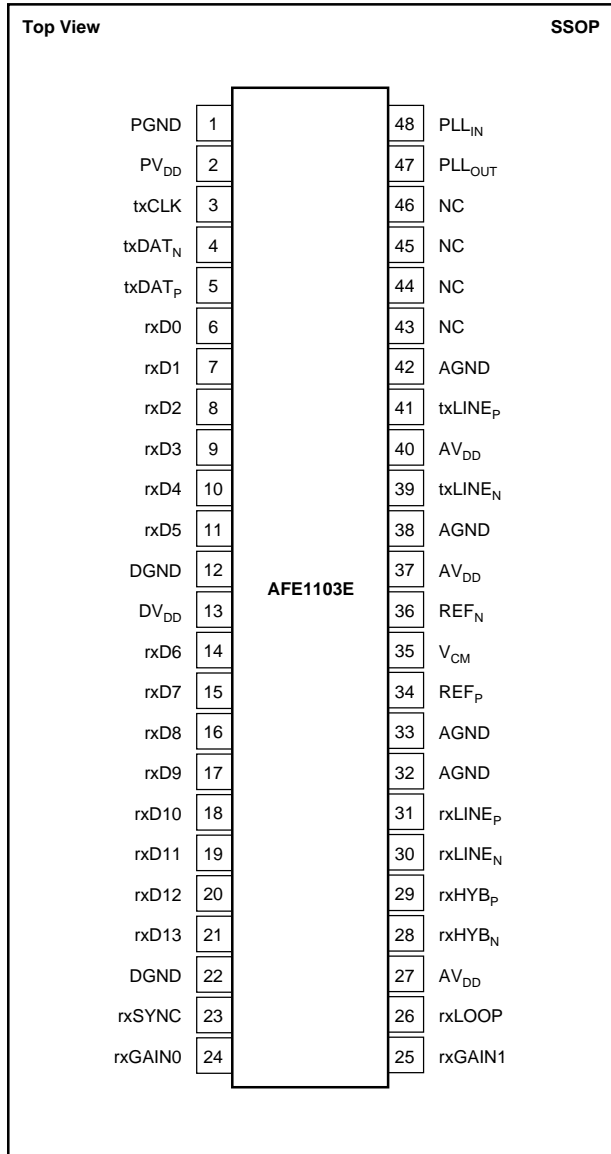
NOTES: (1) With a balanced differential signal, the positive input is 180° out of phase with the negative input, therefore the actual voltage swing about the common mode voltage on each pin is ±1.5V to achieve a differential input range of ±3.0V or 6Vp-p. (2) FSR is Full-Scale Range. (3) The output data is available at twice the symbol rate with interpolated values. (4) With a pseudo-random equiprobable sequence of HDLSL pulses; 13.5dBm applied to the transformer (27dBm output from txLINE_P and txLINE_N). (5) See the Discussion of Specifications section of this data sheet for more information. (6) Guaranteed by design and characterization. (7) Uncancelled Echo is a measure of the total analog errors in the transmitter and receiver sections including the effect of non-linearity and noise. See the Discussion of Specifications section of this data sheet for more information. (8) Power dissipation includes only the power dissipated within the component and does not include power dissipated in the external loads. See the Discussion of Specifications section for more information.

PIN DESCRIPTIONS

PIN #	TYPE	NAME	DESCRIPTION
1	Ground	PGND	Analog Ground for PLL
2	Power	PV _{DD}	Analog Supply (+5V) for PLL
3	Input	txCLK	Symbol Clock (QCLK from Bt8952) (392kHz for T1, 584kHz for E1)
4	Input	txDAT _N	XMITB Line from Bt8952
5	Input	txDAT _P	XMIT Line from Bt8952
6	Output	rxD0	ADC Output Bit-0 (RCV 2 from Bt8952)
7	Output	rxD1	ADC Output Bit-1 (RCV 3 from Bt8952)
8	Output	rxD2	ADC Output Bit-2 (RCV 4 from Bt8952)
9	Output	rxD3	ADC Output Bit-3 (RCV 5 from Bt8952)
10	Output	rxD4	ADC Output Bit-4 (RCV 6 from Bt8952)
11	Output	rxD5	ADC Output Bit-5 (RCV 7 from Bt8952)
12	Ground	DGND	Digital Ground
13	Power	DV _{DD}	Digital Supply (+3.3V to +5V)
14	Output	rxD6	ADC Output Bit-6 (RCV 8 from Bt8952)
15	Output	rxD7	ADC Output Bit-7 (RCV 9 from Bt8952)
16	Output	rxD8	ADC Output Bit-8 (RCV 10 from Bt8952)
17	Output	rxD9	ADC Output Bit-9 (RCV 11 from Bt8952)
18	Output	rxD10	ADC Output Bit-10 (RCV 12 from Bt8952)
19	Output	rxD11	ADC Output Bit-11 (RCV 13 from Bt8952)
20	Output	rxD12	ADC Output Bit-12 (RCV 14 from Bt8952)
21	Output	rxD13	ADC Output Bit-13 (RCV 15 from Bt8952)
22	Ground	DGND	Digital Ground
23	Input	rxSYNC	ADC Sync Signal (RCVCLK from Bt8952) (392kHz for T1, 584kHz for E1)
24	Input	rxGAIN0	Receive Gain Control Bit-0
25	Input	rxGAIN1	Receive Gain Control Bit-1
26	Input	rxLOOP	Loopback Control Signal (loopback is enabled by positive signal)
27	Power	AV _{DD}	Analog Supply (+5V)
28	Input	rxHYB _N	Negative Input from Hybrid Network
29	Input	rxHYB _P	Positive Input from Hybrid Network
30	Input	rxLINE _N	Negative Line Input
31	Input	rxLINE _P	Positive Line Input
32	Ground	AGND	Analog Ground
33	Ground	AGND	Analog Ground
34	Output	REF _P	Positive Reference Output, Nominally 3.5V
35	Output	V _{CM}	Common-Mode Voltage (buffered), Nominally 2.5V
36	Output	REF _N	Negative Reference Output, Nominally 1.5V
37	Power	AV _{DD}	Analog Supply (+5V)
38	Ground	AGND	Analog Ground
39	Output	txLINE _N	Transmit Line Output Negative
40	Power	AV _{DD}	Analog Supply (+5V)
41	Output	txLINE _P	Transmit Line Output Positive
42	Ground	AGND	Analog Ground
43	NC	NC	Connection to Ground Recommended
44	NC	NC	Connection to Ground Recommended
45	NC	NC	Connection to Ground Recommended
46	NC	NC	Connection to Ground Recommended
47	Output	PLL _{OUT}	PLL Filter Output
48	Input	PLL _{IN}	PLL Filter Input

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Analog Inputs: Current	±100mA, Momentary
	±10mA, Continuous
Voltage	AGND -0.3V to AV _{DD} +0.3V
Analog Outputs Short Circuit to Ground (+25°C)	Continuous
AV _{DD} to AGND	-0.3V to 6V
PV _{DD} to PGND	-0.3V to 6V
DV _{DD} to DGND	-0.3V to 6V
PLL _{IN} or PLL _{OUT} to PGND	-0.3V to PV _{DD} +0.3V
Digital Input Voltage to DGND	-0.3V to DV _{DD} +0.3V
Digital Output Voltage to DGND	-0.3V to DV _{DD} +0.3V
AGND, DGND, PGND Differential Voltage	0.3V
Junction Temperature (T _J)	+150°C
Storage Temperature Range	-40°C to +125°C
Lead Temperature (soldering, 3s)	+260°C
Power Dissipation	700mW

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
AFE1103E	48-Pin Plastic SSOP	333	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



ELECTROSTATIC DISCHARGE SENSITIVITY

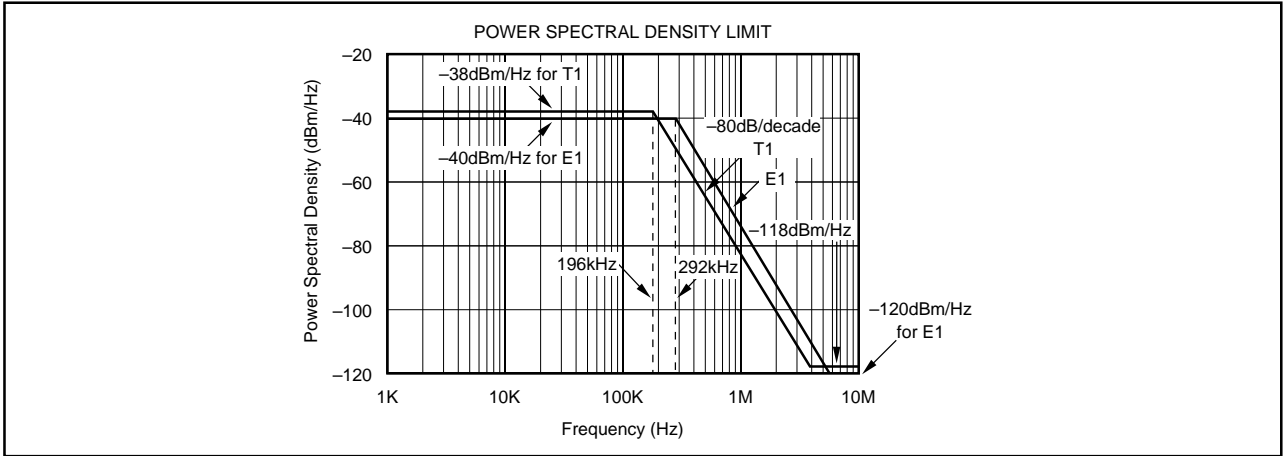
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

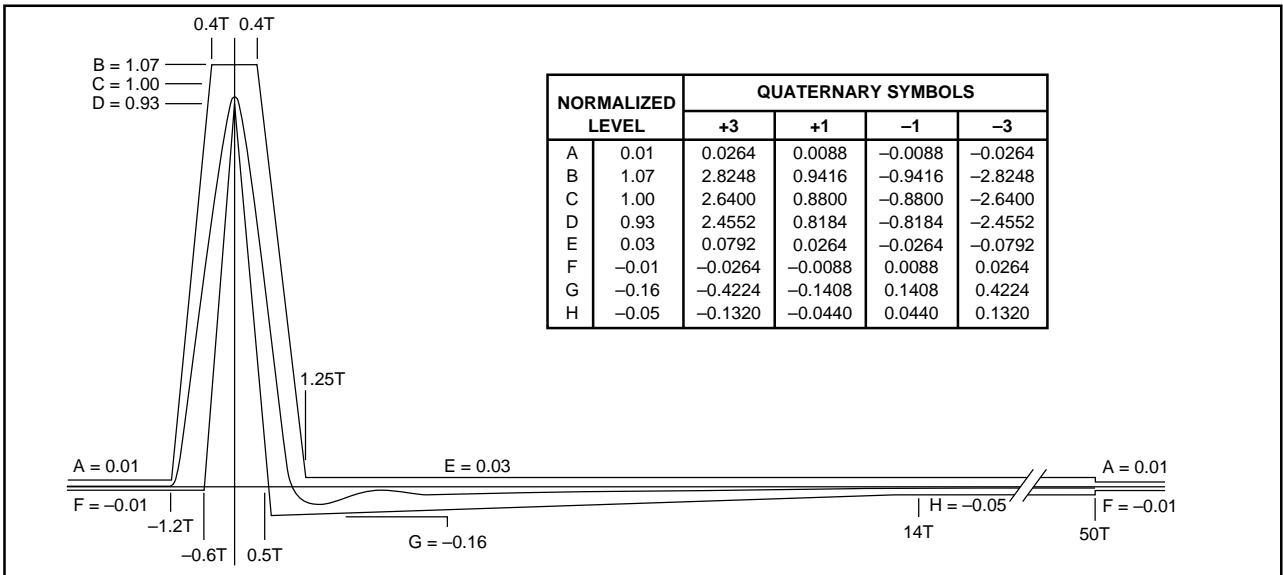
TYPICAL PERFORMANCE CURVES

At Output of Pulse Transformer

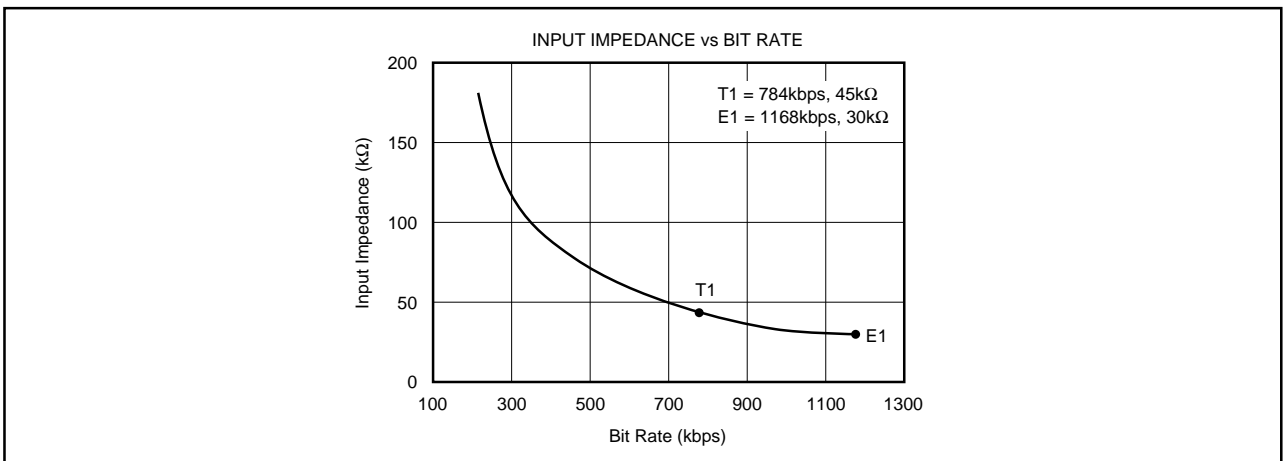
Typical at 25°C, AV_{DD} = +5V, DV_{DD} = +3.3V, unless otherwise specified.



CURVE 1. Upper Bound of Power Spectral Density Measured at the Transformer Output.



CURVE 2. Transmitted Pulse Template and Actual Performance as Measured at the Transformer Output.



CURVE 3. Input Impedance of rxLINE and rxHYB.

THEORY OF OPERATION

The transmit channel consists of a switched-capacitor pulse forming network followed by a differential line driver. The pulse forming network receives symbol data from the XMIT and XMITB outputs of the Bt8952 and generates a 2B1Q output waveform. The output meets the pulse mask and power spectral density requirements defined in European Telecommunications Standards Institute document RTR/TM-03036 for E1 mode and in sections 6.2.1 and 6.2.2.1 of Bellcore technical advisory TA-NWT-001210 for T1 mode. The differential line driver uses a composite output stage combining class B operation (for high efficiency driving large signals) with class AB operation (to minimize cross-over distortion).

The receive channel is designed around a fourth-order delta sigma A/D converter. It includes a difference amplifier designed to be used with an external compromise hybrid for first order analog crosstalk reduction. A programmable gain amplifier with gains of 0dB to +9dB is also included. The delta sigma modulator operating at a 24X oversampling ratio produces 14 bits of resolution at output rates up to 584kHz. The basic functionality of the AFE1103 is illustrated in Figure 1 shown below.

The receive channel operates by summing the two differential inputs, one from the line (rxLINE) and the other from the compromise hybrid (rxHYB). The connection of these two inputs so that the hybrid signal is subtracted from the line signal is described in the paragraph titled "Echo Cancellation in the AFE". The equivalent gain for each input in the difference amp is 1. The resulting signal then passes to a programmable gain amplifier which can be set for gains of 0dB through 9dB. The ADC converts the signal to a 14-bit digital word, rxD13-rxD0.

rxLOOP INPUT

rxLOOP is the loopback control signal. When enabled, the rxLINE_P and rxLINE_N inputs are disconnected from the AFE. The rxHYB_P and rxHYB_N inputs remain connected. Loopback is enabled by applying a positive signal (Logic 1) to rxLOOP.

ECHO CANCELLATION IN THE AFE

The rxHYB input is designed to be subtracted from the rxLINE input for first order echo cancellation. To accomplish this, note that the rxLINE input is connected to the same polarity signal at the transformer (positive to positive and negative to negative) while the rxHYB input is connected to opposite polarity through the compromise hybrid (negative to positive and positive to negative) as shown in Figure 2.

RECEIVE DATA CODING

The data from the receive channel A/D converter is coded in offset binary.

ANALOG INPUT	OUTPUT CODE (rxD13 - rxD0)
Positive Full Scale	11111111111111
Negative Full Scale	00000000000000

RECEIVE CHANNEL PROGRAMMABLE GAIN AMPLIFIER

The gain of the amplifier at the input of the Receive Channel is set by two gain control pins, rxGAIN1 and rxGAIN0. The resulting gain between 0dB and +9dB is shown below.

rxGAIN1	rxGAIN0	GAIN
0	0	0dB
0	1	3.25dB
1	0	6dB
1	1	9dB

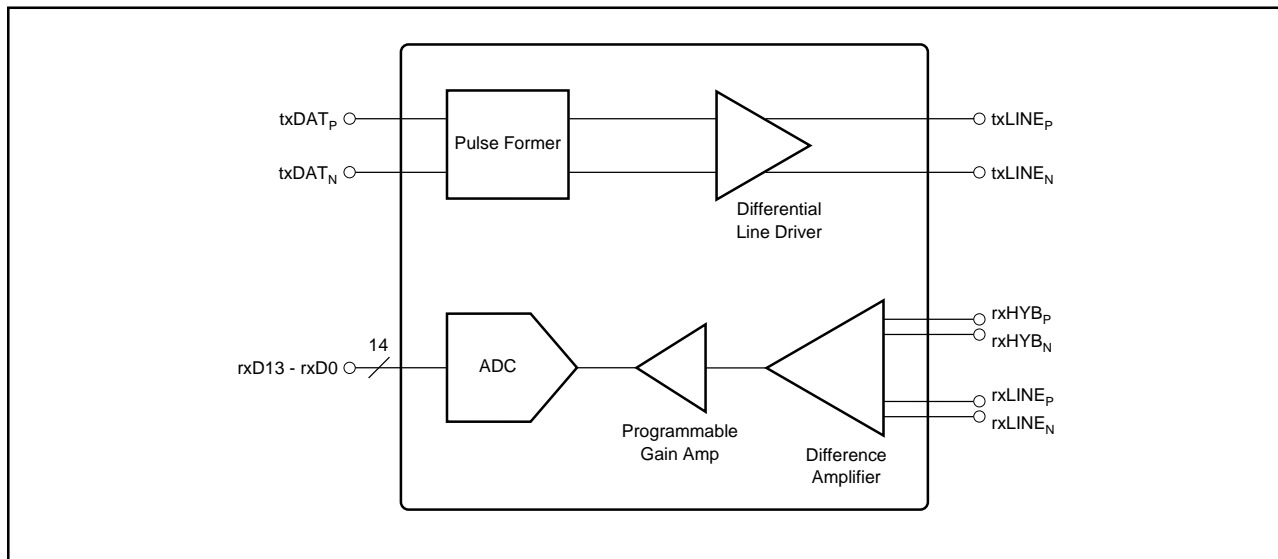


FIGURE 1. Functional Block Diagram of AFE1103.

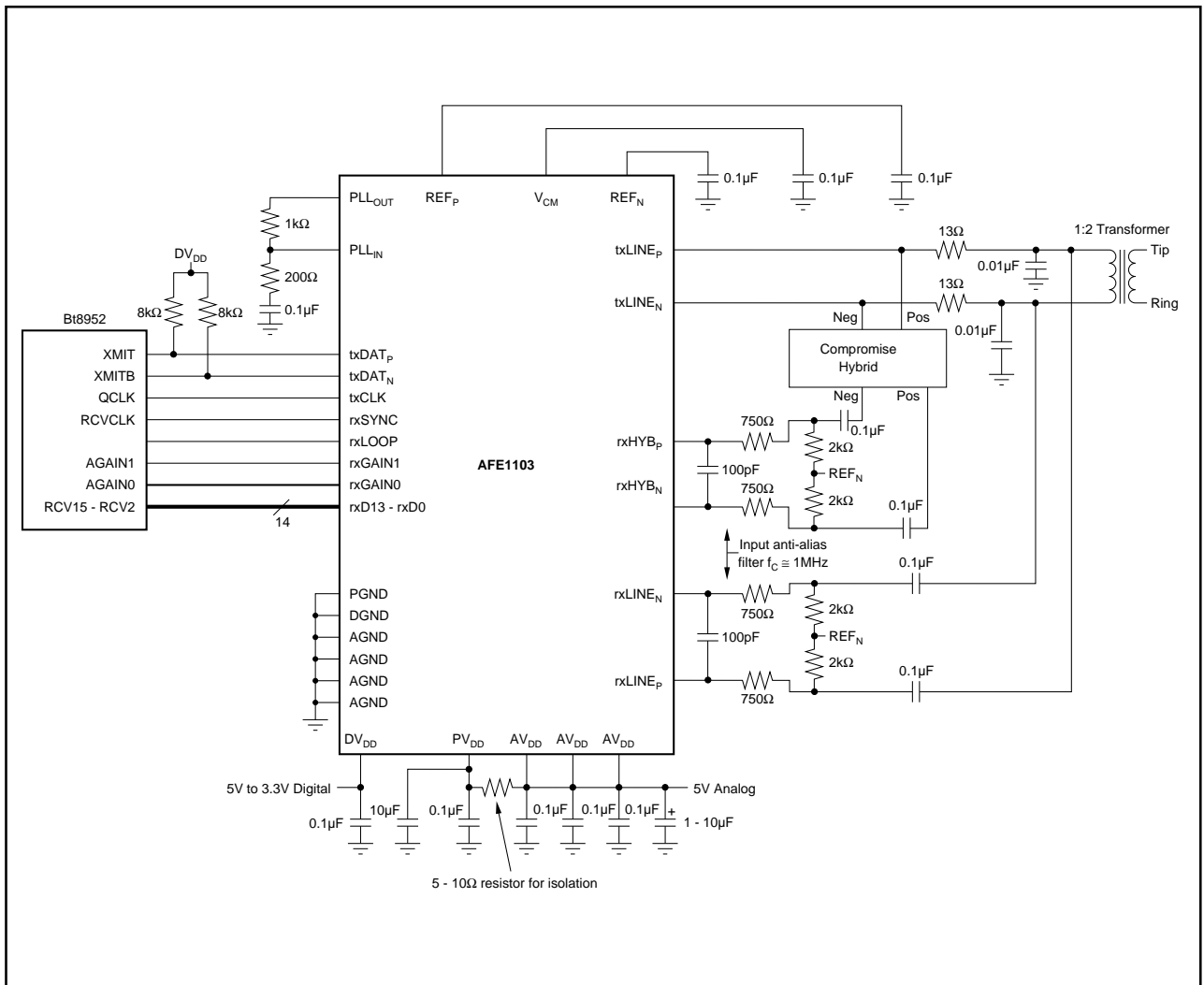


FIGURE 2. Basic Connection Diagram.

rxHYB AND rxLINE INPUT ANTI-ALIASING FILTERS

The -3dB frequency of the input anti-aliasing filter for the rxLINE and rxHYB differential inputs should be about 1MHz. Suggested values for the filter are 750Ω for each of the two input resistors and 100pF for the capacitor. Together the two 750Ω resistors and the 100pF capacitor result in -3dB frequency of just over 1MHz. The 750Ω input resistors will result in a minimal voltage divider loss with the input impedance of the AFE1103.

This circuit applies at both T1 and E1 rates. For slower rates, the antialiasing filters will give best performance with their -3dB frequency approximately equal to the bit rate. For example, a -3dB frequency of 500kHz should be used for a single pair bit rate of 500kbps.

rxHYB AND rxLINE INPUT BIAS VOLTAGE

The transmitter output on the txLINE pins is centered at midscale, 2.5V. But, the rxLINE input signal is centered at 1.5V in the circuit shown in Figure 2 above.

Inside the AFE1103, the rxHYB and rxLINE signals are subtracted as described in the paragraph on echo cancellation above. This means that the rxHYB inputs need to be centered at 1.5V just as the rxLINE signal is centered at 1.5V. REF_N (Pin 36) is a 1.5V voltage source. The external compromise hybrid must be designed so that the signal into the rxHYB inputs is centered at 1.5V.

TIMING DIAGRAM

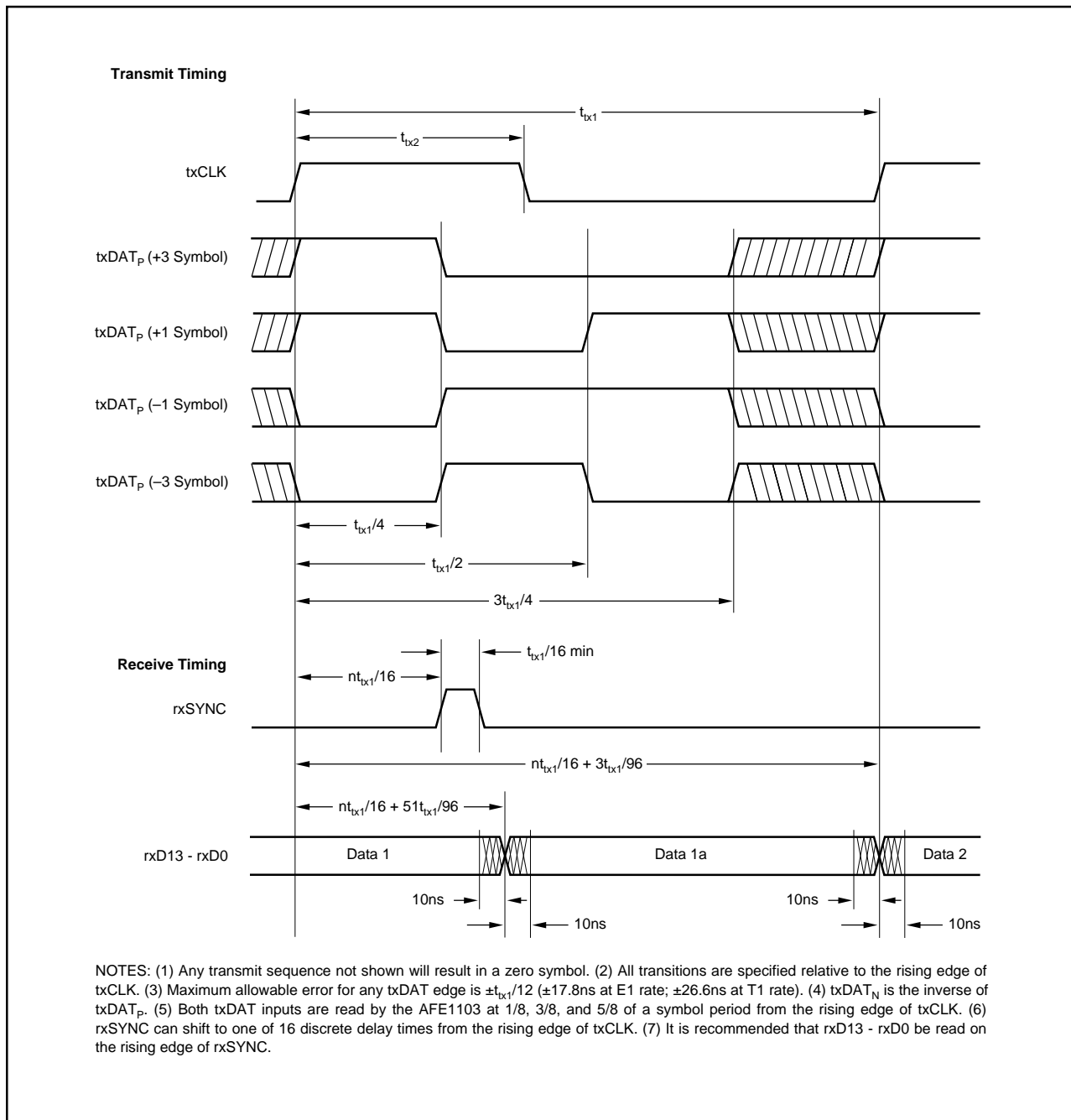


FIGURE 3. Timing Diagram.

RECEIVE TIMING

The rxSYNC signal controls portions of the A/D converter's decimation filter and the data output timing of the A/D converter. It is generated at the symbol rate by the user and must be synchronized with txCLK. The leading edge of rxSYNC can occur at the leading edge of txCLK or it can be shifted by the user in increments of 1/16 of a symbol period to one of 15 discrete delay times after the leading edge of txCLK.

The bandwidth of the A/D converter decimation filter is equal to one half of the symbol rate. The A/D converter data output rate is 2X the symbol rate. The specifications of the AFE1103 assume that one A/D converter output is used per symbol period and the other interpolated output is ignored. The Receive Timing Diagram above suggests using the rxSYNC pulse to read the first data output in a symbol period. Either data output may be used. Both data outputs may be used for more flexible post-processing.

DISCUSSION OF SPECIFICATIONS

UNCANCELLED ECHO

The key measure of transceiver performance is uncancelled echo. This measurement is made as shown in the diagram of Figure 4. The AFE is connected to an output circuit including a typical 1:2 line transformer. The line is simulated by a 135Ω resistor. Symbol sequences are generated by the tester and applied both to the AFE and to the input of an adaptive filter. The output of the adaptive filter is subtracted from the AFE output to form the uncancelled echo signal. Once the filter taps have converged, the RMS value of the uncancelled echo is calculated. Since there is no far-end signal source or additive line noise, the uncancelled echo contains only noise and linearity errors generated in the transmitter and receiver.

The data sheet value for uncancelled echo is the ratio of the RMS uncancelled echo (referred to the receiver input through the receiver gain) to the nominal transmitted signal (13.5dBm into 135Ω, or 1.74Vrms). This echo value is measured under a variety of conditions: with loopback enabled (line input disconnected); with loopback disabled under all receiver gain ranges; and with the line shorted (S₁ closed in Figure 4).

POWER DISSIPATION

Approximately 75% of the power dissipation in the AFE1103 is in the analog circuitry, and this component does not change with clock frequency. However, the power dissipa-

tion in the digital circuitry does decrease with lower clock frequency. In addition, the power dissipation in the digital section is decreased when operating from a smaller supply voltage, such as 3.3V. (The analog supply, AV_{DD}, must remain in the range 4.75V to 5.25V.)

The power dissipation listed in the specifications section applies under these normal operating conditions: 5V Analog Power Supply; 3.3V Digital Power Supply; standard 13.5dBm delivered to the line; and a pseudo-random equiprobable sequence of HDSL output pulses. The power dissipation specifications includes all power dissipated in the AFE1103, it does not include power dissipated in the external load. The external power is 16.5dBm, 13.5dBm to the line and 13.5dBm to the impedance matching resistors. The external load power of 16.5dBm is 45mW. The typical power dissipation in the AFE1103 under various conditions is shown in Table I.

BIT RATE PER AFE1103 (Symbols/sec)	DVDD (V)	TYPICAL POWER DISSIPATION IN THE AFE1103 (mW)
584 (E1)	3.3	250
584 (E1)	5	300
392 (T1)	3.3	240
392 (T1)	5	270
146 (E1/4)	3.3	230
146 (E1/4)	5	245

TABLE I. Typical Power Dissipation.

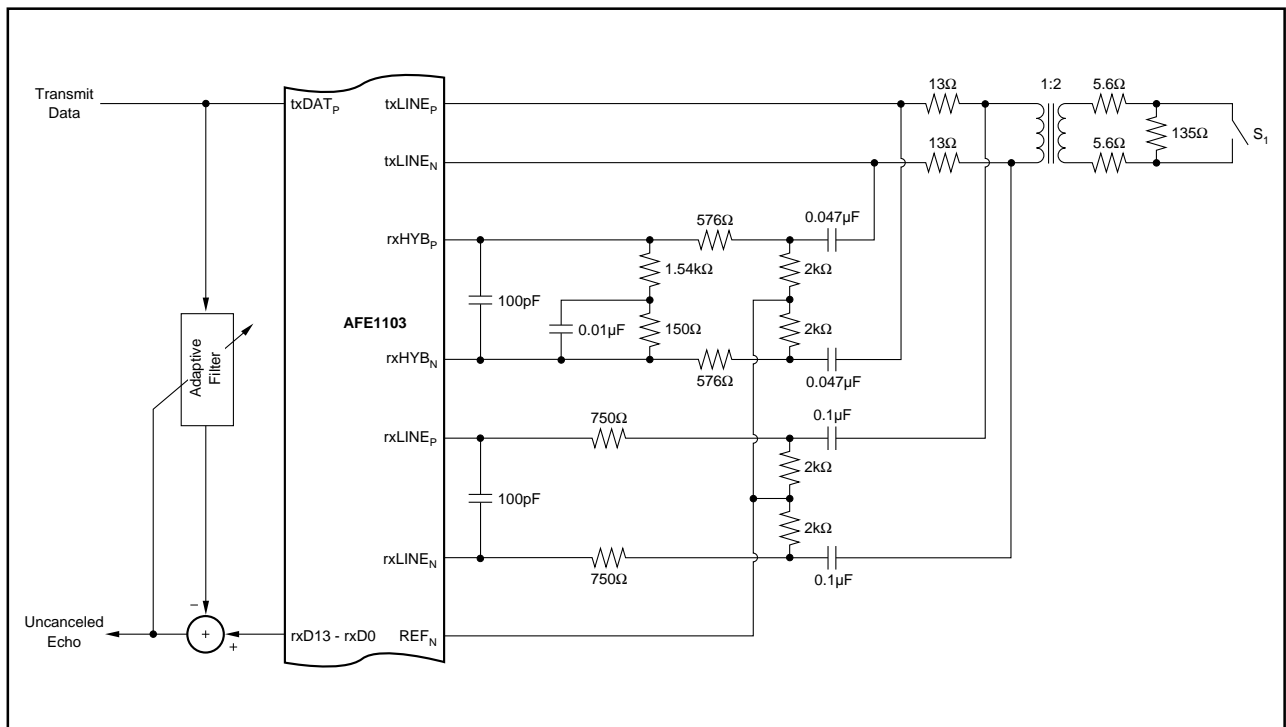


FIGURE 4. Uncanceled Echo Test Diagram.

LAYOUT

The analog front end of an HDSL system has a number of conflicting requirements. It must accept and deliver digital outputs at fairly high rates of speed, phase-lock to a high-speed digital clock, and convert the line input to a high-precision (14-bit) digital output. Thus, there are really three sections of the AFE1103: the digital section, the phase-locked loop, and the analog section.

The power supply for the digital section of the AFE1103 can range from 3.3V to 5V. This supply should be decoupled to digital ground with a ceramic 0.1 μ F capacitor placed as close to DGND (pin 12) and DV_{DD} (pin 13) as possible. Ideally, both a digital power supply plane and a digital ground plane should run up to and underneath the digital pins of the AFE1103 (pins 3 through 26). However, DV_{DD} may be supplied by a wide printed circuit board (PCB) trace. A digital ground plane underneath all digital pins is strongly recommended.

The phase-locked loop is powered from PV_{DD} (pin 2) and its ground is referenced to PGND (pin 1). Note that PV_{DD} must be in the 4.75V to 5.25V range. This portion of the AFE1103 should be decoupled with both a 10 μ F Tantalum capacitor and a 0.1 μ F ceramic capacitor. The ceramic capacitor should be placed as close to the AFE1103 as possible. The placement of the Tantalum capacitor is not as critical, but should be close. In each case, the capacitor should be connected between PV_{DD} and PGND.

In most systems, it will be natural to derive PV_{DD} from the AV_{DD} supply. A 5 Ω to 10 Ω resistor should be used to connect PV_{DD} to the analog supply. This resistor in combination with the 10 μ F capacitor form a lowpass filter—keeping glitches on AV_{DD} from affecting PV_{DD}. Ideally, PV_{DD} would originate from the analog supply (via the resistor) near the power connector for the printed circuit board. Likewise, PGND should connect to a large PCB trace or small ground plane which returns to the power supply connector underneath the PV_{DD} supply path. The PGND “ground plane” should also extend underneath PLL_{IN} and PLL_{OUT} (pins 47 and 48).

The remaining portion of the AFE1103 should be considered analog. All AGND pins should be connected directly to a common analog ground plane and all AV_{DD} pins should be connected to an analog 5V power plane. Both of these planes should have a low impedance path to the power supply.

Ideally, all ground planes and traces and all power planes and traces should return to the power supply connector before being connected together (if necessary). Each ground and power pair should be routed over each other, should not overlap any portion of another pair, and the pairs should be separated by a distance of at least 0.25 inch (6mm). One exception is that the digital and analog ground planes should be connected together underneath the AFE1103 by a small trace.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
AFE1103E	NRND	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Samples Not Available
AFE1103E/1K	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
AFE1103E/1KG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
AFE1103EG4	NRND	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Samples Not Available

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE1103E/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE1103E/1K	SSOP	DL	48	1000	346.0	346.0	49.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2010, Texas Instruments Incorporated