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CCD Analog Front-End with Timing Generator and Vertical Driver for Digital Cameras

Check for Samples: VSP01M01, VSP01M02

FEATURES

- **CCD Signal Processing:**
  - **36-MHz Correlated Double Sampling (CDS)**
- **16-Bit Analog-to Digital Conversion:**
  - **36-MHz Conversion Rate**
  - **No Missing Codes Ensured**
- **80-dB Input-Referred SNR (at 12-dB Gain)**
- **Programmable Black Level Clamping**
- **Programmable Gain Amplifier (PGA):**
  - **–9 dB to +44 dB**
    –3 dB to +18 dB by Analog Front Gain
    –6 dB to +26 dB by Digital Gain
- **Timing Generator:**
  - **Fully Programmable V_{RATE} Timing by Serial I/O**
  - **Default Timing Supports Standard Operation**
  - **Flexible V_{RATE} Pin Assignment**
  - **HD/VD Master or Slave Mode**
  - **External Trigger, Strobe Function Support**
  - **Flexible Draft or Pixel Summing Operation**
- **RG and HG Driver:**
  - **Programmable Drivability Control**
  - **Two Horizontal Transfer Independent Drivers**
  - **One Reset Gate Driver**
- **CCD Horizontal High-Speed Clock Phase Control:**
  - **Fine Step: 0.28 ns**
  - **Wide Step: 1/3 Pixel Rate**
- **Vertical CCD Driver:**
  - **8-Channel V_{DRIVER} with Sub-Driver**
  - **Supports Three-Field CCD Driving**
  - **Three Level Drivers ($V_{TRANSFER}$) × 5**
  - **Two Level Drivers ($V_{TRANSFER}$) × 3**
  - **Two Level Drivers ($E_{SHUTTER}$) × 1**
  - **450 pF to 1890 pF with 60 Ω to 240 Ω**
- **Flexible Voltage Operation:**
  - **AFET + TG: 2.7 V to 3.6 V**
  - **VL: –5.0 V to –9.0 V**
  - **VM: GND**
  - **VH: 11.5 V to 15.5 V**
  - **Low Power: 139 mW at 3.0 V, 36 MHz**
  - **Stand-By + Power-Save Mode: 36 mW**
  - **Stand-By Mode (MCK Off): 10 mW**
- **BGA-100 Package**

DESCRIPTION

The VSP01M01 and VSP01M02 are complete mixed-signal ICs for charge-coupled device (CCD) signal processing with a built-in CCD timing generator, analog-to-digital converter (ADC), and CCD vertical driver. The AFE CCD channel has correlated double sampling to extract image information from the CCD output signal. Signal paths have gains ranging from –9 dB to +44 dB. The black level clamping circuit enables accurate black reference level and quick black level recovery after gain changes. An input signal clamp with CDS offset adjustment function is available. The system synchronizes the master clock, horizontal driver (HD), and vertical driver (VD). The VSP01M01 and VSP01M02 support all signal terminals required by CCD architecture. The RG driver, HG driver, and vertical driver synchronize the ADC clock phase in order to realize ideal performance.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VSP01M01ZWD(2)	BGA-100	ZWD	–25°C to +85°C	VSP01M01	VSP01M01ZWD	Tray, 360
					VSP01M01ZWDR	Tape and Reel
VSP01M01GWD	BGA-100	GWD	–25°C to +85°C	VSP01M01	VSP01M01GWD	Tray, 360
					VSP01M01GWDR	Tape and Reel
VSP01M02ZWD(2)	BGA-100	ZWD	–25°C to +85°C	VSP01M02	VSP01M02ZWD	Tray, 360
					VSP01M02ZWDR	Tape and Reel

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The package is Pb-free.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		VSP01M01, VSP01M02	UNIT
Supply voltage	AVDD	–0.3 to +4.0	V
	DRVDD	–0.3 to +4.0	V
	VDD5	–0.3 to +6.0	V
	VL	GND to –10	V
	VH	VL + 26	V
Supply voltage differences	AVDD, DRVDD	±0.1	V
Ground voltage differences	VSS	±0.1	V
Digital input voltage		–0.3 to (DVDD + 0.3)	V
Analog input voltage		–0.3 to (AVDD + 0.3)	V
Input current (any pins except supplies)		±10	mA
Ambient temperature under bias		–25 to +85	°C
Storage temperature		–55 to +125	°C
Junction temperature		+150	°C
Package temperature (IR reflow, peak)		+250	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
Analog supply voltage	AVDD	2.7	3.0	3.6	V
Digital supply voltage	DVDD	2.7	3.0	3.6	V
	VDD5	3.0		5.5	V
Driver supply voltage	VL	–9.0		–5.0	V
	VH	11.5		15.5	V
Digital input logic family			CMOS		
Digital input clock frequency	MCK	12		36	MHz
	SCLK			20	MHz
Digital output load capacitance				10	pF
Operating free-air temperature	T_A	–25		+85	°C

ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, all power supply voltages = +3.0 V, and conversion rate = 36 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP01M01ZWD, VSP01M01GWD, VSP01M02ZWD			UNIT
			MIN	TYP	MAX	
RESOLUTION						
Resolution		VSP01M01 only		10		Bits
		VSP01M02 only		12		Bits
CONVERSION/CLOCK RATE						
Conversion/clock rate					36	MHz
ANALOG INPUT (CCDIN)						
Input signal level for full-scale out		CDS gain = 0 dB, DPGA gain = 0 dB			1000	mV
Maximum input range		CDS gain = –3 dB, DPGA gain = 0 dB			1300	mV
Input capacitance				15		pF
Input limit			–0.3		3.3	V
TRANSFER CHARACTERISTICS						
Differential nonlinearity	DNL	CDS gain = 0 dB, DPGA gain = 0 dB		±0.25		LSB
Integral nonlinearity	INL	CDS gain = 0 dB, DPGA gain = 0 dB		±0.5		LSB
No missing codes				Ensured		
Step response settling time		Full-scale step input		1		Pixel
Overload recovery time		Step input from 1.8 V to 0 V		2		Pixels
Data latency				9		Clocks
Signal-to-noise ratio (1)		Grounded input capacitor, PGA gain = 0 dB		76		dB
		Grounded input capacitor, analog gain = +12 dB		68		dB
CCD offset correction range			–200		200	mV
INPUT CLAMP						
Clamp on-resistance				400		Ω
Clamp level				1.5		V
PROGRAMMABLE ANALOG FRONT GAIN (CDS)						
Minimum gain		Gain code = 111b		–3		dB
Default gain		Gain code = 000b		0		dB
Medium gain 1		Gain code = 001b		6		dB
Medium gain 2		Gain code = 010b		12		dB
Maximum gain		Gain code = 011b		18		dB
Gain control error				0.5		dB
PROGRAMMABLE DIGITAL GAIN (DPGA)						
Programmable gain range			–6		26	dB
Gain step				0.03125		dB
OPTICAL BLACK CLAMP LOOP						
Control DAC resolution				10		Bits
Loop time constant				40.7		µs
Optical black clamp level (VSP01M01 only)		Programmable range of clamp level	16		78	LSB
		OBCLP level at code = 01000b		32		LSB
		OB level program step		2		LSB
Optical black clamp level (VSP01M02 only)		Programmable range of clamp level	64		312	LSB
		OBCLP level at code = 01000b		128		LSB
		OB level program step		8		LSB

(1) SNR = 20 log (full-scale voltage/rms noise).

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, all power supply voltages = +3.0 V, and conversion rate = 36 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP01M01ZWD, VSP01M01GWD, VSP01M02ZWD MIN	TYP	MAX	UNIT
DIGITAL INPUTS						
Logic family				CMOS		
Input voltage	V_{T+}	Low to high threshold voltage		1.7		V
	V_{T-}	High to low threshold voltage		1.0		V
Input current	I_{IH}	Logic high, V_{IN} = +3 V			±20	µA
	I_{IL}	Logic low, V_{IN} = 0 V			±20	µA
Input capacitance				5		pF
Maximum input voltage			–0.3		DVDD + 0.3	V
DIGITAL OUTPUTS (DATA)						
Logic family				CMOS		
Logic coding				Straight Binary		
Output voltage	V_{OH}	Logic high	2.4			V
	V_{OL}	Logic low			0.4	V
Additional output data delay		Output data delay code = 00b		0		ns
		Output data delay code = 01b		2		ns
		Output data delay code = 10b		4		ns
		Output data delay code = 11b		6		ns
H_{DRIVER} OUTPUTS						
Output voltage	RG, HL	Logic high (V_{OH}) I_{OH} = 0 mA	VDD5 – 0.05			V
		Logic high (V_{OH}) I_{OH} = –6.8 mA	VDD5 – 0.6			V
		Logic low (V_{OL}) I_{OL} = 6.8 mA			0.4	V
Output voltage (HG1A, HG1B, HG2A, HG2B)		Logic high (V_{OH}) I_{OH} = 0 mA	VDD5 – 0.05			V
		Logic high (V_{OH}) I_{OH} = –13.6 mA (max), –6.8 mA (min)	VDD5 – 0.6			V
		Logic low (V_{OL}) I_{OL} = 13.6 mA (max), 6.8 mA (min)			0.4	V
TG OUTPUTS						
Output voltage (V0N-V12N, P0-P5, SUBN, FIELD, STROBE, MSHUT, SUBSW1, SUBSW2, ADCCK, HD, VD)		Logic high (V_{OH}) I_{OH} = –1.7 mA	DVDD – 0.6			V
		Logic low (V_{OL}) I_{OL} = 1.7 mA			0.4	V
TP output voltage (TPP, TPD)		Logic high (V_{OH}) I_{OH} = –1.7 mA	DVDD – 0.6			V
		Logic low (V_{OL}) I_{OL} = 1.7 mA			0.4	V
V_{DRIVER} OUTPUTS						
Output current (V1, V2, V3A, V3B, V4, V5A, V5B, V6) (VL = –9.0 V, VM = 0 V, VH = 15.5 V)	I_{OL}	V1, V2, V3A, V3B, V4, V5A, V5B, V6 = –8.1 V	10			mA
	I_{OM1}	V1, V2, V3A, V3B, V4, V5A, V5B, V6 = –0.2 V			–5.0	mA
	I_{OM2}	V1, V3A, V3B, V5A, V5B = 0.2 V	5			mA
	I_{OH}	V1, V3A, V3B, V5A, V5B = 14.55 V			–7.2	mA
	I_{OSL}	SUB = –8.1 V	5.4			mA
	I_{OSH}	SUB = 14.55 V			–4	mA

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, all power supply voltages = +3.0 V, and conversion rate = 36 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP01M01ZWD, VSP01M01GWD, VSP01M02ZWD			UNIT
			MIN	TYP	MAX	
POWER SUPPLY						
Supply voltage	AV_{DD}		2.7	3.0	3.6	V
	DV_{DD}					
	VDD5	for HG1A, HG1B, HG2A, HG2B, HL, RG	3.0		5.5	V
	VL	for V1, V2, V3A, V3B, V4, V5A, V5B, V6	–9		–5	V
	VH	for V1, V2, V3A, V3B, V4, V5A, V5B, V6	11.5		15.5	V
Power dissipation	AFE	Normal operation mode: no CCD load (at 3.0 V, 38 MHz)		85		mW
Power dissipation	TG + H, R_{DRIVER}			50		mW
Power dissipation	V_{DRIVER}			4		mW
Power dissipation (total) without CCD load				139		mW
Power dissipation (total)		Standby + power-save mode (at 3.0 V, 38 MHz)		36		mW
		Master clock off mode (at 3.0 V)		10		mW
TEMPERATURE RANGE						
Operating temperature			–25		+85	°C
Thermal resistance	θ_{JA}	At 165 mW power dissipation with load		46.18		°C/W

SWITCHING CHARACTERISTICS

All specifications at T_A = +25°C, all power supply voltages = +3.0 V, and conversion rate = 36 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay time	t_{PLM}			15	100	ns
	t_{PMH}			20	100	ns
	t_{PLH}			20	100	ns
	t_{PML}			15	50	ns
	t_{PHM}			30	50	ns
	t_{PHL}			30	50	ns
Rise time	t_{TLM}	VL → VM			300	ns
	t_{TMH}	VM → VH			300	ns
	t_{TLH}	VL → VH			300	ns
Fall time	t_{TML}	VM → VL			300	ns
	t_{THM}	VH → VM			300	ns
	t_{THL}	VH → VL			300	ns
Output noise voltage	V_{CLH}				2.0	V
	V_{CLL}				2.0	V
	V_{CMH}				2.0	V
	V_{CML}				2.0	V
	V_{CHL}				2.0	V

PIN CONFIGURATION

VSP01M01ZWD, VSP01M01GWD
BGA PACKAGE
(BOTTOM VIEW)

	1	2	3	4	5	6	7	8	9	10
A	DAC1	V12N	CH2N	V6N	NC	V1N	V0N	NC	NC	CH0N
B	DAC2	V11N	V10N	V8N	V7N	CH1N	NC	CH3N	B8	NC
C	CCDIN	CCDGND	V9N	V3N	V4N	V2N	CH5N	B9	B6	B7
D	COB	BYP	BYP2	AVDD	DVSS	DVSS	DRVDD	CH4N	B4	B5
E	CM	BYPM	REFN	AVDD	AVSS	AVSS	DRVDD	B3	B1	B2
F	REFP	V5N	NC	AVDD	AVSS	AVSS	DRVDD	V2	B0	SUB
G	BYPD	V3B	TPD	DVSS	VL	VH	VDD5	VSS5	VSS5	NC
H	TPP	SYSRST	R_{LOAD}	V5A	V3A	STROBE	VDD5	V6	RG	H1A
J	SDATA	SCLK	TRIG	VD	SUBSW1	MSHUT	SUBN	HL	V4	ADCCK
K	MCK	$\overline{CS}$	HD	SUBSW2	V1	FIELD	V5B	H2A	H1B	H2B

PIN CONFIGURATION

VSP01M02ZWD
BGA PACKAGE
(BOTTOM VIEW)

	1	2	3	4	5	6	7	8	9	10
A	DAC1	V12N	CH2N	V6N	NC	V1N	V0N	NC	NC	CH0N
B	DAC2	V11N	V10N	V8N	V7N	CH1N	NC	CH3N	B10	B1
C	CCDIN	CCDGND	V9N	V3N	V4N	V2N	CH5N	B11	B8	B9
D	COB	BYP	BYP2	AVDD	DVSS	DVSS	DRVDD	CH4N	B6	B7
E	CM	BYPM	REFN	AVDD	AVSS	AVSS	DRVDD	B5	B3	B4
F	REFP	V5N	NC	AVDD	AVSS	AVSS	DRVDD	V2	B2	SUB
G	BYPD	V3B	TPD	DVSS	VL	VH	VDD5	VSS5	VSS5	B0
H	TPP	SYSRST	R_{LOAD}	V5A	V3A	STROBE	VDD5	V6	RG	H1A
J	SDATA	SCLK	TRIG	VD	SUBSW1	MSHUT	SUBN	HL	V4	ADCCK
K	MCK	$\overline{CS}$	HD	SUBSW2	V1	FIELD	V5B	H2A	H1B	H2B

Table 2. TERMINAL FUNCTIONS

TERMINAL		TYPE[1]	DESCRIPTION
NAME	PIN		
DAC1	A1	DO	DAC1 output
V12N	A2	DO	Vertical rate signal 12N
CH2N	A3	DO	Universal vertical rate signal 2N (for V3A)
V6N	A4	DO	Vertical rate signal 6N (for V6)
NC	A5	—	No connection
V1N	A6	DO	Vertical rate signal 1N (for V1)
V0N	A7	DO	Vertical rate signal 0N
NC	A8	—	No connection
NC	A9	—	No connection
CH0N	A10	DO	Universal vertical rate signal 0N
DAC2	B1	DO	DAC2 output
V11N	B2	DO	Vertical rate signal 11N
V10N	B3	DO	Vertical rate signal 10N
V8N	B4	DO	Vertical rate signal 8N
V7N	B5	DO	Vertical rate signal 7N
CH1N	B6	DO	Universal vertical rate signal 1N (for V1)
NC	B7	—	No connection
CH3N	B8	DO	Universal vertical rate signal 3N (for V5A)
B8	B9	DO	Data out bit 8 (VSP01M01 only)
B10	B9	DO	Data out bit 10 (VSP01M02 only)
NC	B10	—	No connection (VSP01M01 only)
B1	B10	DO	Data out bit 1 (VSP01M02 only)
CCDIN	C1	AI	CCD signal input
CCDGND	C2	AI	CCD signal input ground
V9N	C3	DO	Vertical rate signal 9N
V3N	C4	DO	Vertical rate signal 3N (for V3A, V3B)
V4N	C5	DO	Vertical rate signal 4N (for V4)
V2N	C6	DO	Vertical rate signal 2N (for V2)
CH5N	C7	DO	Universal vertical rate signal 5N (for V5B)
B9	C8	DO	Data out bit 9 (MSB) (VSP01M01 only)
B11	C8	DO	Data out bit 11 (MSB) (VSP01M02 only)
B6	C9	DO	Data out bit 6 (VSP01M01 only)
B8	C9	DO	Data out bit 8 (VSP01M02 only)
B7	C10	DO	Data out bit 7 (VSP01M01 only)
B9	C10	DO	Data out bit 9 (VSP01M02 only)
COB	D1	AO	OB loop feedback capacitor[2]
BYP	D2	AO	Internal reference[3]
BYP2	D3	AO	Internal reference[4]
AVDD	D4	P	Analog power supply
DVSS	D5	P	Ground
DVSS	D6	P	Ground

(1) Designators by type: P: power-supply and ground, DI: digital input, DO: digital output, DI/O: digital input and output, AI: analog input, AO: analog output, and VDO: V_{DRIVER} digital output.
(2) Should be connected to ground with a bypass capacitor. The recommended value is 0.1 µF to 0.22 µF; however, actual value depends on the application environment. Refer to the *OB Loop and OB Clamp Level* section for more detail.
(3) Should be connected to ground with a bypass capacitor (0.1 µF). Refer to the *Voltage Reference* section for more detail.
(4) Should be connected to ground with a bypass capacitor. The recommended value is 400 pF to 1000 pF; however, actual value depends on the application environment. Refer to the *Voltage Reference* section for more detail.

Table 2. TERMINAL FUNCTIONS (continued)

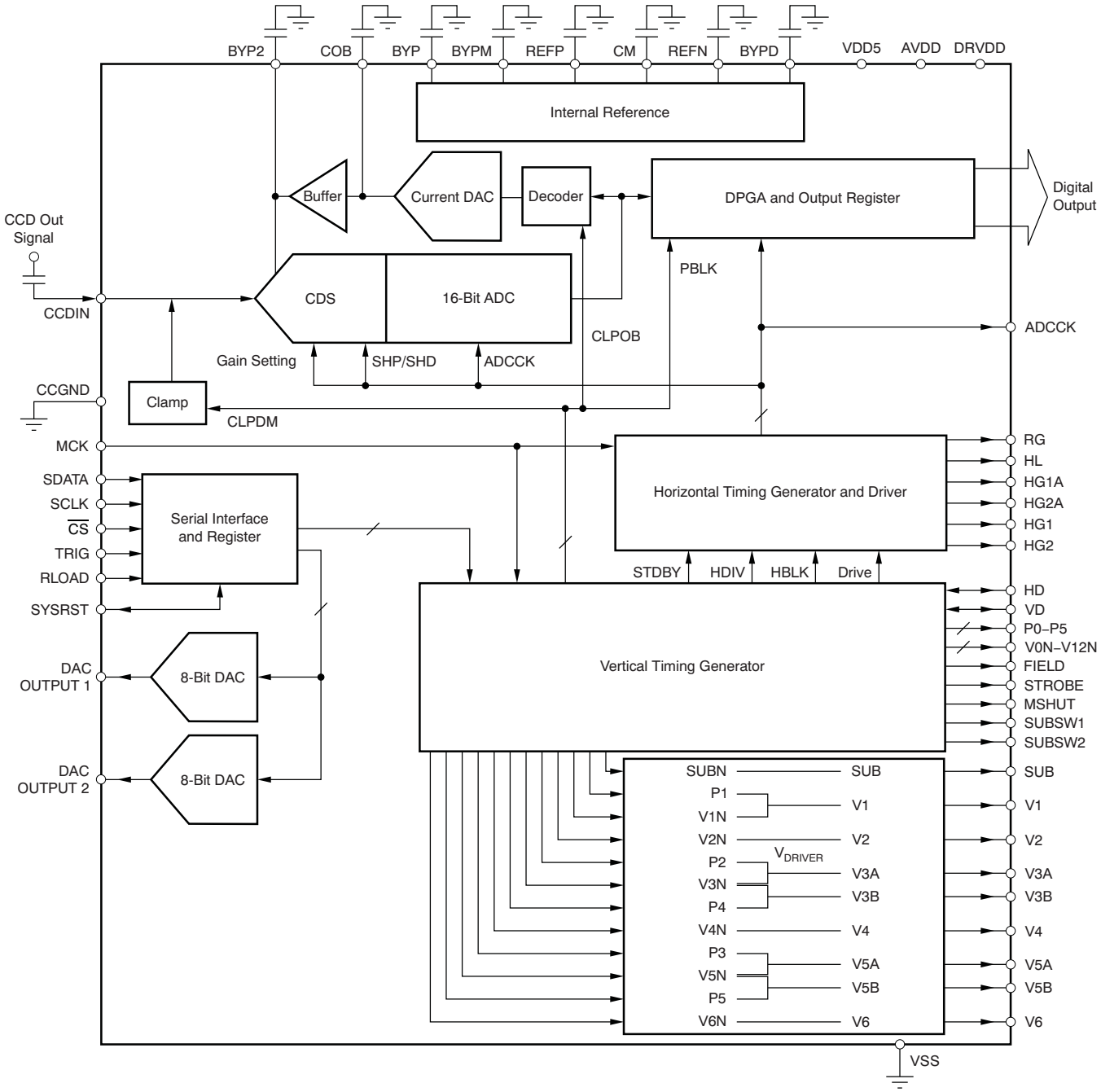
TERMINAL		TYPE[1]	DESCRIPTION
NAME	PIN		
DRVDD	D7	P	Digital output power supply
CH4N	D8	DO	Universal vertical rate signal 4N (for V3B)
B4	D9	DO	Data out bit 4 (VSP01M01 only)
B6	D9	DO	Data out bit 6 (VSP01M02 only)
B5	D10	DO	Data out bit 5 (VSP01M01 only)
B7	D10	DO	Data out bit 7 (VSP01M02 only)
CM	E1	AO	Internal reference[3]
BYPM	E2	AO	Internal reference[4]
REFN	E3	AO	Internal reference[3]
AVDD	E4	P	Analog power supply
AVSS	E5	P	Ground
AVSS	E6	P	Ground
DRVDD	E7	P	Digital output power supply
B3	E8	DO	Data out bit 3 (VSP01M01 only)
B5	E8	DO	Data out bit 5 (VSP01M02 only)
B1	E9	DO	Data out bit 1 (VSP01M01 only)
B3	E9	DO	Data out bit 3 (VSP01M02 only)
B2	E10	DO	Data out bit 2 (VSP01M01 only)
B4	E10	DO	Data out bit 4 (VSP01M02 only)
REFP	F1	AO	Internal reference[5]
V5N	F2	DO	Vertical rate signal 5N (for V5A, V5B)
NC	F3	—	No connection
AVDD	F4	P	Analog power supply
AVSS	F5	P	Ground
AVSS	F6	P	Ground
DRVDD	F7	P	Digital output power supply
V2	F8	VDO	V_{DRIVER} out 2
B0	F9	DO	Data out bit 0 (LSB) (VSP01M01 only)
B2	F9	DO	Data out bit 2 (VSP01M02 only)
SUB	F10	VDO	V_{DRIVER} out for CCD electric shutter
BYPD	G1	AO	DLL bypass[6]
V3B	G2	VDO	V_{DRIVER} out 3B
TPD	G3	DO	Test pin for SHD, CLPDM, HDIV
DVSS	G4	P	Ground
VL	G5	P	V_{DRIVER} power supply
VH	G6	P	V_{DRIVER} power supply
VDD5	G7	P	Digital power supply
VSS5	G8	P	Digital ground
VSS5	G9	P	Digital ground
NC	G10	—	No connection (VSP01M01 only)
B0	G10	DO	Data out bit 0 (LSB) (VSP01M02 only)
TPP	H1	DO	Test pin for SHP, CLPOB, PBLK, HBLK
SYSRST	H2	DI	Asynchronous reset
R_{LOAD}	H3	DI	Register load

(5) Should be connected to ground with a bypass capacitor (0.1 µF). Refer to the *Voltage Reference* section for more detail.
(6) Should be connected to ground with a bypass capacitor. The recommended value is 1000 pF to 0.1 µF; however, actual value depends on the application environment.

Table 2. TERMINAL FUNCTIONS (continued)

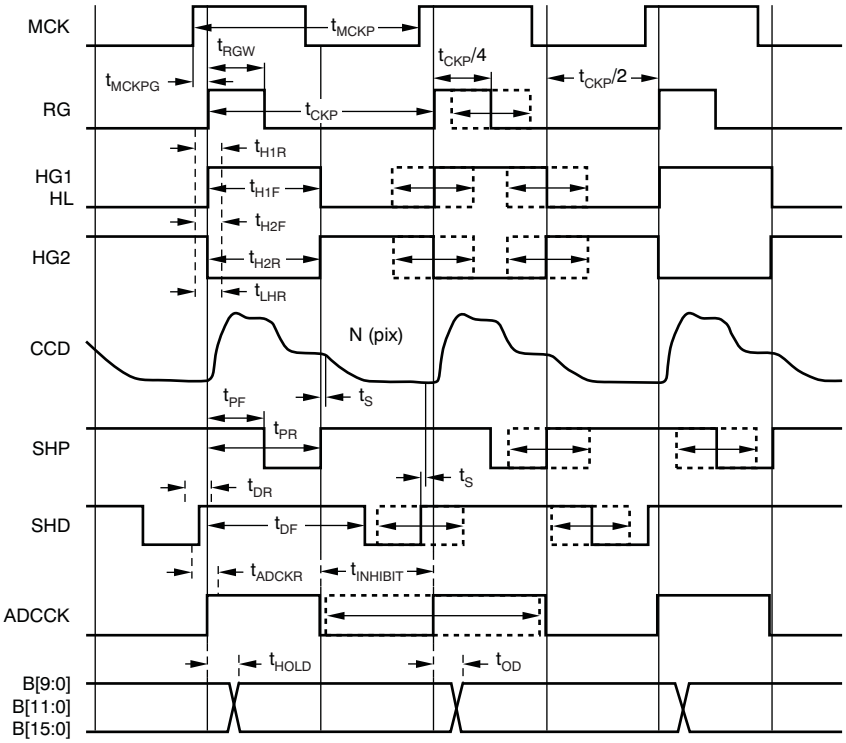
TERMINAL		TYPE[1]	DESCRIPTION
NAME	PIN		
V5A	H4	VDO	V_{DRIVER} out 5A
V3A	H5	VDO	V_{DRIVER} out 3A
STROBE	H6	DO	Strobe signal
VDD5	H7	P	Digital power supply
V6	H8	VDO	V_{DRIVER} out 6
RG	H9	DO	CCD reset gate signal
H1A	H10	DO	CCD horizontal transfer signal 1A
SDATA	J1	DI	Serial data
SCLK	J2	DI	Serial data clock
TRIG	J3	DI	External trigger
VD	J4	DI/O	Vertical sync
SUBSW1	J5	DO	CCD substrate signal switch 1
MSHUT	J6	DO	Mechanical shutter signal
SUBN	J7	DO	CCD electric shutter (for SUB)
HL	J8	DO	CCD horizontal transfer signal
V4	J9	VDO	V_{DRIVER} out 4
ADCCK	J10	DO	Clock for digital output buffer
MCK	K1	DI	Master clock
$\overline{CS}$	K2	DI	Chip select
HD	K3	DI/O	Horizontal sync
SUBSW2	K4	DO	CCD substrate signal switch 2
V1	K5	VDO	V_{DRIVER} out 1
FIELD	K6	DO	Field index signal
V5B	K7	VDO	V_{DRIVER} out 5B
H2A	K8	DO	CCD horizontal transfer signal 2A
H1B	K9	DO	CCD horizontal transfer signal 1B
H2B	K10	DO	CCD horizontal transfer signal 2B

FUNCTIONAL BLOCK DIAGRAM



TIMING CHARACTERISTICS

TG HIGH-SPEED PULSE TIMING



NOTE: Dashed lines indicate programmable parameters.

Figure 1. TG High-Speed Pulse Timing

Table 3. Timing Characteristics for Figure 1

PARAMETER		MIN	TYP	MAX	UNIT
t_{MCKP}	MCK clock period	27.7		83.3	ns
t_{MCKRG}	MCK rising edge to RG rising edge(1)		14		ns
t_{CKP}	Pixel rate	27.7		83.3	ns
t_{RGW}	RG rising edge to RG falling edge(2)	$t_{CKP}/4 - 16t_{CKP}/100$	$t_{CKP}/4$	$t_{CKP}/4 + 15t_{CKP}/100$	ns
t_{H1R}	RG rising edge to HG1 rising edge(2)	$-16t_{CKP}/100$	0	$15t_{CKP}/100$	ns
t_{H1F}	RG rising edge to HG1 falling edge(2)	$t_{CKP}/2 - 16t_{CKP}/100$	$t_{CKP}/2$	$t_{CKP}/2 + 15t_{CKP}/100$	ns
t_{H2R}	RG rising edge to HG2 rising edge(2)	$t_{CKP}/2 - 16t_{CKP}/100$	$t_{CKP}/2$	$t_{CKP}/2 + 15t_{CKP}/100$	ns
t_{H2F}	RG rising edge to HG2 falling edge(2)	$-16t_{CKP}/100$	0	$+15t_{CKP}/100$	ns
t_{LHR}	RG rising edge to HL rising edge(2)	$-16t_{CKP}/100$	0	$+15t_{CKP}/100$	ns
t_{LHF}	RG rising edge to HL falling edge(2)	$t_{CKP}/2 - 16t_{CKP}/100$	$t_{CKP}/2$	$t_{CKP}/2 + 15t_{CKP}/100$	ns
t_{PF}	RG rising edge to SHP falling edge(2)	$t_{CKP}/4 - 16t_{CKP}/100$	$t_{CKP}/4$	$t_{CKP}/4 + 15t_{CKP}/100 + 6$	ns
t_{PR}	RG rising edge to SHP rising edge(2)	$t_{CKP}/2 - 16t_{CKP}/100$	$t_{CKP}/2$	$t_{CKP}/2 + 15t_{CKP}/100 + 6$	ns
t_{DF}	RG rising edge to SHD falling edge(2)	$3t_{CKP}/4 - 24t_{CKP}/100$	$3t_{CKP}/4 - 8t_{CKP}/100$	$3t_{CKP}/4 + 7t_{CKP}/100 + 6$	ns
t_{DR}	RG rising edge to SHD rising edge(2)	$-24t_{CKP}/100$	$-8t_{CKP}/100$	$7t_{CKP}/100 + 6$	ns
t_{ADCKR}	RG rising edge to ADCCK rising edge(3)	$-50t_{CKP}/100$	0	$49t_{CKP}/100$	ns
t_S	Sampling delay for SHP and SHD		3		ns
$t_{INHIBIT}$	Inhibited clock period	4	7	10	ns
t_{ADC}	ADCCK duty		50		%
t_{DOD}	Data out delay (register setting 002h)	0	0	6	ns
t_{HOLD}	Output hold time	$2 + t_{DOD}$			ns
t_{OD}	Output delay (no load)			$27 + t_{DOD}$	ns
DL	Data latency		9 (fixed)		t_{CKP} cycles

(1) Pulse phase can be programmed through the serial interface.
(2) RG pulse width can be programmed through the serial interface. Refer to the *High-Speed Pulse Adjustment* section of the *TG (Timing Generator) Section* for details.
(3) ADCCK phase can also be programmed as a 90-degree step through the serial interface.

SLAVE MODE: VD, HD SPECIFICATIONS

VD, HD Detect

The odd field of the two-field CCD operation and the first field of the even field operation is detected by the VD and HD phase. The delay limit of the VD and HD phase is specified in Figure 2 and Figure 3.

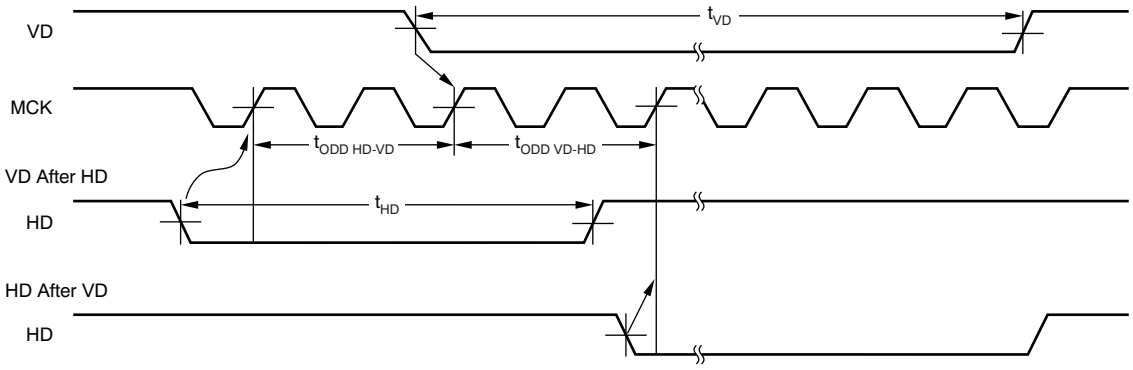


Figure 2. VD, HD Falling Edge Detect

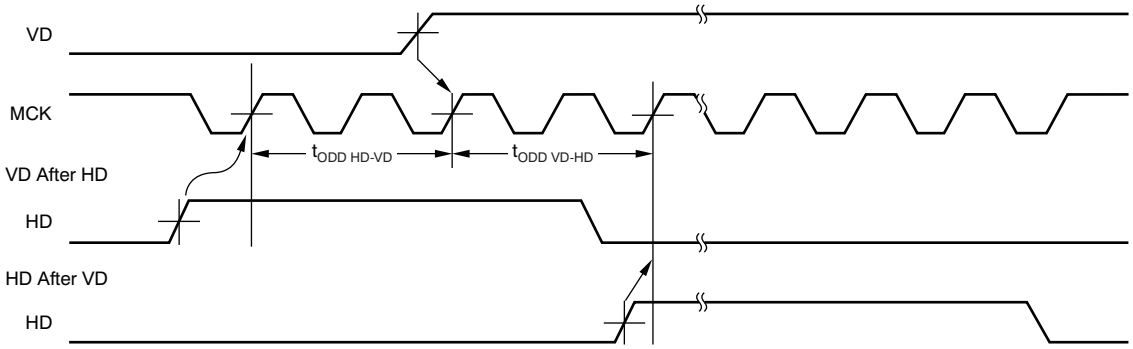


Figure 3. VD, HD Rising Edge Detect

Table 4. Timing Characteristics for Figure 2 and Figure 3 (1)

PARAMETER		MIN	TYP	MAX	UNIT
t_{VD}	VD trail-to-trail	10			τ (MCK cycles)
t_{HD}	HD trail-to-trail	10			τ (MCK cycles)
$t_{ODD\ HD-VD}$	VD trail delay limit for ODD detect (register setting 02Fh[2:0])	0	1	6	τ (MCK cycles)
$t_{ODD\ HD-VD}$	HD trail delay limit for ODD detect (register setting 02Fh[5:3])	0	1	6	τ (MCK cycles)

(1) The VD, HD edge is detected by the rising edge of MCK.

$H_{COUNTER}$ Reset

$H_{COUNTER}$ is reset via HD detection. The timing is shown in Figure 4 and Figure 5.

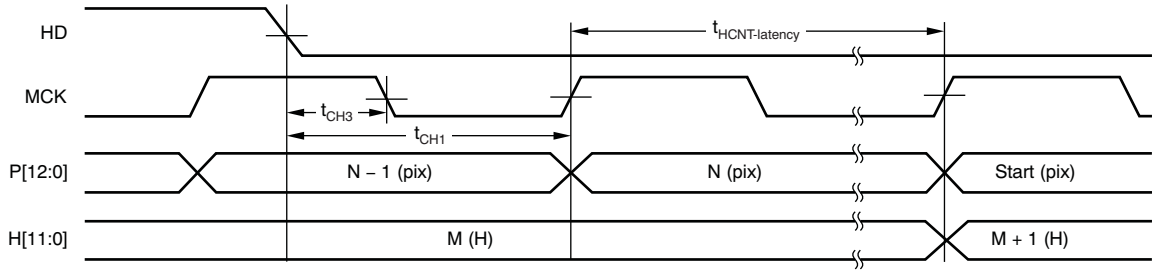


Figure 4. HD Falling Edge Detect

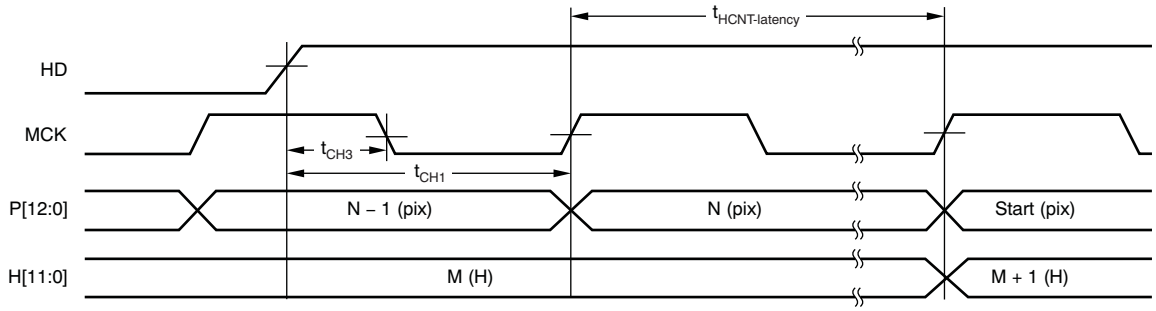


Figure 5. HD Rising Edge Detect

Table 5. Timing Characteristics for Figure 4 and Figure 5 (1)

PARAMETER		REGISTER		MIN	TYP	MAX	UNIT
		VD, HD EDGE 020h[3]	MCK EDGE 020h[2]				
t_{CH1}	HD falling edge to MCK rising edge	0 (falling)	0 (rising)	–6		1	ns
t_{CH2}	HD rising edge to MCK rising edge	1 (rising)	0 (rising)	–6		1	ns
t_{CH3}	HD falling edge to MCK falling edge	0 (falling)	1 (falling)	–4		3	ns
t_{CH4}	HD rising edge to MCK falling edge	1 (rising)	1 (falling)	–4		3	ns
$t_{HCNT-LATENCY}$	$H_{COUNTER}$ reset latency (register setting 034h[3:0])	—	—		6		τ (MCK cycles)

(1) $H_{COUNTER}$ reset timing is selected by MCK edge polarity.

MASTER MODE: HD, VD SPECIFICATIONS

The HD, VD MCK timing is shown in Figure 6 and Figure 7.

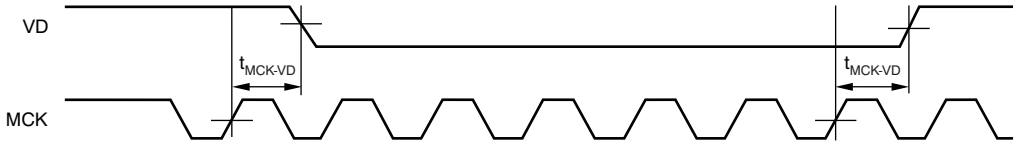


Figure 6. VD MCK Specification

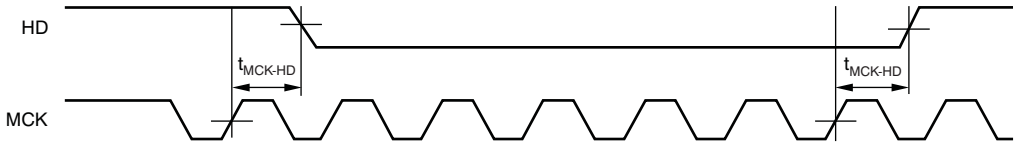


Figure 7. HD MCK Specification

Table 6. Timing Characteristics for Figure 6 and Figure 7

PARAMETER		MIN	TYP	MAX	UNIT
t_{MCK-VD}	MCK rising edge to VD falling edge		10		ns
t_{MCK-HD}	MCK rising edge to HD falling edge		10		ns

SERIAL INTERFACE TIMING SPECIFICATION

The serial interface has two writing modes: standard and continuous write. These modes are shown in Figure 8 and Figure 9.

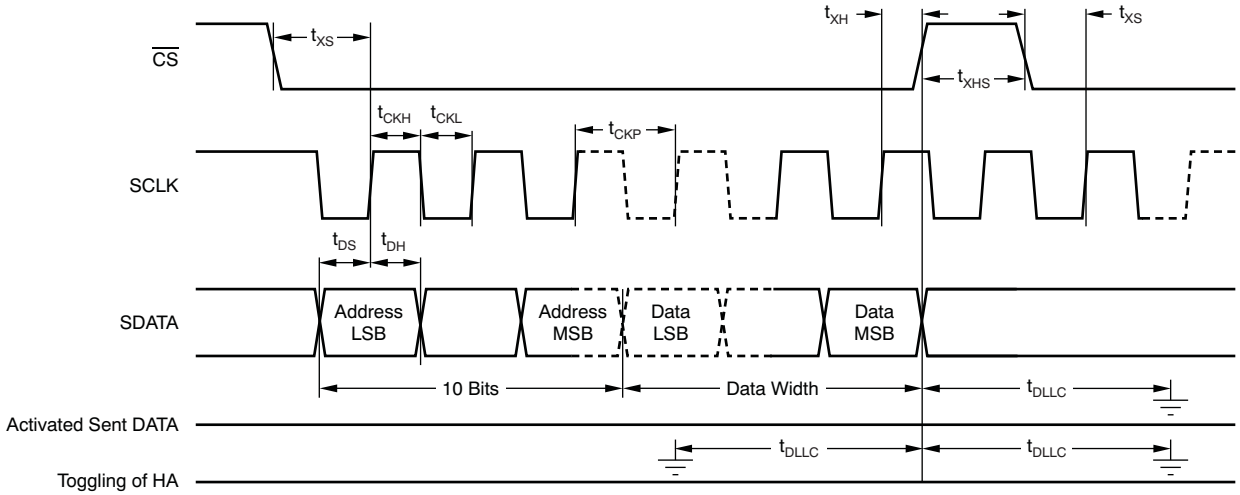


Figure 8. Standard Mode Timing

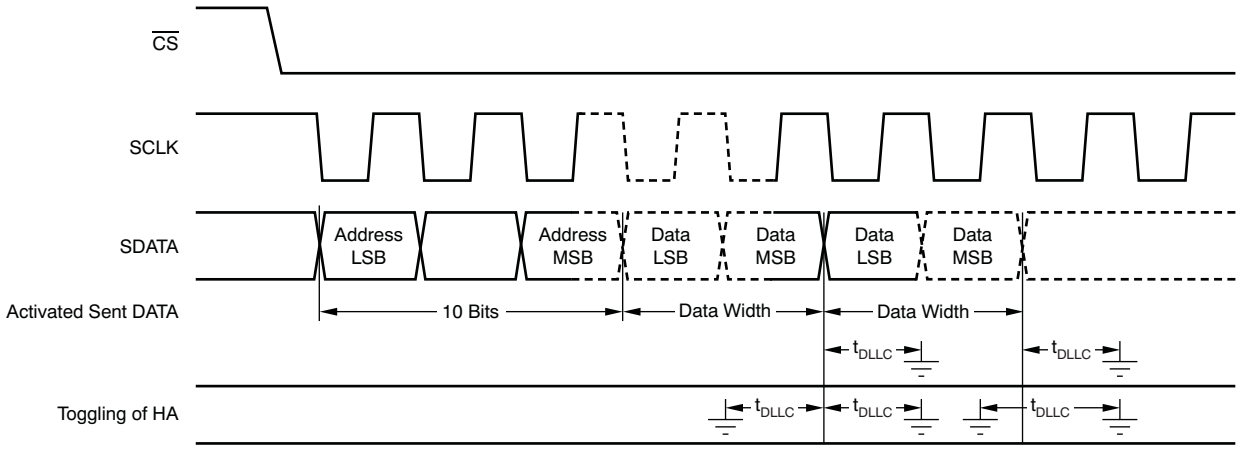


Figure 9. Continuous Write Mode Timing

Table 7. Timing Characteristics for Figure 8 and Figure 9

PARAMETER		MIN	TYP	MAX	UNIT
t_{CKP}	Clock period	50			ns
t_{CKH}	Clock high pulse width	25			ns
t_{CKL}	Clock low pulse width	25			ns
t_{DS}	Data setup time	15			ns
t_{DH}	Data hold time	15			ns
t_{XS}	S_{LOAD} to SCLK setup time	20			ns
t_{XH}	SCLK to $\overline{CS}$ hold time	20			ns
t_{XHS}	$\overline{CS}$ width	20			ns
t_{DLLC}	Data load latency clock			10	MCK CLK

Data shift operation should decode at the rising edges of SCLK while $\overline{CS}$ is low.

Parallel latch timing for each mode is described in Table 8.

Table 8. Parallel Latch

MODE	PARALLEL LATCH TIMING
Standard write	Rising edge of $\overline{CS}$
Continuous write	End of data (MSB)

In addition to the parallel latch, there are several registers dedicated to the specific features of the device; these registers are synchronized with MCK. It takes less than 10 clock cycles for the data in the parallel latch to be written to these registers. Therefore, to complete the data updates, it requires less than 10 clock cycles after parallel latching.

Toggling of HA is inhibited from parallel latch. Refer to the *Serial interface (SPI)* section of the *Common Section* for details.

EQUIVALENT CIRCUITS

Figure 10 shows the HG1A, HG1B, HG2A, and HG2B high-speed driver and load model. The driver supports up to 150 pF. Figure 11 shows the RG and HL high-speed driver and load model. The driver supports up to 10 pF.

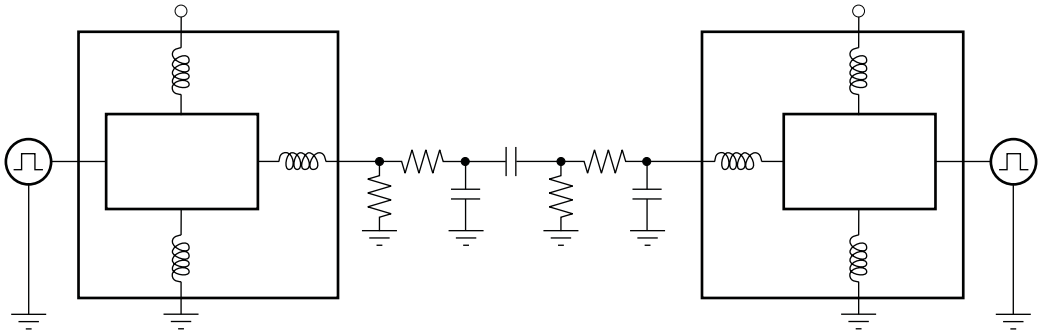


Figure 10. HG Driver and Load Model

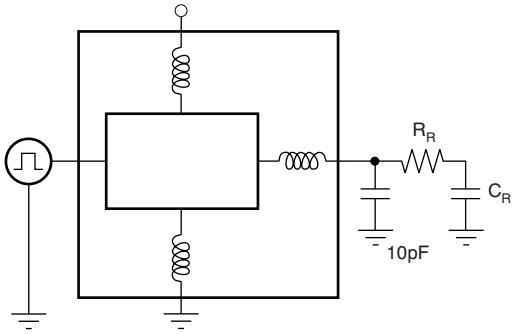
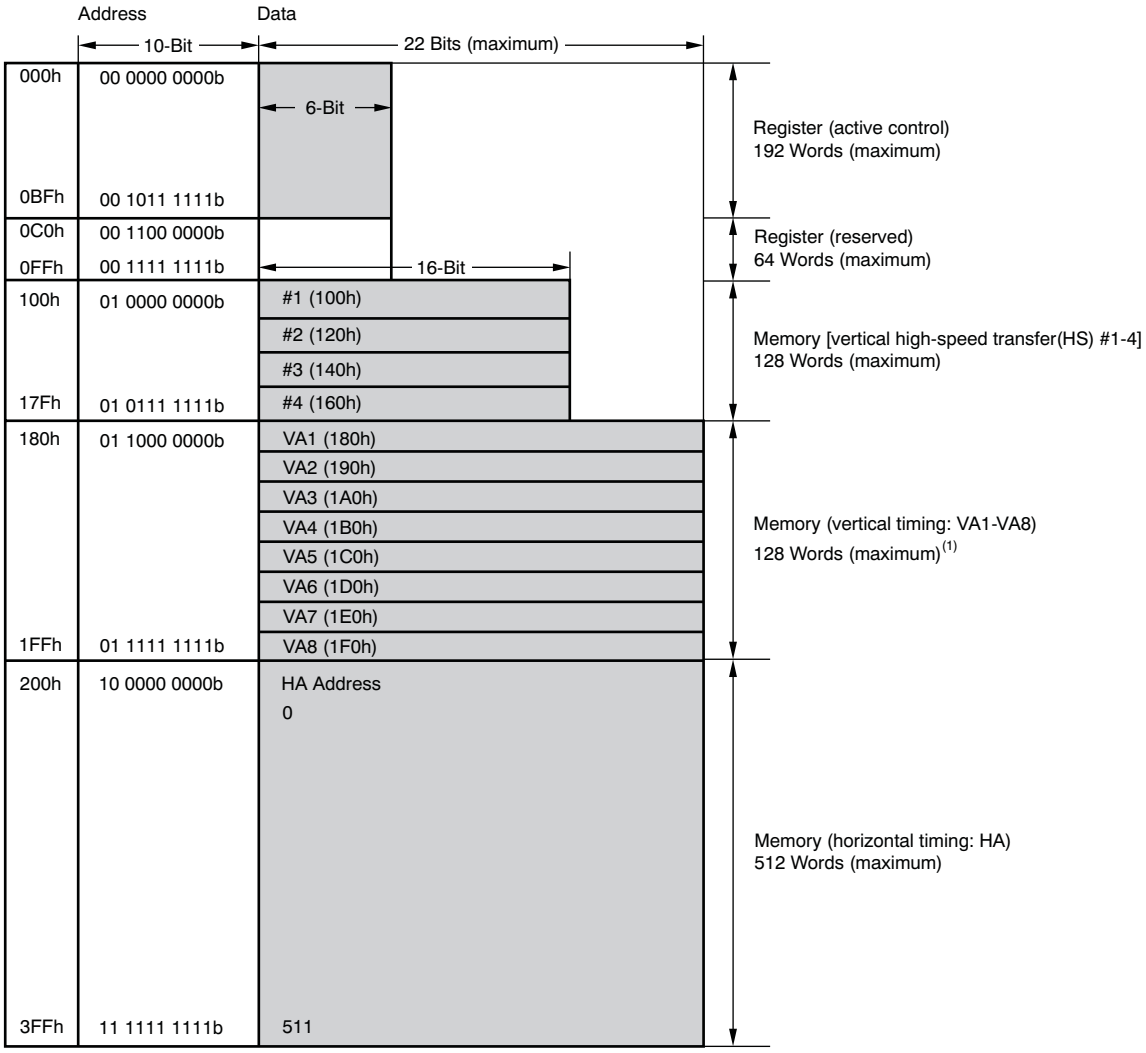


Figure 11. RG Driver and Load Model

COMMON SECTION

REGISTER/MEMORY MAP

Figure 12 shows the TG register/memory map, which has 1024 words of 32-bit instruction (max). The 256-word register area enables active instruction, which requires dynamic operation. The 768-word memory area enables static instruction, which is almost fixed during a frame rate.



NOTE: Shaded cells indicate the area under discussion.

(1) Refer to the *TG Instruction Hierarchy* section of the *TG (Timing Generator) Section* for details.

Figure 12. VSP01M01/VSP01M02 TG Register/Memory Map

SERIAL INTERFACE (SPI)

The SPI functions and timings are controlled through the serial interface, which is composed of three signals: SDATA, SCLK, and $\overline{CS}$. SDATA data are sequentially stored to the shift register at the rising edge of SCLK. Before a write operation, $\overline{CS}$ must go low, and remain low during writing. Refer to *Serial Interface Timing Specification* for further details.

The serial interface command is composed of a 10-bit address and 6-bit, 16-bit, or 22-bit data. Table 9 shows the data width for each address area.

Table 9. Address Data Width(1)

ADDRESS (10-Bit)	DATA WIDTH (Bits)	USAGE
000h-0BFh	6	Register
100h-17Fh	16	HS memory
180h-3FFh	22	HA and VA memory

(1) Refer to *Register/Memory Map* for details.

The SPI has two write modes: standard and continuous.

Standard Write Mode

The VSP01M01 and VSP01M02 support a standard write mode, as shown in Figure 13. Normally, a serial interface command is sent by one address and data combination. The 10-bit address should primarily be sent LSB first; the following 6-bit, 16-bit, or 22-bit data should also sent LSB first. 6-bit, 16-bit, or 22-bit data are stored in the respective register by the 10-bit address at the rising edge of $\overline{CS}$. The stored serial command data change immediately at rising edge of $\overline{CS}$ or are reserved by programmable control. If the data bit does not contain either 6-bits, 16-bits, or 22-bits at the end of the data stream, any empty data bits are ignored.

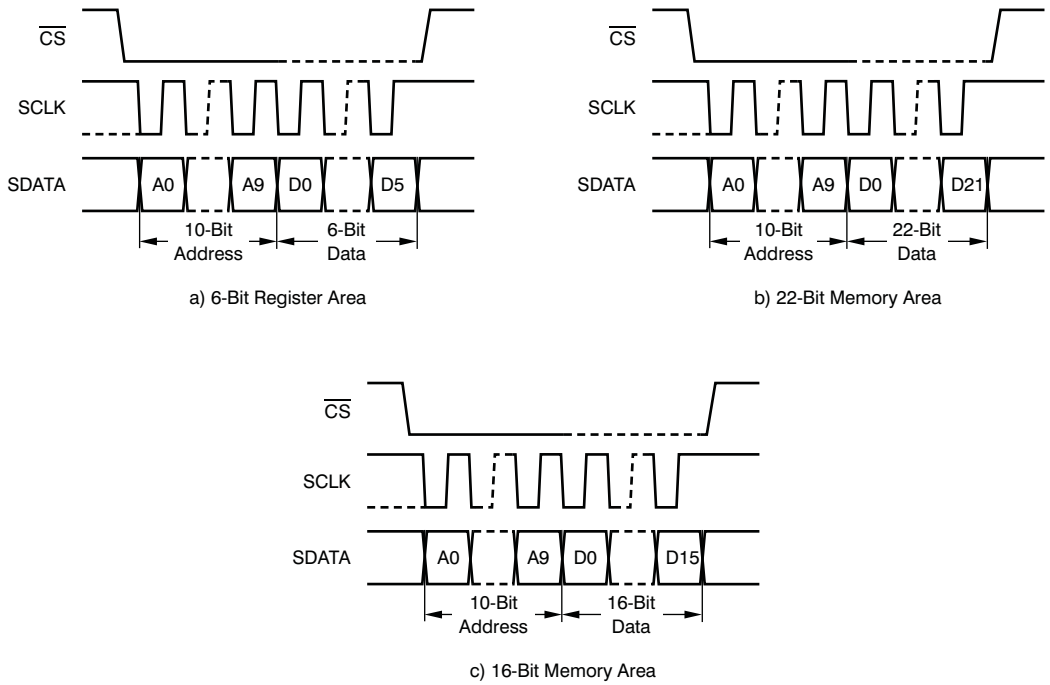


Figure 13. SPI Standard Write Mode

Continuous Write Mode

These devices also support a continuous write mode, as shown in Figure 14. When the input serial data are longer than one set of instructions, the following data stream is automatically recognized as the data of the next address. In this mode, 6-bit, 16-bit, or 22-bit serial command data are stored to the respective registers immediately when those data are fetched. Address and data should be sent LSB first, in the same way as standard write mode. If the data bit does not contain either 6-bits, 16-bits, or 22-bits at the end of the data stream, any empty data bits are ignored.

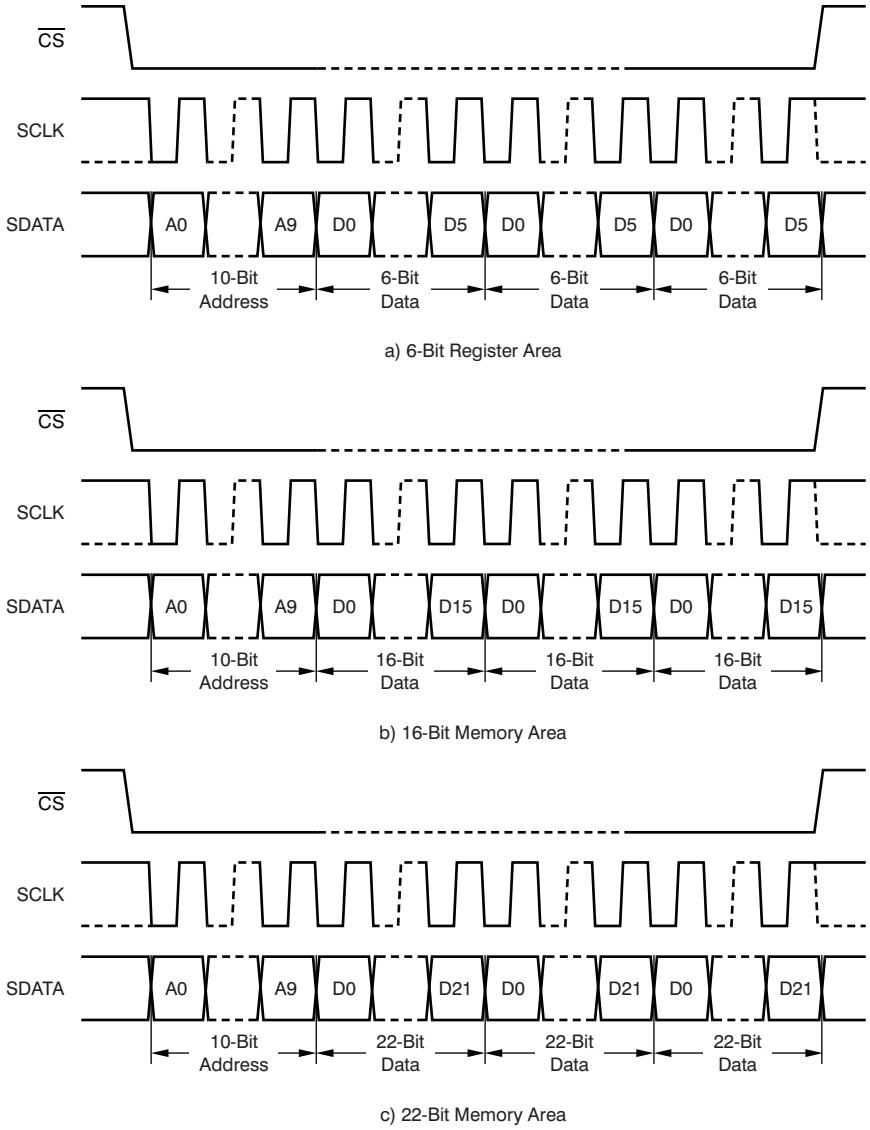


Figure 14. SPI Continuous Write Mode

Mode Confusion

If 22 bits of data are sent to a 6-bit register area, the SPI recognizes *continuous write mode*, because usually only 6-bit data should be sent to 6-bit register area in *standard write mode*, as shown in Figure 15. The end-of-data point is recognized by the rising edge of CS.

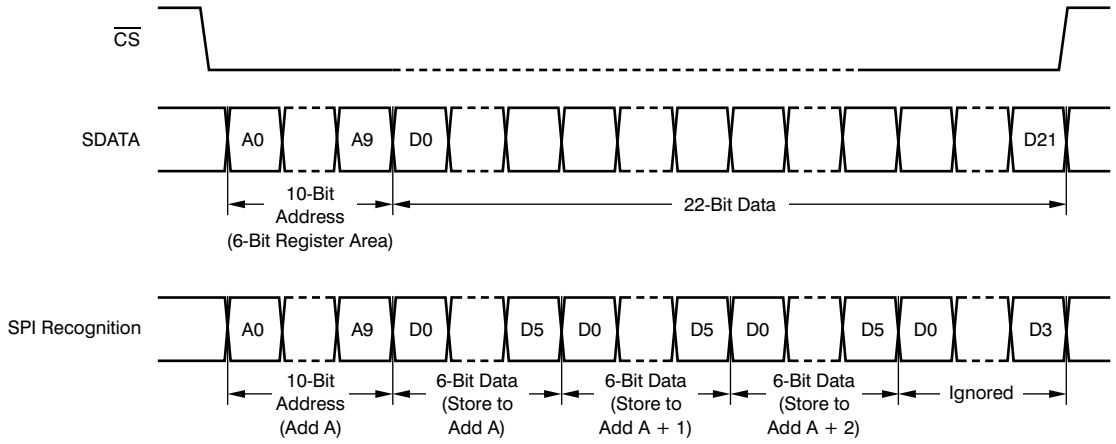


Figure 15. Mode Confusion

SPI recognition is shown in Table 10.

Table 10. SPI Recognition

ADDRESS AREA	DATA WIDTH			
	6-BIT	16-BIT	22-BIT	32-BIT
6-bit register	Standard(1) (one word)	Continuous(2) (two words)	Continuous (three words)	Continuous (five words)
16-bit memory	Ignored	Standard (one word)	Standard(3) (one word)	Continuous (two words)
22-bit memory	Ignored	Ignored	Standard (one word)	Standard (one word)

(1) Shaded cells indicate standard operation.
(2) Continuous = continuous write mode.
(3) Standard = standard write mode.

Read and Write Batting

Address 100h-3FFh is the memory area. HA, VA, and HS access this memory area to read programs. If the SPI writes to the memory area during a program read, the programmed operation is cancelled. SPI operation should be done with *TG disable*. If SPI operation must be done with *TG enable* (TG operating), the SPI must write for a no-read term (no toggling term). For the register area (000h-0FFh), this precaution is not necessary.

REGISTER UPDATE

The update timing of each register is specified in Table 11.

Table 11. Updated Timing

REGISTER ADDRESS	UPDATE TIMING
000h	Real time
001h-01Fh	Timing specified at bits 0-2 of 000h (AFE update)
020h-035h	Real time
036h[2:0]	VD; refer to the *CCD Timing Composition* section of the *TG (Timing Generator) Section* for details.
036h[5:3]	TRIG; refer to the *CCD Timing Composition* section of the *TG (Timing Generator) Section* for details.
037h-0FFh	Timing specified at bit 3 of 000h (TG update)

The AFE register is updated in real time by the R_{LOAD} pin or VD, as shown in Table 12.

Table 12. Update Select Register (AFE)

PARAMETER	REGISTER ADDRESS	DESCRIPTION
AFE UPDATE	000h[0]	0 = Real-time update (default) 1 = Updated by R_{LOAD} pin or VD
AFE UP POL	000h[2:1]	AFE register update signal and polarity 00b = R_{LOAD} rising edge (default) 10b = VD rising edge 01b = R_{LOAD} falling edge 11b = VD falling edge

The TG register can be updated at a specified line number through VA instruction. The update method selection is described in Table 13. In general, this function is used for SUBN control.

Table 13. Update Select Register (TG)

PARAMETER	REGISTER ADDRESS	DESCRIPTION
TG UPDATE	000h[3]	0 = Real-time update (default) 1 = Updated by VA instruction line number Refer to the *Vertical Sequence* section for VA instruction details.

MCK STOP DETECT

The MCK stop detect function is supported, as shown in Table 14. If an MCK stop was detected, all register values are cleared. After an MCK stop detect, a SYSRST is required.

Table 14. MCK Stop Detect Register

PARAMETER	REGISTER ADDRESS	DESCRIPTION
MCK detect	020h[4]	0 = Disabled 1 = Enabled (default)

STANDBY FUNCTION

For increased power savings, this device can be put into a standby mode (power-down mode) through serial interface control when the device is not in use. In this mode, all function blocks are disabled. Current consumption drops to about 2 mA. Because all the bypass capacitors discharge during this mode, a substantial time (usually on the order of 200 ms to 300 ms) is required to return from standby mode. A four-part standby is selected independently, as described in Table 15.

Table 15. Standby Control Register

SECTION	REGISTER ADDRESS	DESCRIPTION	SIGNAL STATUS IN STANDBY
TG	020h[0]	0 = Standby (default) 1 = Normal operation	Refer to the *Signal* section of the *TG (Timing Generator) Section* .
AFE	001h[0]	0 = Normal operation (default) 1 = Standby	Digital output = high impedance
DAC1	001h[1]	0 = Enabled 1 = Disabled (Standby) (default)	Analog output = low
DAC2	001h[2]	0 = Enabled 1 = Disabled (Standby) (default)	—

AFE standby, DAC1 standby, or DAC2 standby should be completed before TG standby if using the VD update method for the the AFE section. If the AFE standby is completed after TG standby, the AFE standby, DAC1 standby, or DAC2 standby are not activated.

SYSTEM RESET

All parameters are reset to the respective default values when the SYSRST pin goes low asynchronously with respect to the system clock. All register and memory values are cleared by SYSRST. SYSRST should be pulled up for operation. Figure 16 shows typical SYSRST implementation with a pull-up resistor.

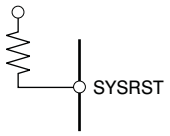


Figure 16. SYSRST Pin

POWER-UP SEQUENCE

When the device is powered up, follow this recommended sequence:

1. Turn on the power supplies for the device.
2. Apply the master clock input to the MCK, VD, and HD signals.
3. Input the serial data for the 6-bit register setting. Input SRG for 16-bit serial data. (10-bit address + 6-bit data). TG disable must be complete. (020h[0] = 0)
4. Input the serial data for $V_{HIGH\ SPEED}$ transfer toggling. Input SRG for 26-bit serial data. (10-bit address + 16-bit data)
5. Input the serial data for V_{RATE} toggling. Input SRG for 32-bit serial data. (10-bit address + 22-bit data)
6. Input the serial data for H_{RATE} toggling. Input SRG for 32-bit serial data. (10-bit address + 22-bit data)
7. Input the serial data for TG enable. Input SRG for 16-bit serial data. (10-bit address + 16-bit data) TG enable must be complete. (020h[0] = 1)

Figure 17 shows the timing for the power-up sequence.

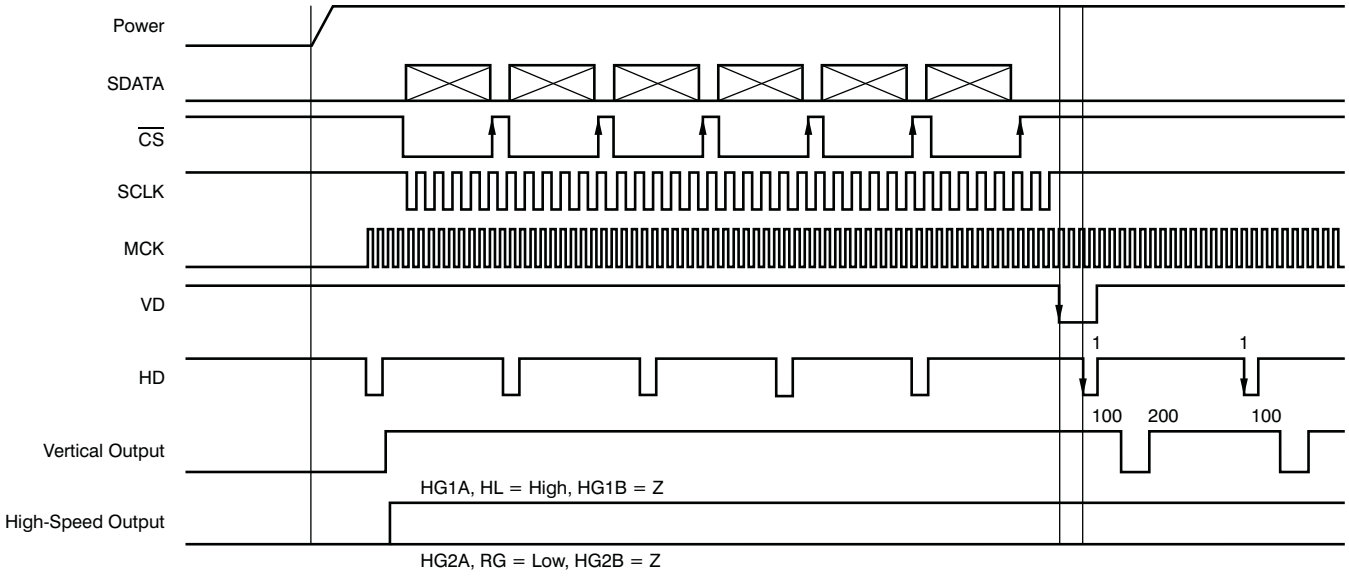


Figure 17. Power-Up Sequence

AFE (ANALOG FRONT-END) SECTION

OVERVIEW

Composition

The VSP01M01/VSP01M02 are complete mixed-signal ICs that contain all of the key features associated with processing of the CCD imager output signal in video cameras, digital still cameras, security cameras, or similar applications. A simplified block diagram of the AFE section is shown in Figure 18. The AFE section includes these features:

- Correlated double sampler (CDS)
- Programmable gain amplifier (PGA)
- Analog-to-digital converter (ADC)
- Input clamp
- Optical black (OB) level clamp loop
- Timing control
- Internal reference voltage generator

It is recommended that an off-chip emitter follower buffer be placed between the CCD output and the device CCDIN input. The serial interface controls PGA gain, clock polarity setting, and operation mode.

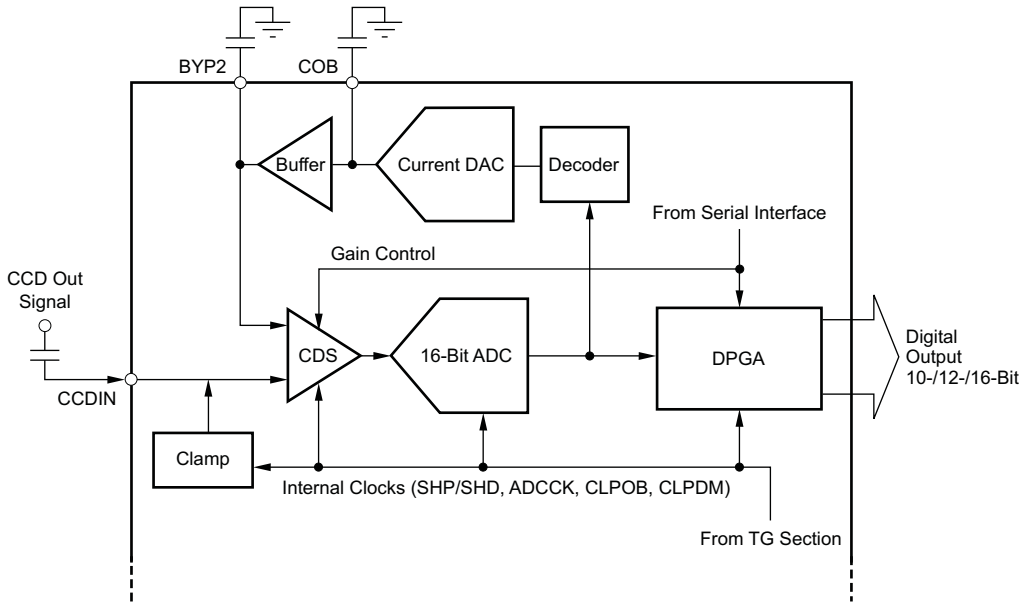


Figure 18. Simplified Block Diagram of the AFE Section

Function

Table 16 shows the major functions of the AFE section.

Table 16. AFE Functional Summary

FUNCTION	RELATED REGISTER	SECTION
Selectable CDS (analog) gain	008h	Programmable Gain
Programmable digital gain	006h, 007h	
Programmable OB clamp level	004h	OB Loop and OB Clamp Level
Standby mode	001h[2:0]	Standby Function
Hot pixel rejection	005h	Hot Pixel Rejection
Selectable register update	000h[2:0]	AFE Register Update Function
Data output enable control	002h[2]	Data Output Enable

CORRELATED DOUBLE SAMPLER (CDS)

The output signal of the CCD image sensor is sampled twice during one pixel period: once at the reference interval and again at the data interval. Subtracting these two samples extracts the video information of the pixel as well as removes any noise, which is common to both intervals. Thus, CDS is very important to reduce the reset noise and the low-frequency noise that are present on the CCD output signal. Figure 19 shows the block diagram of the CDS section. SHP, SHD, CLPDM, and CLPOB are supplied from the TG section; these signals are active low (close).

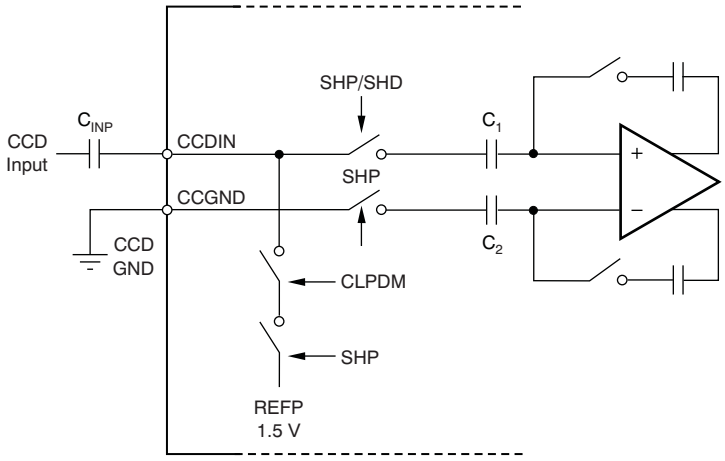


Figure 19. Block Diagram of CDS and Input Clamp

INPUT CLAMP

The buffered CCD output is capacitively coupled to this device. The purpose of the input clamp is to restore the dc component of the input signal, which was lost with the ac coupling, and to establish the desired dc bias point for the CDS. Figure 19 also shows the block diagram of the input clamp. The input level is clamped to the internal reference voltage, CM (1.25 V), during the dummy pixel interval. More specifically, the clamping function becomes active when both CLPDM and SHP are active.

Immediately after power on, the clamp voltage of the input capacitor is not charged. For fast charge-up for clamp voltage, these devices provide a boost-up circuit.

ANALOG-TO-DIGITAL CONVERTER (ADC)

These devices provide a high-speed, 16-bit analog-to-digital converter (ADC). This ADC uses a fully differential pipelined architecture with a correction feature. The ADC error correction architecture is very advantageous to realize a better linearity for lower signal levels. Large linearity errors tend to occur at specific points in the full-scale range and the linearity improves for a signal level below that specific point. The ADC ensures 16-bit resolution across the entire full-scale range.

OB LOOP AND OB CLAMP LEVEL

This device has a built-in OB offset self-calibration circuit (OB loop) that compensates the OB level by using optical black (OB) pixels output from the CCD image sensor. A block diagram of the OB loop and OB clamp circuit is shown in Figure 20.

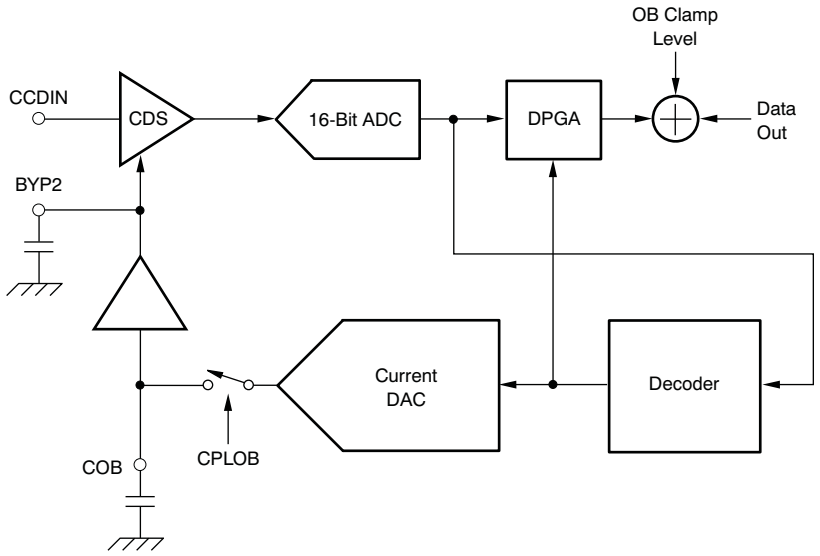


Figure 20. OB Loop and OB Clamp Level

CCD offset is compensated by the convergence of this calibration circuit while activating CLPOB during a period when OB pixels are output from the CCD. Note that the total number of effective pixels is (the CLPOB period –6 pixels).

At the CDS circuit, CCD offset is compensated as a difference between reference level and data level of the OB pixel. These compensated signal levels are recognized as actual *OB levels*, and the outputs are clamped to the OB levels set by the serial interface. These OB levels are the base of black for the effective pixel period thereafter.

Because DPGA, which is a gain stage, is outside the OB loop, OB levels are not affected even if the gain is changed.

Converging time of the OB loop is determined by the capacitor value connected to the COB terminal and output from the current output DAC of the loop. The time constant can be obtained from Equation 1:

$$T = \frac{C}{(16384 \times I_{MIN})}$$

Where:

C is the capacitor value connected to COB,

I_{MIN} is the minimum current (0.15 µA) of the current DAC which is an equivalent current to 1 LSB of the DAC output.

When C = 0.1 µF, T is 40.8 µs. (1)

Slew rate (SR) can be obtained from Equation 2:

$$SR = \frac{I_{MAX}}{C}$$

Where:

C is the capacitor value connected to COB,

I_{MAX} is the maximum current (76 µA) of the current DAC which is an equivalent current to 511 LSB of the DAC output. (2)

Immediately after power-on, the COB capacitors are not charged. For fast start-up, a COB voltage boost-up circuit is provided.

The OB clamp level (digital output value) can be set externally through the serial interface by inputting a digital code to the OB clamp level register. The digital codes to be input and the corresponding OB clamp levels are shown in Table 17.

Table 17. Input Code and OB Clamp Level to Be Set

CODE (Register = 004h)	CLAMP LEVEL (LSB)	
	VSP01M01 (10-Bit)	VSP01M02 (12-Bit)
00000b	16	64
00001b	18	72
—	—	—
00110b	28	112
00111b	30	120
01000b (default)	32	128
01001b	34	136
—	—	—
11110b	76	304
11111b	78	312

PROGRAMMABLE GAIN

The VSP01M01 and VSP01M02 gain ranges from –9 dB to 44 dB. The desired gain is set as a combination of CDS gain and the digital programmable gain amplifier (DPGA). CDS gain can be programmed in the range of –3 dB to 18 dB (–3 dB, 0 dB, 6 dB, 12 dB, 18 dB). –3 dB gain supports large input levels ranging from 1 V to 1.3 V. Digital gain can be programmed in the range of –6 dB to 26 dB in 0.03125-dB steps. Both gains are controlled through the serial interface. Gain changes linearly in proportion to the setting code, as shown in Figure 21.

Table 18. Programmable Gain Register(1)

PARAMETER	REGISTER ADDRESS
CDS (analog) gain	008h
DPGA	006h, 007h

(1) Refer to the *Configuration Register* section for details.

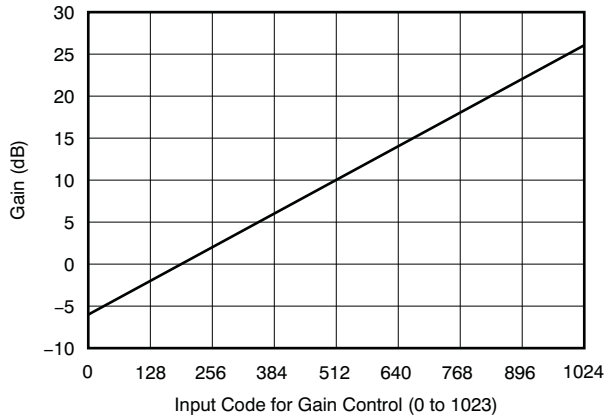


Figure 21. DPGA Setting Code vs Gain

PRE-BLANKING AND DATA LATENCY

These devices have a pre-blanking function. When PBLK = low, all digital outputs are set to '0' after the latching ADCCK clocks counting from PBLK go low to accommodate the clock latency of these devices.

CLOCK TIMINGS FOR THE AFE SECTION

The CDS and the ADC are operated by SHP and SHD; the derivative timing clocks are generated by the on-chip timing generator. The output register and decoder are operated by ADCCK. The digital output data are synchronized with ADCCK. The timing relationship between the CCD signal, SHP, SHD, ADCCK, and the output data is described in the *Timing Characteristics* . CLPOB is used to activate the black level clamp loop during the OB pixel interval and CLPDM is used to activate the input clamping during the dummy pixel interval. In standby mode, ADCCK, SHP, SHD, CLPOB, and CLPDM are internally masked and pulled high. Refer to the *Standby Function* section of the *Common Section* and the *Signal* section of the *TG (Timing Generator) Section* for details.

VOLTAGE REFERENCE

All reference voltages and bias currents used on the device are created from an internal band-gap circuitry. The VSP01M01 and VSP01M02 have symmetrically independent voltage references.

CDS and the ADC primarily use three reference voltages: REFP (1.5 V), REFN (1.0 V), and CM (1.25 V) of the individual reference. REFP and REFN are buffered on-chip. CM is derived as the mid-voltage of the register chain connecting REFP and REFN internally. Twice the difference voltage between REFP and REFN [that is, 2(REFP – REFN)] determines the ADC full-scale range.

REFP, REFN, and CM should be heavily decoupled with appropriate capacitors. Refer to the *Terminal Functions* section for details.

HOT PIXEL REJECTION

Sometimes the OB pixel output signal from the CCD includes an unusual level signal that causes pixel defection. If this level reaches a full-scale level, is may affect OB level stability. These devices have a function that rejects this large unusual pixel level (hot pixel) at the OB pixel. Through this function, these devices improve the CCD yield at camera manufacturing.

The rejection level for hot pixels can be programmed through the serial interface. When a hot pixel comes from the CCD, the VSP01M01 and VSP01M02 omit it and replace it with the previous pixel level from the OB level calculation.

Table 19. Hot Pixel Rejection Register(1)

PARAMETER	REGISTER ADDRESS
Hot pixel rejection	005h

(1) Refer to the *Configuration Register* section for details.

AFE REGISTER UPDATE FUNCTION

Some registers for the AFE section can be selected during update timing. Refer to the *Register Update* section of the *Common Section* for details.

DATA OUTPUT ENABLE

Data out is enabled or disabled by the Data Output Enable register, as shown in Table 20. When disabled, the output level is high impedance.

Table 20. Data Output Enable Register

PARAMETER	REGISTER ADDRESS	DESCRIPTION
OE	002h[2]	0 = Enabled (default) 1 = Disabled (high impedance)

DAC

The VSP01M01 and VSP01M02 provide a two-channel, general-purpose, 8-bit DAC, as shown in Table 21. This DAC can be used for various applications such as CCD bias control, iris control, etc.

Table 21. DAC Input Register(1)

PARAMETER	REGISTER ADDRESS
DAC1	00Ah, 00Bh
DAC2	00Ch, 00Dh

(1) Refer to the *Configuration Register* section for details.

TG (TIMING GENERATOR) SECTION

OVERVIEW

Composition

The VSP01M01 and VSP01M02 support variable CCD timing. For horizontal and vertical sequencing, full programming is available. These devices include a counter, high-speed signal generator, VA selector for frame mode change, output controller, and a TRIG function section.

High-speed signal rise and fall timing are generated through the high-speed signal generator.

For each signal, enabling and initial polarity are controlled by the output controller.

Counter

Table 22 shows the operation of each counter.

Table 22. Counter Operation

COUNTER	INCREASED BY	RESET BY	OUTPUT/OPERATION
Frame	Reset (VA)	VA instruction TRIG	Frame count
VA (vertical)	Reset (HA)	VD EOF (VA) TRIG	Line count Instruction: Frame count reset Initialize Event number start/stop EOF Call HA Address
HA (horizontal)	MCK	HD EOL (HA) TRIG	Pixel count Signal toggling V0N-12N, P0-5, CLPDM, CLPOB, PBLK, HBLK, HDIV, HD, VD Instruction: HS number start/stop EOL
HS ($V_{HIGH\ SPEED}$ transfer)	MCK	HS number start (HA) Repeat (HS)	V_{SIGNAL} toggling Repeat instruction
Event	Trigger V	Event number start (VA)	V_{SIGNAL} control

The HA counter controls the horizontal sequence with the pixel counter. Some signal toggling is controlled by the pixel step. The VA counter controls the vertical sequence with the line counter. The VA calls the HA address by a line step. HS controls the $V_{HIGH\ SPEED}$ transfer sequence with a pixel counter. V_{SIGNAL} toggling is controlled by a pixel step. This counter is started by the HA start command. The loop cycle continues until an HA stop command is issued. An event counter controls $V_{HIGH\text{-}SPEED}$ transfer for an electrical zoom function. This counter operates between the VA start and stop commands.

TRIG Function Section

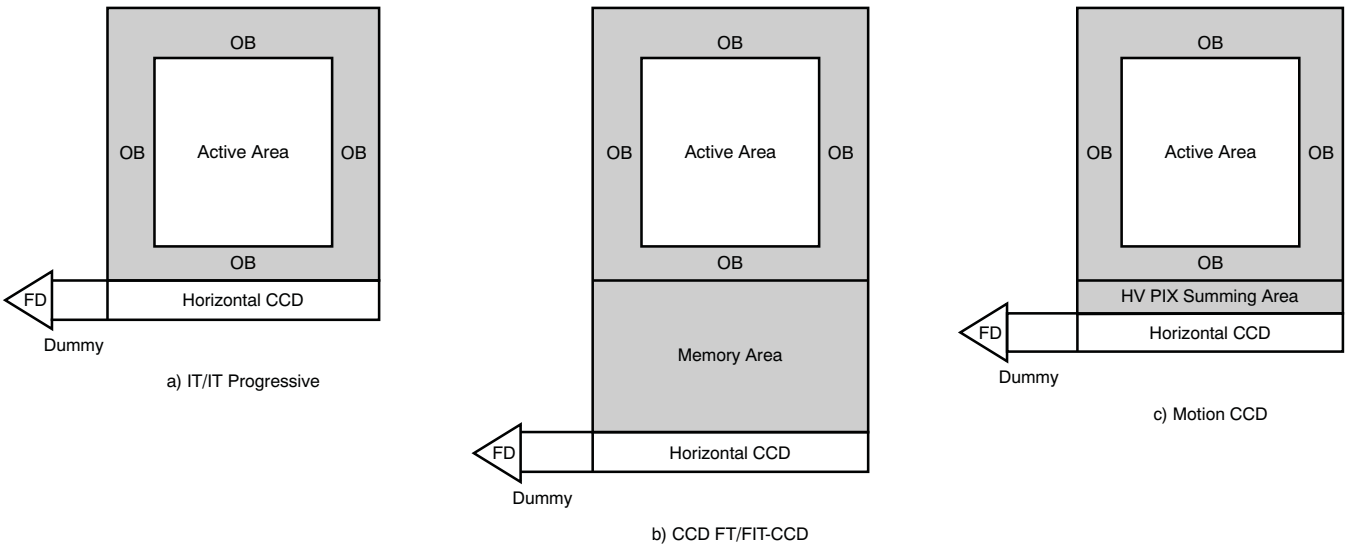
TRIG has the following functionality:

- Frame counter reset function
- Load frame function
- TG stop function

These functions are activated by a register setting.

CCD Support

The VSP01M01 and VSP01M02 TG are designed for various kinds of CCD sensor operation, including IT-CCD as well as FT-CCD, IT progressive CCD, FIT-CCD, and motion CCD, as shown in Figure 22.



NOTE: Shaded cells indicate the area under discussion.

Figure 22. CCD Support Applications

The CCD operation supports these functions:

- Vertical format:
  - IT-CCD: two, three, or four field types
  - IT-progressive CCD
  - FT-CCD
  - FIT-CCD
  - Motion CCD
- Horizontal transfer format:
  - Four channels, two phases
- Floating diffusion reset:
  - One floating diffusion or single phase reset

Timing Range

The VSP01M01 and VSP01M02 have a horizontal 13-bit counter and a vertical 12-bit counter. The counter synchronizes the pixel rate master clock (MCK). The reference signal (HD/VD) has flexibility that can select either the master or slave mode. The timing is programmable so that the TG generates every signal. Apply the program through the serial interface. Refer to the *Register/Memory Map* section of the *Common Section* for details.

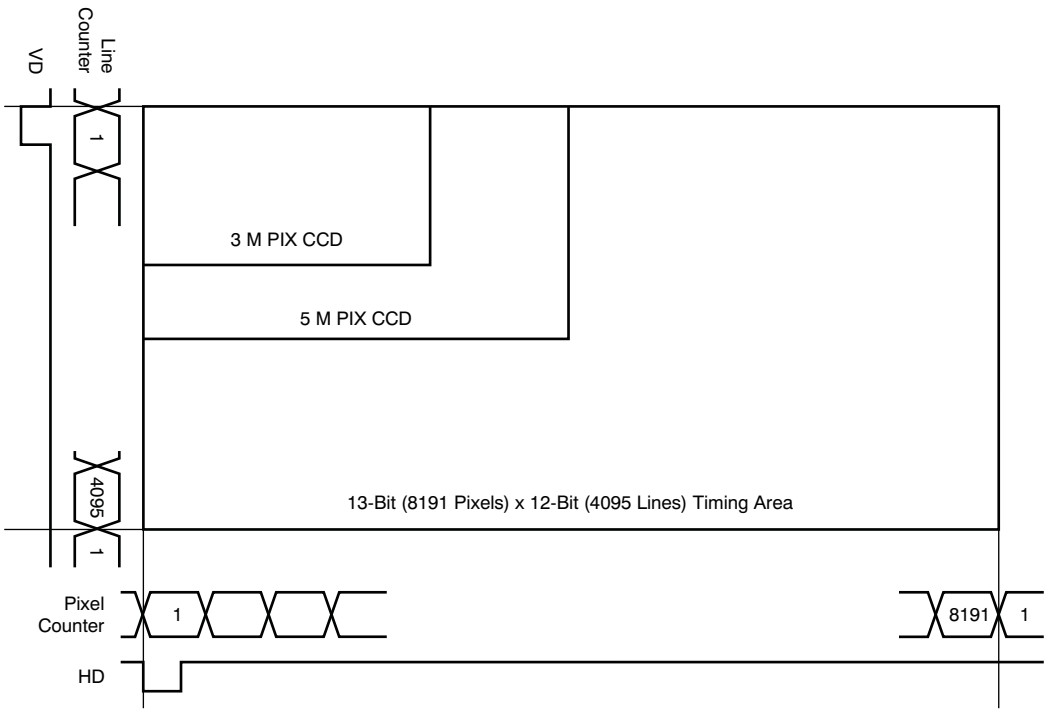


Figure 23. TG Handling Time Range

Operating Mode

The primary operating mode consists of a combination of normal mode, monitor mode, still mode, and motion picture mode.

Normal Mode

Normal mode operates as a basic function with an electric shutter, integration, readout, vertical transfer, and horizontal transfer.

IT-CCD, FT-CCD, and progressive-CCD use a horizontal sequence (see the *Horizontal Sequence* section), vertical sequence (see the *Vertical Sequence* section), and an HBLK function (see the *HBLK Function* section). IT-CCD, progressive-CCD, and most of the FT-CCD use an electric shutter function (see the *Electric Shutter Function* section).

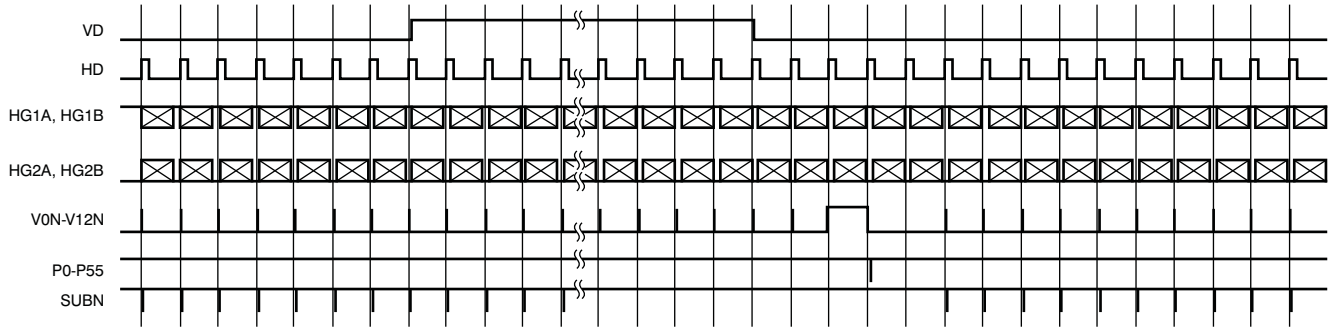


Figure 24. Normal Mode Timing Example

Monitor Mode

Monitor mode operates vertically over several pixel intervals, with an electric shutter, integration, readout, vertical transfer, and horizontal transfer.

IT-CCD, FT-CCD, and progressive-CCD use a horizontal sequence (see the *Horizontal Sequence* section), vertical sequence (see the *Vertical Sequence* section), and an HBLK function (see the *HBLK Function* section). IT-CCD, progressive-CCD, and most of the FT-CCD use an electric shutter function (see the *Electric Shutter Function* section).

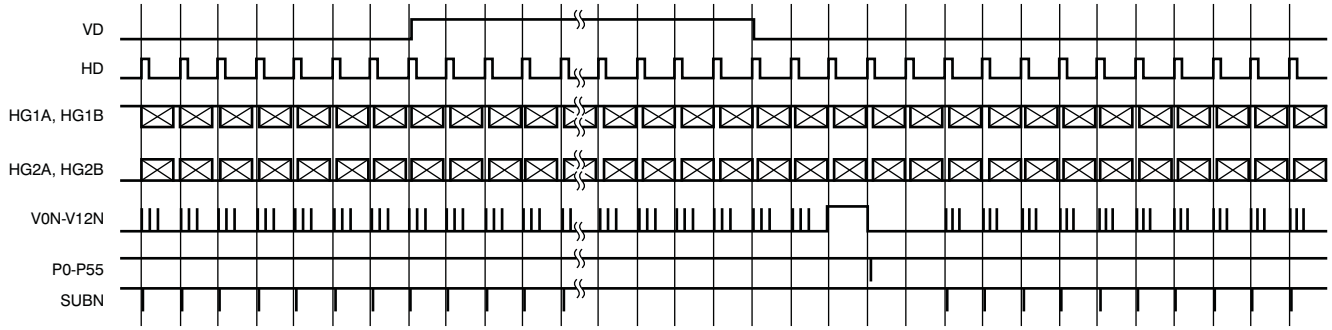


Figure 25. Monitor Mode Timing Example

Still Mode

Still mode operates as a smear dump operation and SUBSW control.

IT-CCD, FT-CCD, and progressive-CCD use a vertical sequence (see the *Vertical Sequence* section), horizontal sequence (see the *Horizontal Sequence* section), vertical high-speed transfer sequence (see the *Vertical High-Speed Transfer (HS) Sequence* section), and an HBLK function (see the *HBLK Function* section). IT-CCD, progressive-CCD, and most of the FT-CCD uses an electric shutter function (see the *Electric Shutter Function* section). IT-CCD and progressive-CCD use a SUBSW function (see the *SUBSW Function* section) for CCD substrate bias control.

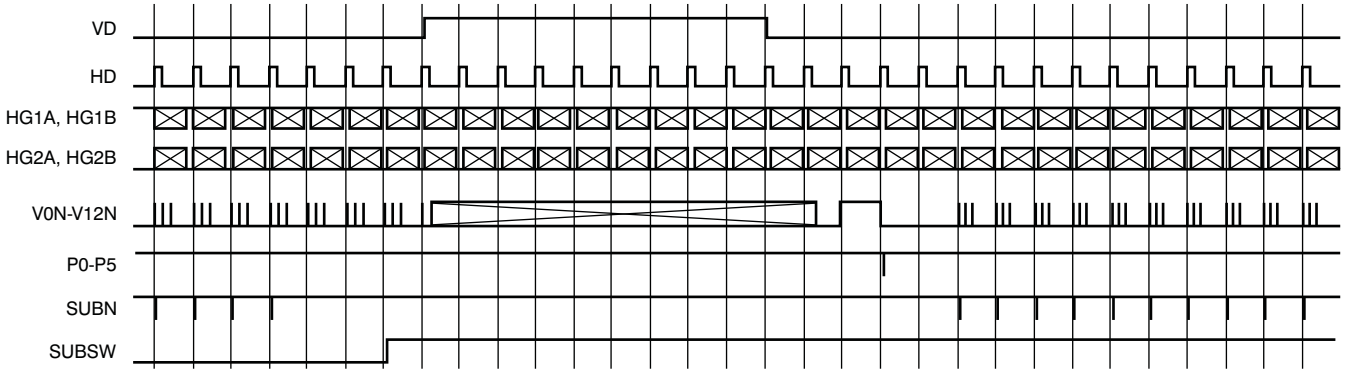


Figure 26. Still Mode Timing Example

Motion Picture Mode

Motion picture mode adds up the pixels in the CCD horizontal and vertical transfer.

IT-CCD is dedicated to this mode and uses a vertical sequence (see the *Vertical Sequence* section), horizontal sequence (see the *Horizontal Sequence* section), an HBLK function (see the *HBLK Function* section), and HDIV function (see the *HDIV Function* section).

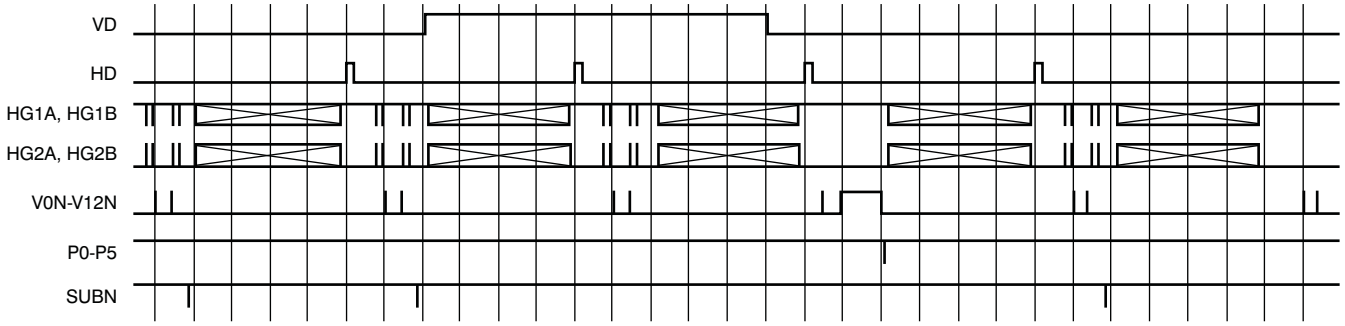


Figure 27. Motion Picture Mode Timing Example

Function

Table 23 summarizes the primary TG section functionality.

Table 23. TG Function

FUNCTION	RELATED REGISTER	SECTION
Adjustable high-speed pulse	002h, 003h, 010h-01Ah	High-Speed Pulse Adjustment
Programmable horizontal pattern	200h-3FFh	Horizontal Sequence
Programmable vertical pattern	180h-1FFh	Vertical Sequence
Programmable V_{CCD} high-speed transfer pattern	100h-17Fh	Vertical High-Speed (HS) Transfer Sequence
Electrical zoom function	030h-033h, 037h-03Eh	
Sync signal selectable (master or slave)	020h	Synchronous Function
Field index for two-field CCD	022h, 02Fh, 035h[0]	
Programmable electrical shutter	08Ch-0A3h	Electric Shutter Function
Programmable strobe	04Ch-07Bh	Strobe Function
Programmable MECH shutter	040h-04Bh	MSHUT Function
Programmable SUBSW	07Ch-08Bh	SUBSW Function
Programmable frame sequence for strobe, MECH shutter, and SUBSW	021h[4], 022h[2]	Frame Count Function
Frame mode control by trigger	021h[3:2], 036h[5:3]	Trigger Function
Waiting mode by trigger	020h[4], 021h[1:0]	
Frame sequence (for strobe, MECH shutter, and SUBSW) control by trigger	021h[4:3], 022h[2]	
Standby mode	020h[0]	Standby Function
Programmable HG signal for horizontal blank	—	HBLK Function
Flexible pixel summing operation	01Bh[2:0]	HDIV Function
Monitor out for internal signal	001h[3], 0B5h	Signal
Selectable HG power	01Ch[1:0]	
Flexible register update	000h[3]	TG Register Update Function

SIGNAL

This device has 32 vertical signals and nine horizontal signals. The universal-purpose signal has flexible usage. Refer to the *Terminal Functions* table for details.

Pin enabling of vertical signals is set by register address 023h-028h. Pin initial polarity is set by register address 029h-02Eh. The initial polarity is applied by the VA *initialize* instruction. (The initial polarity is not applied by the TG operation start). Refer to the *Configuration Register* section for details.

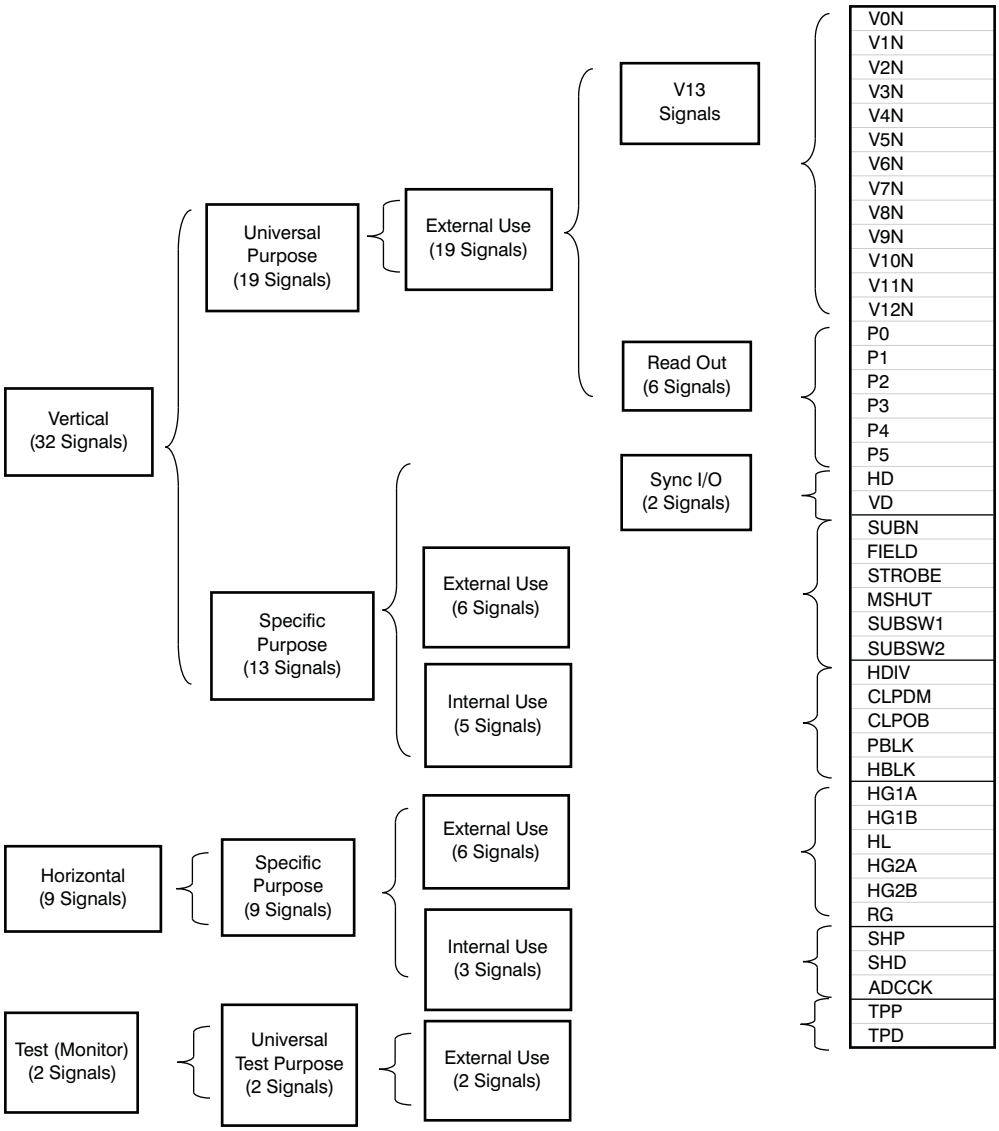


Figure 28. Signal Overview

Programmed Signal (Memory Assignment)

The signal timing (described in Table 24) is specified by the HA (horizontal address) program. Terminal assignment numbers are used by the HA command (data[17:13]). The default output level is fixed except for an MCK stop condition. These signals are disabled with a power-up default. The CLPDM, CLPOB, PBLK, HBLK, and HDIV signal active polarity is low.

Table 24. Memory Assignment Signal

TERMINAL NAME	SIGNAL FUNCTION	TERMINAL ASSIGNMENT	REGISTER ADDRESS		LEVEL			
			ENABLE	INITIAL	POWER-UP DEFAULT	AFE STANDBY	TG STANDBY	TRIG STOP MCK
V[0:12]N	Vertical transfer signal (high-speed transfer)	00001b-01101b (1-13)	023h-025h	029h-02Bh	High	No effect	High	No effect
P[0:5]	Vertical transfer signal (general signal)	10000b-10101b (16-21)	025h-026h	02Bh-02Ch				
CLPDM	Clump dummy signal	11000b (24)	026h[5]	02Ch[5]	Low		Low	
CLPOB	Clump OB signal	11001b (25)	027h [0]	02Dh [0]				
PBLK	Pre-blanking signal (digital out = low)	11010b (26)	[1]	[1]				
HBLK	Horizontal transfer pulse blank	11011b (27)	[2]	[2]				
HDIV	Horizontal transfer pulse divide	11100b (28)	[3]	[3]				
VD	Vertical sync signal (master mode)	11101b (29)	[4]	[4]				
HD	Horizontal sync signal (master mode)	11110b (30)	[5]	[5]				

Decoded Signal (Register Assignment)

The signal timing of Table 25 is specified by the decoder. The decoder refers to the register value of the frame number, line number, or pixel number. Default output levels are fixed except for an MCK stop condition. These signals are disabled with a power-up default.

Table 25. Register Assignment Signal

TERMINAL NAME	SIGNAL FUNCTION	REGISTER ADDRESS				LEVEL			
		ENABLE		INITIAL		POWER-UP DEFAULT	AFE STANDBY	TG STANDBY	TRIG STOP MCK
SUBN	Electric shutter	028h	[0]	02Eh	[0]	High	No effect	High	No effect
FIELD	Field index		[1]		[1]	Low		Low	
STROBE	Strobe signal		[2]		[2]				
MSHUT	Mechanical shutter		[3]		[3]				
SUBSW1	CCD substrate bias control 1		[4]		[4]				
SUBSW2	CCD substrate bias control 2		[5]		[5]				

Phase Controlled Signal (Register Assignment)

The high-speed signal timing is specified by a register. Default output levels are shown in Table 26.

Table 26. Horizontal Signal

TERMINAL NAME	SIGNAL FUNCTION	REGISTER ADDRESS ENABLE		LEVEL POWER-UP DEFAULT	LEVEL DISABLE 01Bh[2]	LEVEL ENABLE AFE STANDBY	LEVEL ENABLE TG STANDBY	LEVEL ENABLE TRIG STOP MCK
HG1A, HL	Horizontal transfer signal 1	01Bh[3]	—	High	01Bh[4] 0 = Low 1 = High	High	High	High
HG1B			01Ch[2]	Z				
HG2A	Horizontal transfer signal 2		—	Low	Low	Low	Low	Low
HG2B			01Ch[2]	Z				
RG	CCD reset signal	Always enable		Toggling	No effect	Low	Toggling	Toggling
SHP	Reference level sampling					High		
SHD	Data level sampling							
ADCCK	ADCCK buffer					Low		

HG Drive

The HG drive power for HG1A, HG1B, HG2A, and HG2B is selected by the HG power select register (01Ch[1:0]), as shown in Table 27.

Table 27. HG Power Select Register

TERMINAL NAME	REGISTER 01Ch[1:0]
HG1A	00 = Minimum
HG1B	01 = Default
HG2A	10 = Mid-range
HG2B	11 = Maximum

The HG drive power can be doubled by a connection between HGAx and HGBx. However, this setting is typically used for power dissipation. If HGBx is not used, disable and do not connect HGBx.

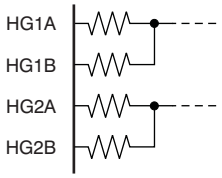


Figure 29. HG Double Power Connection

Monitor Signal

The test pin (TPP, TPD) is set up by address 001h, data bit [3] = 1, as shown in Table 28. Table 29 describes TPP and TPD.

Table 28. Monitor Pin Enable Register(1)

PARAMETER	REGISTER ADDRESS	VALUE
Monitor pin	001h[3]	1 = Enable

(1) Refer to the *Configuration Register* section for details.

Table 29. Test Pin Output Select

REGISTER 0B5h[3:0]	TPP	TPD
1000b (8)	SHP	SHD
1001b (9)	CLPOB	CLPDM
1010b (10)	PBLK	HDIV
1011b (11)	HBLK	—

SHP and SHD are monitored at the TG section output, as shown in Figure 30. The actual sampling point is delayed from the monitor point. The delay time is shown in Figure 30. The actual sampling point delay = delay controller value (003h[1:0] = 0 ns-6 ns) + sampling delay (3 ns).

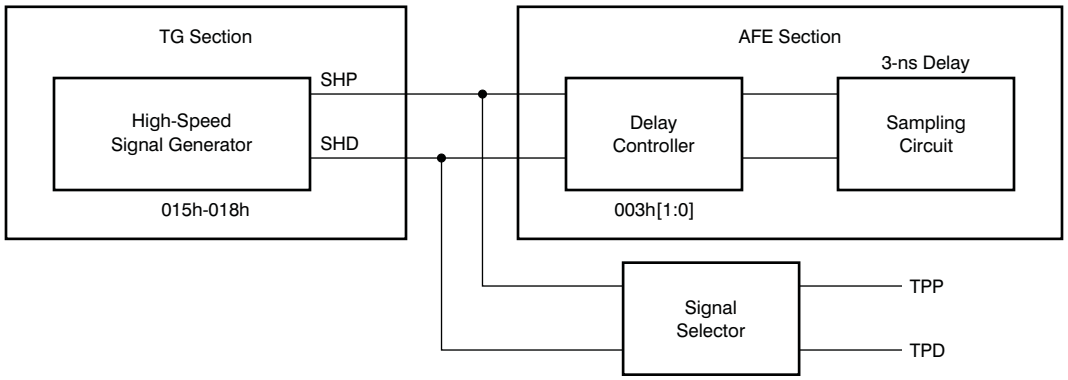


Figure 30. SHP/SHD Monitor Out

HIGH-SPEED PULSE ADJUSTMENT

The high-speed pulse can be adjusted in steps of one pixel clock cycle per 100. The assignment register for each pulse is shown in Table 30. The rising edge of the RG pulse as a reference.

Table 30. High-Speed Pulse Adjustment Register

CONTROL ITEM	TERMINAL NAME	REGISTER ADDRESS		
		FALLING	RISING	DELAY
RG	RG	014h[4:0]	—	—
G1h	G1Ah G1Bh HL	011h[4:0]	010h[4:0]	
G2h	G2Ah G2Bh	012h[4:0]	013h[4:0]	
SHP	SHP	015h[4:0]	016h[4:0]	
SHD	SHD	017h[4:0]	018h[4:0]	003h[1:0]
ADCCK	ADCCK	—	—	019h[5:0] 019h[6]
Data out	B0-B15	—	—	002h[1:0]

RG Control

RG control is described in Figure 31 and Table 31.

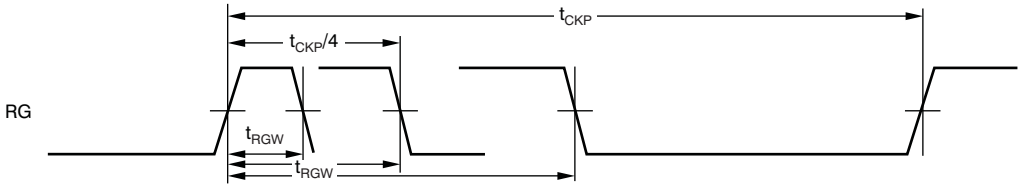


Figure 31. RG Fall Timing

Table 31. RG Fall Register

ADDRESS	NAME	DESCRIPTION		
00 0001 0100b (014h)	RG FALL[4:0]	RG falling edge from RG rising edge ($t_{CKP}/4 - 16t_{CKP}/100 < t_{RGW} < t_{CKP}/4 + 15t_{CKP}/100$)		
		DATA	(DEC)	STEP
		10000b	(16)	–16
		10001b	(17)	–15
		—	—	—
		11111b	(31)	–1
		00000b	(0)	0 (default)
		00001b	(1)	1
		—	—	—
		01110b	(14)	14
		01111b	(15)	15
		STEP is twos complement of data. 1 step = (1 pixel clock term)/100		

HG1 Control

HG1 control is described in Figure 32 and Table 32.

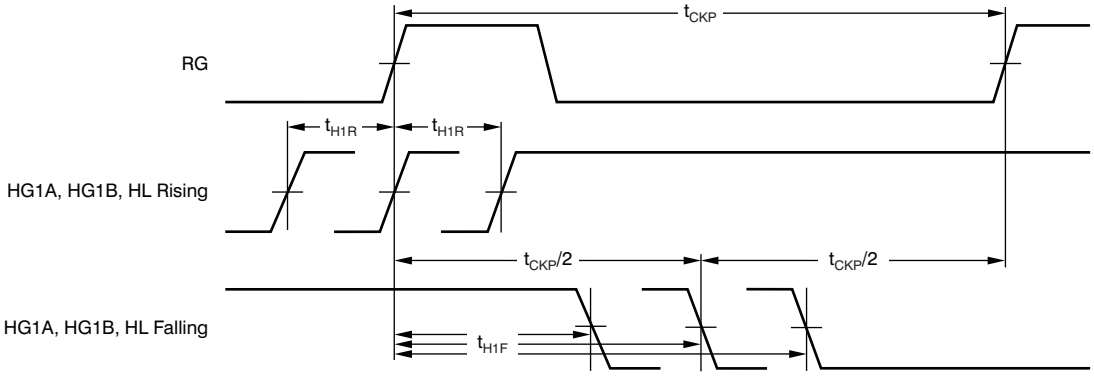


Figure 32. HG1 Timing

Table 32. HG1 Register

ADDRESS	NAME	DESCRIPTION
00 0001 0000b (010h)	HG1 RISE[4:0]	HG1A, HG1B, and HL rising edge from RG rising edge ($–t_{CKP}16/100 < t_{H1R} < t_{CKP}15/100$) Same step control as for Table 31. Default = 00000b.
00 0001 0001b (011h)	HG1 FALL[4:0]	HG1A, HG1B, and HL falling edge from RG rising edge ($t_{CKP}/2 - 16t_{CKP}/100 < t_{H1F} < t_{CKP}/2 + 15t_{CKP}/100$) Same step control as for Table 31. Default = 00000b.

HG2 Control

HG2 control is described in Figure 33 and Table 33.

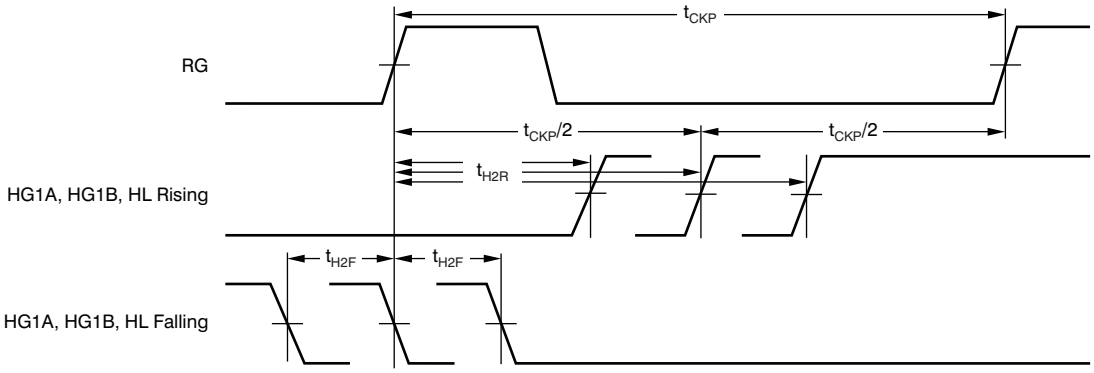


Figure 33. HG2 Timing

Table 33. HG2 Register

ADDRESS	NAME	DESCRIPTION
00 0001 0011b (013h)	HG2 RISE[4:0]	HG2A and HG2B rising edge from RG rising edge ($t_{CKP}/2 - 16t_{CKP}/100 < t_{H2R} < t_{CKP}/2 + 15t_{CKP}/100$) Same step control as for Table 31. Default = 00000b.
00 0001 0010b (012h)	HG2 FALL[4:0]	HG2A and HG2B falling edge from RG rising edge ($-t_{CKP}16/100 < t_{H2F} < t_{CKP}15/100$) Same step control as for Table 31. Default = 00000b.

SHP Control

SHP control is described in Figure 34 and Table 34.

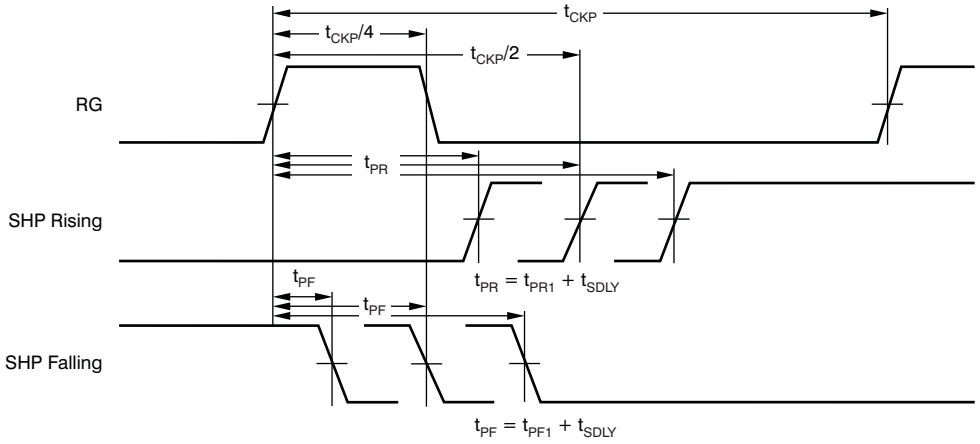


Figure 34. SHP Timing

Table 34. SHP Register

ADDRESS	NAME	DESCRIPTION
00 0001 0110b (016h)	SHP RISE[4:0]	SHP rising edge from RG rising edge ($t_{CKP}/2 - 16t_{CKP}/100 < t_{PR1} < t_{CKP}/2 + 15t_{CKP}/100$) Same step control as for Table 31. Default = 00000b.
00 0001 0101b (015h)	SHP FALL[4:0]	SHP falling edge from RG rising edge ($t_{CKP}/4 - 16t_{CKP}/100 < t_{PF1} < t_{CKP}/4 + 15t_{CKP}/100$) Same step control as for Table 31. Default = 00000b.
00 0000 0011b (003h)	S-DELAY[1:0]	Sampling delay for SHP/SHD (0 ns < t_{SDLY} < 6 ns) 00b = 0 ns (default) 01b = 2 ns 10b = 4 ns 11b = 6 ns

SHD Control

SHD control is described in Figure 35 and Table 35.

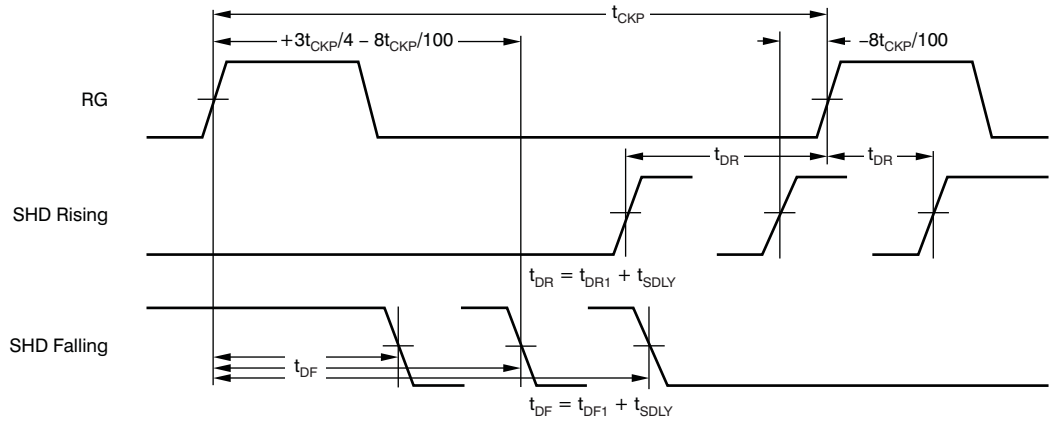


Figure 35. SHD Timing

Table 35. SHD Register

ADDRESS	NAME	DESCRIPTION
00 0001 1000b (018h)	SHD RISE[4:0]	SHD rising edge from RG rising edge ($-24t_{CKP}/100 < t_{DR1} < 7t_{CKP}/100$) Same step control as for Table 31. Default = 00000b.
00 0001 0111b (017h)	SHD FALL[4:0]	SHD falling edge from RG rising edge ($3t_{CKP}/4 - 24t_{CKP}/100 < t_{DF1} < 3t_{CKP}/4 + 7t_{CKP}/100$) Same step control as for Table 31. Default = 00000b.
00 0000 0011b (003h)	S-DELAY[1:0]	Sampling delay for SHP/SHD (0 ns < t_{SDLY} < 6 ns) (0 ns < t_{SDLY} < 6 ns) 00b = 0 ns (default) 01b = 2 ns 10b = 4 ns 11b = 6 ns

ADCCK Control

ADCCK control is described in Figure 36 and Table 36.

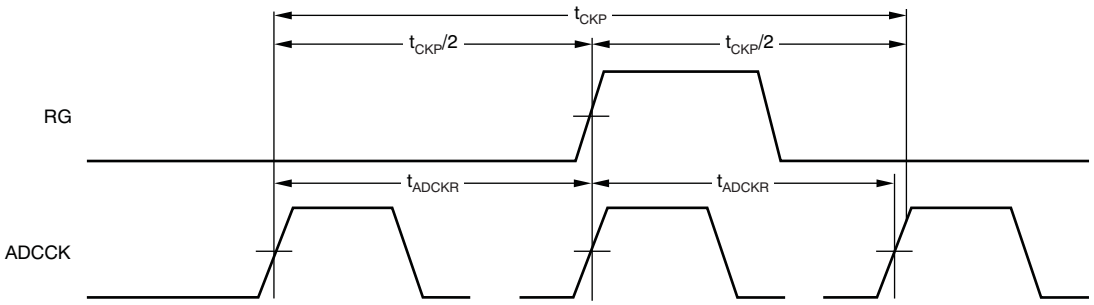


Figure 36. ADCCK Delay Timing

Table 36. ADCCK Delay Register

ADDRESS	NAME	DESCRIPTION				
00 0001 1001b (019h)	ADCCK DELAY[5:0]	ADCCK rising edge from RG rising edge ($-50tM_{CKP}/100 < t_{ADCKR} < 49t_{MCKP}/100$) Default = 00 0000b.				
00 0001 1010b (01Ah)	ADCCK DELAY[6]	Data[6:0] = 01Ah[0] × 26 + 019h[5:0]				
		DATA[6]	**01Ah[0]**	**019h[5:0]**	**(DEC)**	**STEP**
		100 0000b	1	00 0000b	(64)	Reserved
		100 1101b	1	00 1101b	(77)	Reserved
		100 1110b	1	00 1110b	(78)	–50
		100 1111b	1	00 1111b	(79)	–49
		—	—	—	—	—
		111 1111b	1	11 1111b	(127)	–1
		000 0000b	0	00 0000b	(0)	0 (default)
		000 0001b	0	00 0001b	(1)	1
		—	—	—	—	—
		011 0000b	0	11 0000b	(48)	48
		011 0001b	0	11 0001b	(49)	49
		011 0010b	0	11 0010b	(50)	Reserved
		011 1111b	0	11 1111b	(63)	Reserved
		STEP is twos complement of data. 1 step = (1 pixel clock term)/100.				

Data Out Delay Control

Data out delay control is described in Figure 37 and Table 37.

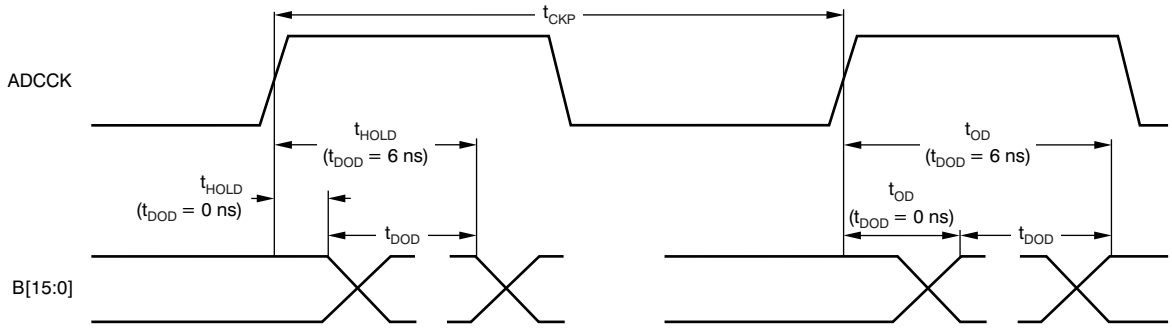


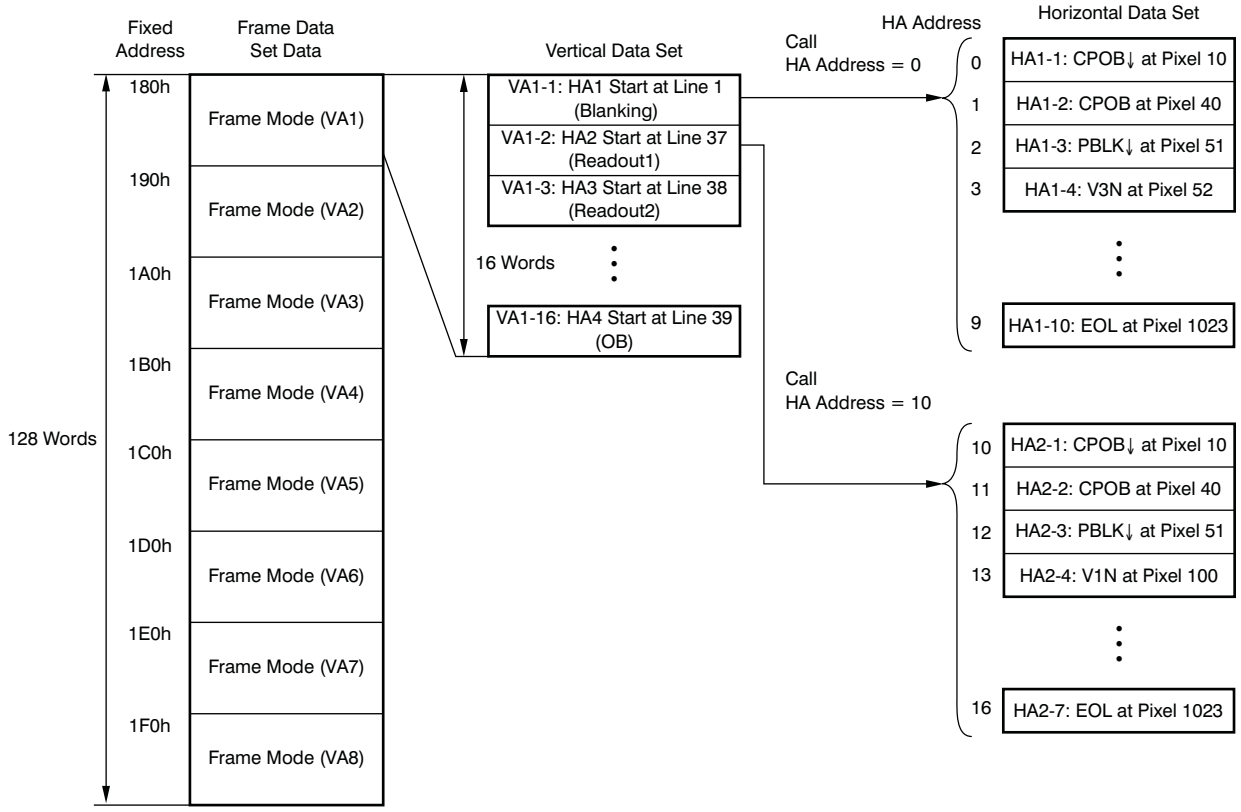
Figure 37. Data Out Delay Timing

Table 37. Data Out Delay Register

ADDRESS	NAME	DESCRIPTION
00 0000 0010b (002h)	DATA OUT DELAY[1:0]	Data out delay 00b to 11b (0 ns < t_{DOD} < 6 ns) 00b = 0 ns (default) 01b = 2 ns 10b = 4 ns 11b = 6 ns

TG INSTRUCTION HIERARCHY

Figure 38 shows the instruction hierarchy. The VA number corresponds to the frame template, and the HA number corresponds to the line template. Each VA has a set of HA number instructions in the vertical timing memory; each HA number has a set of toggling instructions in the horizontal memory. The frame mode is selected by a register (036h).



NOTE: Line number, pixel number, and start of HA address are programmable.

Figure 38. Instruction Hierarchy (Standard Sequence Sample)

CCD TIMING COMPOSITION

TG timing is composed of a vertical data set (VA) that contains eight frames. VA has a horizontal data set (HA), which has several numbers of lines for specific functions. Frame mode is provided by VA. Table 38 shows the frame number for each VA number.

Table 38. Frame Number

PARAMETER	FRAME							
VA number	1	2	3	4	5	6	7	8
Frame number	0	1	2	3	4	5	6	7

Operated VA is updated to the *Frame Now* register by VD. Operated VA is updated to *Frame TRIG* by the TRIG signal with a *Load TRIG frame function*. This updating process is shown in Table 39.

Table 39. Frame Mode Register

PARAMETER	REGISTER ADDRESS	DESCRIPTION
Frame now	036h[2:0]	Set current frame number Default = 000b.
Frame TRIG	036h[5:3]	Set frame number when trigger input Default = 000b.

Figure 39 shows the TG mode transition.

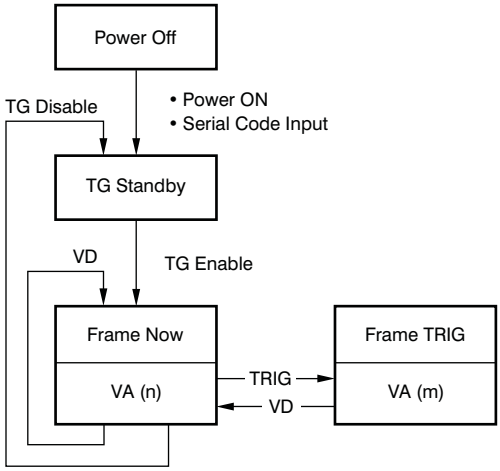


Figure 39. TG Mode Transition

Figure 40 shows the CCD timing composition example, which consists of frames for several operation modes. Each frame counts the line count. *VD (master/slave)* or *TRIG (external trigger)* signal the reset line counter and change during the next frame.

Table 40. TRIG Frame Function Register Setting(1) (2)

PARAMETER	REGISTER ADDRESS	VALUE
VD frame	022h[0]	1 = Enabled
TRIG frame INCR	021h[2]	1 = Enabled
TRIG counter RST	021h[3]	1 = Enabled
Static frame number	036h[2:0]	—
TRIG frame number	036h[5:3]	7

(1) If the TRIG function is not used, *TRIG Frame INCR* and *TRIG Counter RST* should be disabled. Refer to the *TRIG Function Section* of this document
(2) Refer to the *Configuration Register* section for details.

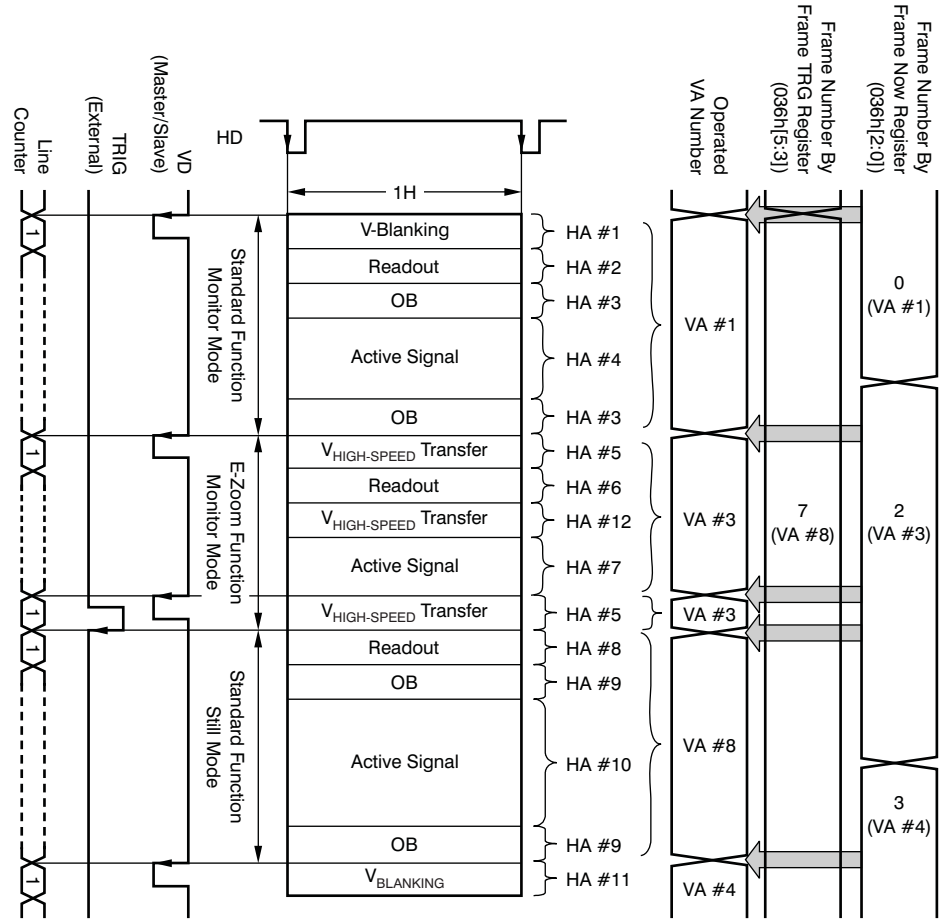


Figure 40. CCD Timing Composition (Example)

SYNCHRONOUS FUNCTION

The system follows either the HD/VD master or slave mode. Select the master/slave mode through register setting (020h[1]: 0 = Slave, 1 = Master), as shown in Table 41. The default setting is slave mode. TG also follows an external HD/VD signal. The master mode generates HD/VD timing according to HA instruction.

Table 41. Sync Mode

MODE	REGISTER 020h[1]	HD AND VD PIN	HD AND VD TIMING	H_{CYCLE}	V_{CYCLE}
Slave	0 (default)	Input	Synchronous		
Master	1	Output	HA command	EOL of HA	EOF of VA

Slave Mode

The system synchronizes the external master clock, HD, and VD. Note that the HD and VD pins are input modes.

VD, HD Detection

VD- and HD-detected edge polarity are selected by register 020h[3]. The selected edge is detected as a rising edge of MCK. VD is detected by the HD phase. If the pixel count between the VD edge and HD edge is within the selected range, VD is detected. The range is selected as shown in Table 42.

Table 42. VD HD Detect Register(1)

PARAMETER	REGISTER ADDRESS	DESCRIPTION
VD HD TRG edge	020h[3]	0 = Falling edge (default) 1 = Rising edge
ODD HD-VD	02Fh[2:0]	VD after HD detect range 0-7 pixel delay Default = 001b
ODD VD-HD	02Fh[5:3]	HD after VD detect range 0-8 pixel delay Default = 001b

(1) Refer to the *Slave Mode: VD, HD Specifications* section for details.

$H_{COUNTER}$ Reset

$H_{COUNTER}$ reset is selected by MCK edge polarity (020h[2]). Table 43 shows the register.

Table 43. MCK Edge Polarity(1)

PARAMETER	REGISTER ADDRESS	DESCRIPTION
VH, HD, and MCK edge	020h[2]	0 = MCK rising edge (default) 1 = MCK falling edge

(1) Refer to the *Slave Mode: VD, HD Specifications* section for details.

Field Index

Field for two-field operation is detected. The detection method is selected to the *VD and HD phase* or *Register*. The *Field* output signal is selected by a register, as shown in Table 44.

ODD detect range is selected by register 02Fh[5:0]. More than seven enabled instructions will always odd detect. Refer to the *Configuration Register* and *Slave Mode: VD, HD Specifications* section for details.

Table 44. ODD/EVEN Detect Register

PARAMETER	REGISTER ADDRESS	DESCRIPTION
Detect method	022h[3]	0 = VD/HD phase (default) 1 = Register (035h[0])
Register select	035h[0]	0 = ODD (default) 1 = EVEN
Field POL	022h[4]	0 = Low at ODD, high at EVEN (default) 1 = High at ODD, low at EVEN
VD even	022h[5]	0 = Disabled (default) 1 = Enabled

Master Mode

The system synchronizes the external master clock, internal HD, and internal VD. Note that the HD and VD pins are output modes. HD and VD timing are provided by the HA command. H_{CYCLE} is provided by an *end-of-line* instruction of the HA command. V_{CYCLE} is provided by the *end-of-frame* instruction of the VA command.

HORIZONTAL SEQUENCE

The horizontal sequence contains toggling information for 1H. Each word describes toggling information. The user must input 2-bit delay information, 2-bit toggling information, 5-bit terminal assignment, and 13-bit pixel count. TG decodes the pixel count and precedes each event sequentially according to the address. A maximum of four signals toggling at the same pixel counter are allowed using the 2-bit delay instruction.

Horizontal Address (HA) Memory

The HA memory area is shown in Table 45.

Table 45. HA Memory Area

PARAMETER	DESCRIPTION
Address	200h-3FFh
Memory area	512 words
Data width	22-bit

Basic Functionality

Table 46 defines the terminal assignment (5-bit) command and pixel address for toggling.

Table 46. HA Bit Function

21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Delay		Toggle		Terminal					Pixel count												

BITS	NAME	DESCRIPTION
21-20	DELAY	Toggling delay pixel number using two bits (0-3)
19-18	TOGGLE	Toggling set to high/low using two bits 00b = Low, 01b = High
17-13	TERMINAL	Terminal assignment using five bit. Terminal: V0N-12N, P0-5, CLPDM, CLPOB, PBLK, HBLK, HDIV, HD (master mode), and VD (master mode) Refer to the *Signal* section for details.
12-0	PIXEL CNT	Toggling of the pixel count using 13 bits (10-8191). Bits below *9* are prohibited. Order in one HA part must be added order. Same pixel count is prohibited.

General Instruction

Table 47 details the V_{CCD} high-speed start and end-of-line commands.

Table 47. HA Instruction Bit Function

21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				1	1	1	1	1													
General instruction				General instruction fix					Pixel count (same as for Table 46)												

GENERAL INSTRUCTION	NAME	DESCRIPTION	
1111b	EOL	The end-of-line reset pixel counter is at the pixel number.	
		Mode	**Pixel Number**
		Master	Target H_{CYCLE} – 1 + register 034h[3:0]
		Slave	8191
0001b	Start HS 1	Start V_{CCD} high-speed transfer (HS 1)	
0010b	Start HS 2	Start V_{CCD} high-speed transfer (HS 2)	
0011b	Start HS 3	Start V_{CCD} high-speed transfer (HS 3)	
0100b	Start HS 4	Start V_{CCD} high-speed transfer (HS 4)	

GENERAL INSTRUCTION	NAME	DESCRIPTION
0101b	Stop HS	Stop V_{CCD} high-speed transfer

$V_{HIGH\text{-}SPEED}$ Transfer (HS) Instruction

Two sets of commands specify the HS start/stop information and the HS toggling pixel address information. As shown in Table 48, HS start/stop information is part of the horizontal memory. Four types of HS are available using the [21:18] bit instruction. An HA programming example is shown in Table 48. Note that sync mode is a slave mode.

Table 48. Horizontal Memory Example

MEMORY ADDRESS		DELAY [21:20]	TOGGLING [19:18]	TERMINAL ASSIGNMENT [17:13]	PIXEL COUNT [12:0]
FIXED [31]	SEQUENTIAL [30:22]				
1	0 0000 0000b (A1h-1h)	00b	00b	11001b (CLPOB)	0 0000 0000 1010b (10)
1	0 0000 0001b (A1h-2h)	00b	01b	11001b (CLPOB)	0 0000 0010 1000b (40)
1	0 0000 0010b (A1h-3h)	00b	00b	11011b (HBLK)	0 0000 0011 0011b (51)
1	0 0000 0011b (A1h-4h)	01b	01b	00001b (V0N flexible)	0 0000 0011 1111b (63)
1	0 0000 0100b (A1h-5h)	00b	01b	00010b (V1N flexible)	0 0000 0100 0000b (64)
1	0 0000 0101b (A1h-6h)	00b	00b	00001b (V0N flexible)	0 0000 0110 0100b (100)
1	0 0000 0110b (A1h-7h)	00b	00b	00010b (V1N flexible)	0 0000 1001 0110b (150)
1	0 0000 0111b (A1h-8h)	00b	01b	11011b (HBLK)	0 0000 1111 0001b (241)
1	0 0000 1000b (A1h-9h)	00b	00b	11000b (CLPDM)	0 0000 1111 1010b (250)
1	0 0000 1001b (A1h-10h)	00b	01b	11000b (CLPDM)	0 0001 0001 1000b (280)
1	0 0000 1010b (A1h-11h)	1111b (EOL)		11111b (general instruction)	1 1111 1111 1111b (8191)

Figure 41 shows the horizontal timing. Sequentially input 22-bit data for each toggling position.

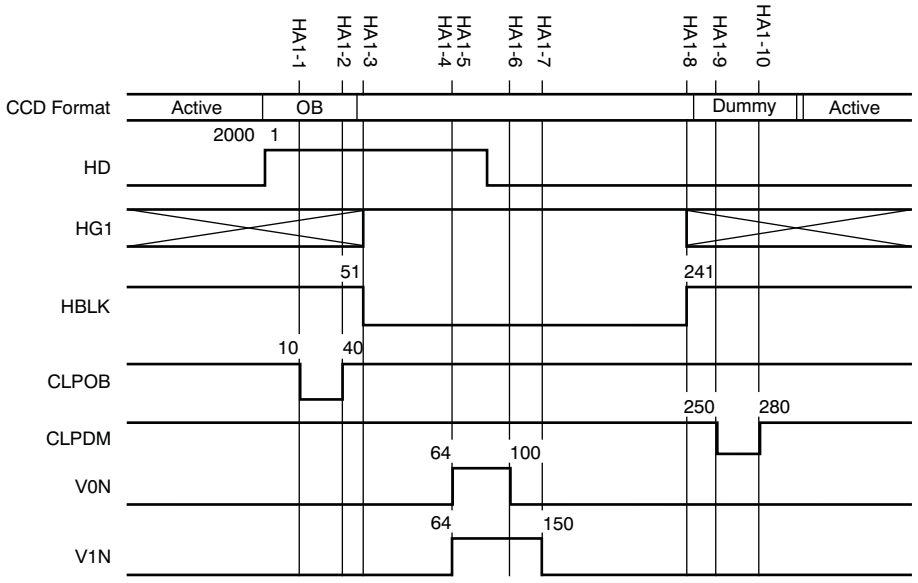


Figure 41. Horizontal Timing Example

VERTICAL SEQUENCE

The vertical sequence consists of elements of the *Horizontal Sequence* . Each word contains a horizontal memory address and a line number, which is applied for the operation. The user must input 1-bit loading information, 9-bit HA address, and 12-bit line number. The TG decodes the line count and precedes each event sequentially according to the address.

Vertical Address (VA) Memory

The VA is detailed in Table 49 and Table 50.

Table 49. VA Memory Area

PARAMETER	DESCRIPTION
Address	180h-1FFh
Memory area	128 words
Data width	22-bit

Table 50. VA Number Start Address

VA NUMBER	1	2	3	4	5	6	7	8
Start address	180h	190h	1A0h	1B0h	1C0h	1D0h	1E0h	1F0h

Basic Functionality

Table 51 defines the HA (horizontal address) command and HA pattern apply line number command.

Table 51. VA Bit Function

21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																					
(1)	HA ADD									LINE											

(1) V_{LOAD}.

BITS	NAME	DESCRIPTION
21	V_{LOAD}	Vertical timing load, fixed at '0'
20-12	HA ADD	HA address load using 9-bit, HA address = (HA physical memory address) – 512
11-0	LINE	Line count using 12-bit (1-4095). Order in one *VA* must be added order. Same line count is prohibited.

MISC Instruction

Table 52 shows the vertical command apply line number command.

Table 52. VA Instruction Bit Function

21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					X	X	X	X	X												
(1)	Instruction				Don't care					LINE											

(1) V_{LOAD}.

BITS	NAME	DESCRIPTION
21	V_{LOAD}	Vertical timing load, fixed at '0'
11-0	LINE	Line count using 12-bit (1-4095). Order in one *VA* must be added order. Same line count is not prohibited.

INSTRUCTION	NAME	DESCRIPTION	
1111b	EOF	End of frame, reset line counter. In master mode, renew frame mode.	
		MODE	**LINE NUMBER**
		Master Slave	Target V_{CYCLE} + 1 4095
0001b	Initialize	Initialize pin output at line 1. (V0N-12N, P0-5, SUBN, CLPDM, CLPOB, PBLK, HBLK, HDIV, FIELD, STROBE, MSHUT, SUBSW1, and SUBSW2)	
0010b	Reserved	Reserved	
0011b	R_{UPDATE}	Register update. Renew TG register (H037-H0A3) at line number.	
0100b	Start event 1	Start V_{CCD} high-speed transfer (dynamic mode) 1 at line number.	
0101b	Start event 2	Start V_{CCD} high-speed transfer (dynamic mode) 2 at line number.	
0110b	End event	Stop V_{CCD} high-speed transfer (dynamic mode) at line number.	
0111b	Frame counter reset	Frame counter reset. Reset and start frame counter at line 1.	

VA programming is shown in Table 53. Sync mode is a slave mode.

Table 53. Vertical Memory Example

MEMORY ADDRESS		LOAD [21]	HA ADDRESS (0-511) OR INSTRUCTION [20:12]	LINE COUNT [11:0]
FIXED [31:30]	SEQUENTIAL [29:22]			
01b	1000 0000b (VA1-0)	0	0 0000 0000b (A1h)	0000 0000 0001b (01)
01b	1000 0001b (VA1-1)	1	0 0010 0000b (initialize)	0000 0000 0001b (01)
01b	1000 0010b (VA1-2)	1	0 1110 0000b (frame count reset)	0000 0000 0001b (01)
01b	1000 0011b (VA1-3)	0	0 0001 0000b (A2h)	0000 0010 0001b (33)
01b	1000 0100b (VA1-4)	0	0 0001 1101b (A3h)	0000 0010 0010b (34)
01b	1000 0101b (VA1-5)	0	0 0011 0011b (A4h)	0000 0010 0011b (35)
01b	1000 0110b (VA1-6)	0	0 0000 0001b (A1h)	0000 0010 0100b (36)
01b	1000 0110b (VA1-7)	1	1 1110 0000b (end of frame)	1111 1111 1111b (4095)

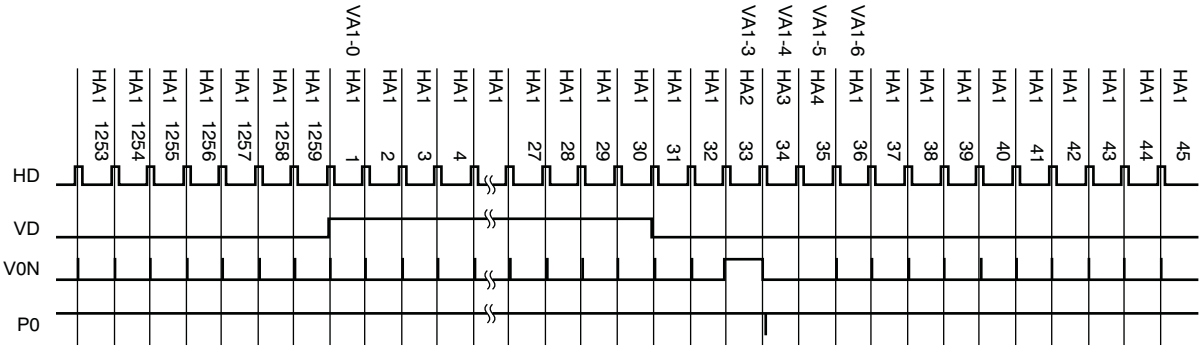


Figure 42. Vertical Timing Example

VERTICAL HIGH-SPEED (HS) TRANSFER SEQUENCE

The vertical high-speed (HS) transfer shifts a charge for a specified number of lines. The still mode and electric zoom use HS. Counter start of HS has three pixel delays from the *Start HS* command of HA. The vertical high-speed transfer has both a programmed operation mode and register dynamic mode.

HS Memory

HS memory is described in Table 54 and Table 55.

Table 54. HS Memory Area

PARAMETER	DESCRIPTION
Address	100h-17Fh
Memory area	128 words
Data width	16-bit

Table 55. HS Number Start Address

HS NUMBER	1	2	3	4
Start address	100h	120h	140h	160h

Basic Functionality

Table 56 describes the HS basic functionality.

Table 56. HS Bit Function

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Delay		Toggle	Terminal			Pixel count									

BITS	NAME	DESCRIPTION	
15-14	DELAY	HS delay using two bits (0-3)	
13	TOGGLE	HS is set to high/low 0 = Low, 1 = High	
12-9	TERMINAL	HS pin using four bits (1-13)	
		TERMINAL NUMBER	**V**
		1	V0N
		13	V12N
8-0	PIXEL CNT	HS toggling pixel using nine bits (1-511)	

Instruction

Table 57 details the HS instruction.

Table 57. HS Instruction Bit Function

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
General instruction							Pixel count								

GENERAL INSTRUCTION	NAME	DESCRIPTION
111 0000b	Repeat	Reset HS pixel counter, pixel number = target cycle – 1

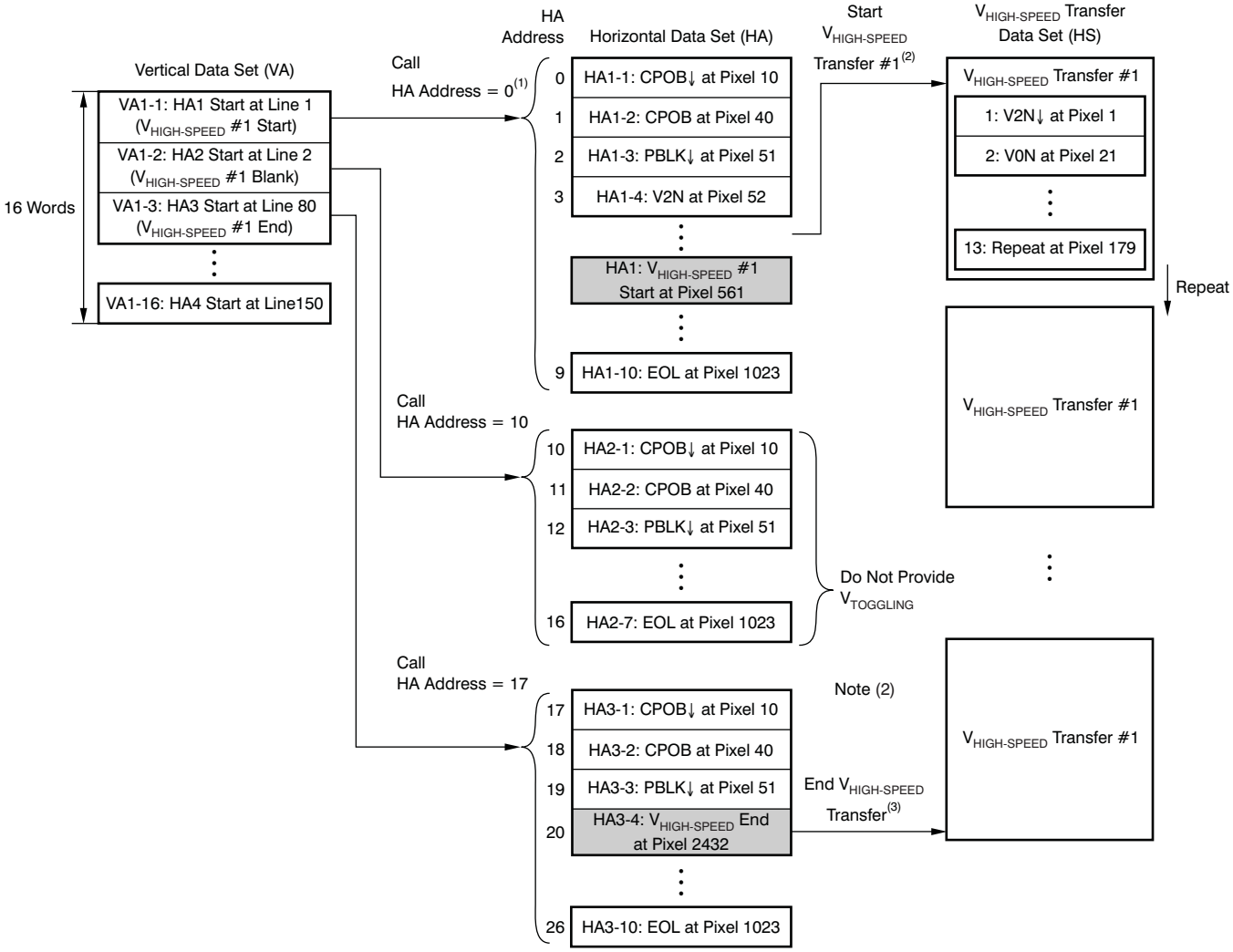
Programmed Operation Mode

The $V_{HIGH-SPEED}$ transfer function is used to clear the V_{CCD}. The HS pattern is supplied in the HS memory area. The pattern can be provided four types. HS start and stop timing is provided in the HA memory area. The operation continues until a decoding stop command of HA. $V_{TOGGLING}$ must not be provided under an HS operation.

1. Provide toggling information in HS memory.
2. Provide *HS start and stop* instruction in the HA memory with no $V_{TOGGLING}$ of HA.
3. Provide the above HA to the VA memory.

V_{CCD} Clear Example

Figure 43 shows an example of a programmable operation mode.



NOTE: Shaded cells indicate the area under discussion.

(1) The HA command block is called by a VA command.

(2) The HS loop sequence is started by an HA command at the selected pixel.

(3) The HS loop sequence is stopped by an HA command at the selected pixel.

(4) Line number, pixel number, and start of HA address are programmable.

Figure 43. Programmed Operation Mode Sequence

As shown in Table 58, $V_{HIGH-SPEED}$ toggling pixel address information is part of the HS memory. Input toggling points for one vertical transfer and one cycle address for repeat.

Table 58. V High-Speed Toggling Memory Example

MEMORY ADDRESS		DELAY [15:14]	SET [13]	TERMINAL ASSIGNMENT [12:9]	PIXEL COUNT [8:0]
FIXED	SEQUENTIAL				
01b	0000 0000b (HS 1-1)	00b	0	0011b	0 0000 0001b (1)
01b	0000 0001b (HS 1-2)	00b	1	0001b	0 0001 0101b (21)
01b	0000 0010b (HS 1-3)	01b	0	0100b	0 0010 1001b (41)
01b	0000 0011b (HS 1-4)	00b	1	0010b	0 0011 1101b (61)
—	—	—	—	—	—
01b	0000 0100b (HS 1-5)	11b	1	0000b (repeat)	0 1011 0011 (179)

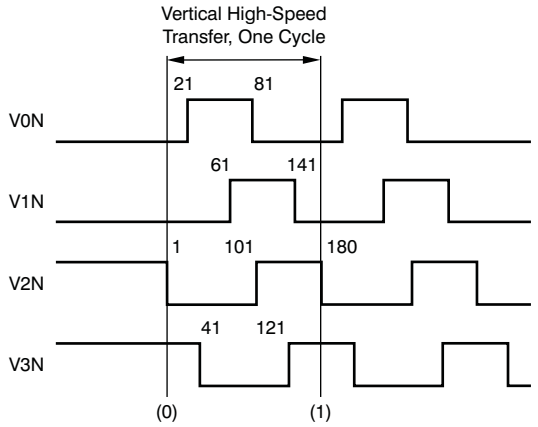


Figure 44. HS One Cycle Example

The HS start and stop command of HA is delayed by three pixel terms. Table 59 shows the delay.

Table 59. HA and HS Pixel Count

ITEM	LINE NUMBER	HA PIXEL COUNT	HS PIXEL COUNT
HA1 $V_{HIGH-SPEED}$ transfer start.	1	561	—
$V_{HIGH-SPEED}$ transfer counter start and V2 pulled low.	1	564	1
—	—	—	—
HA3 $V_{HIGH-SPEED}$ transfer stop.	80	2432	177
$V_{HIGH-SPEED}$ transfer cycle end.	80	2435	180

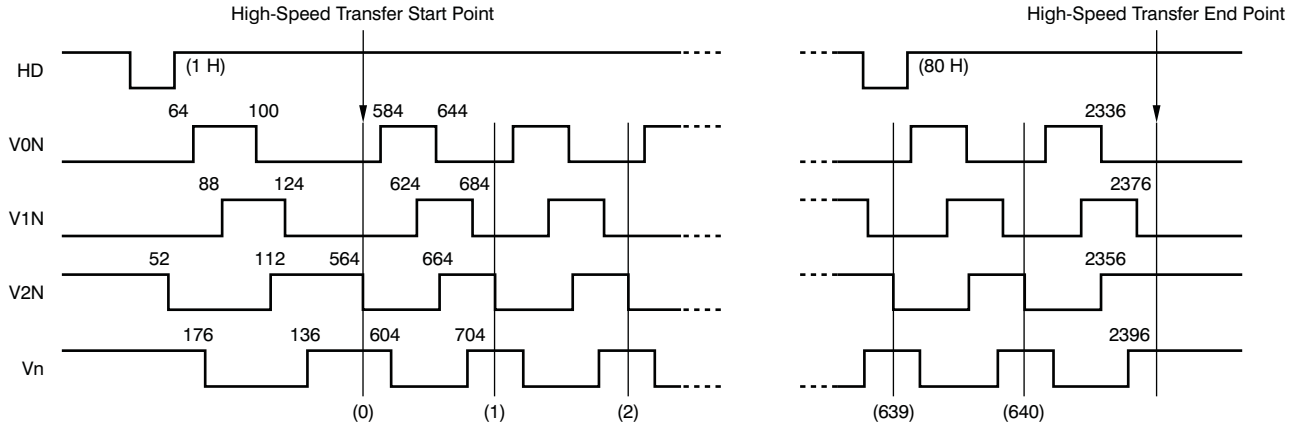
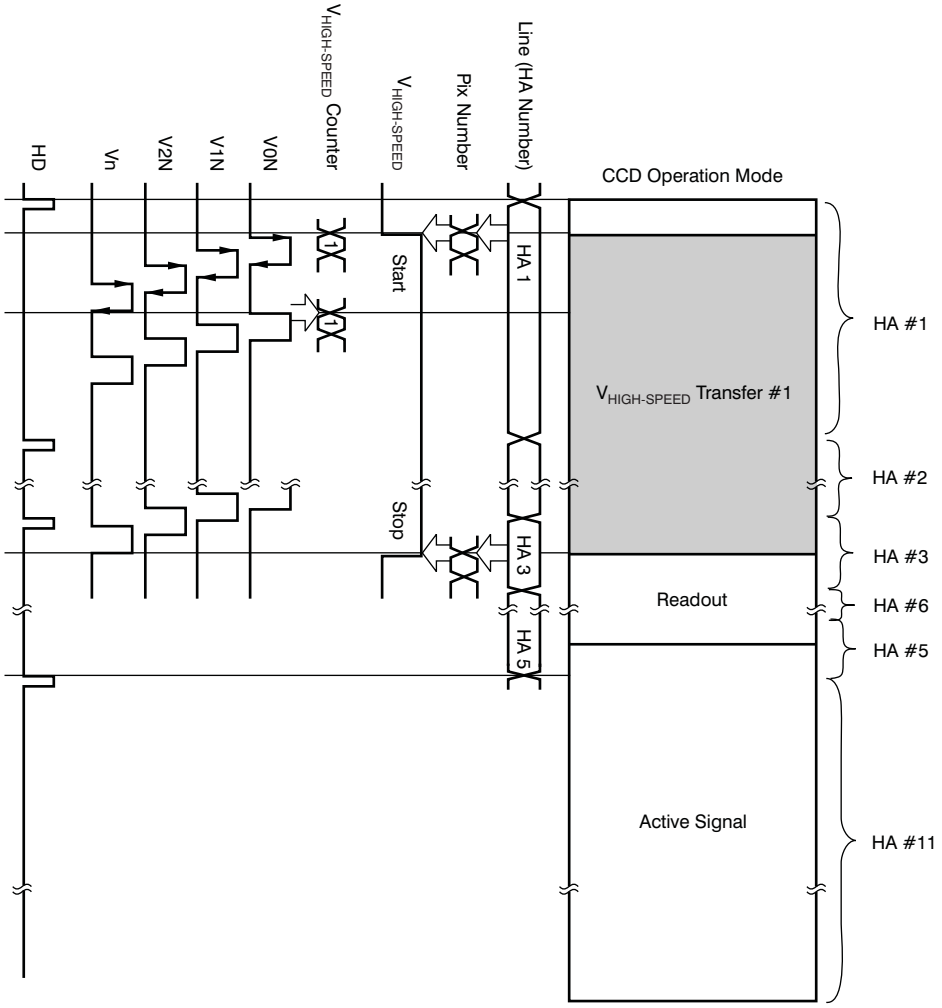


Figure 45. HS Timing Chart Example

Figure 46 shows the programmed operation mode for a still picture.

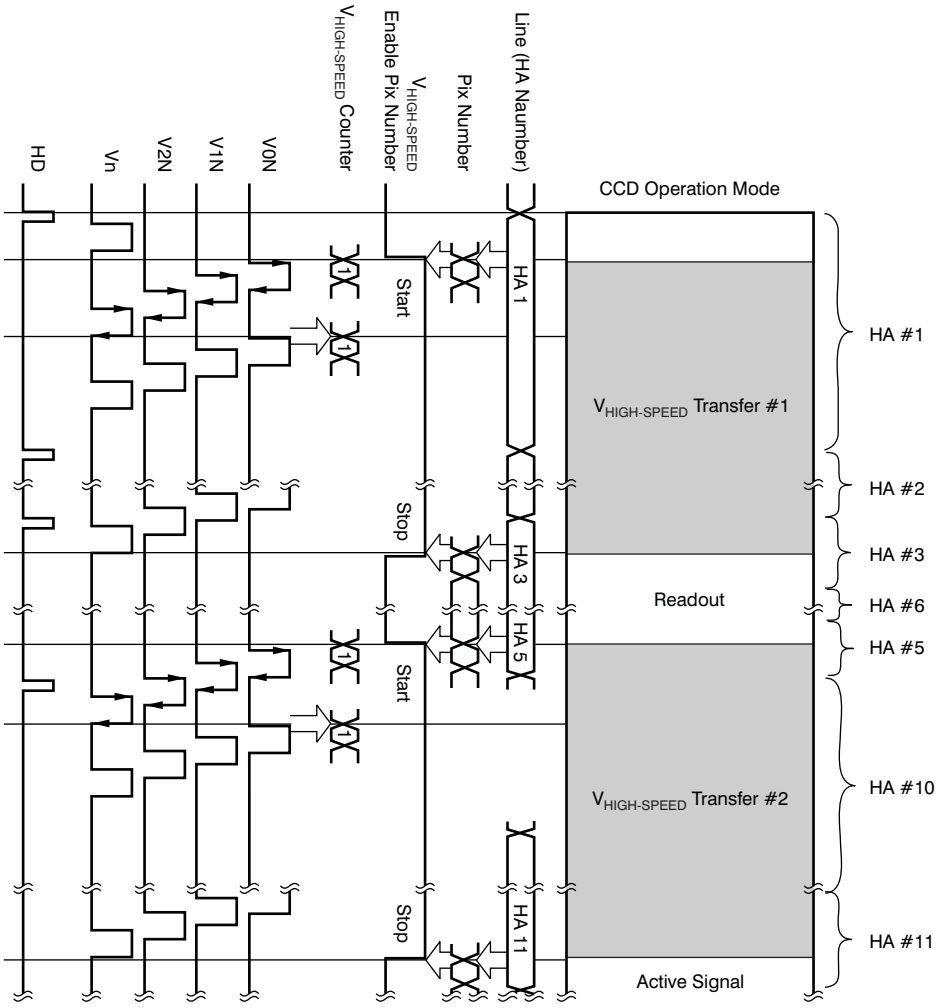


NOTE: Shaded cells indicate the area under discussion.

Figure 46. Programmed Operation Mode for A Still Picture

Example for Electrical Zoom

Figure 47 shows the programmed operation mode for an electric zoom function.



NOTE: Shaded cells indicate the area under discussion.

Figure 47. Programmed Operation Mode for An Electric Zoom Function

Register Dynamic Operation Mode

The HS changes for a specified number of lines. Specifically, the electric zoom requires a dynamic adjustment of the vertical transfer line number. In addition to the programmed operation mode, the HS enables/disables the line number memory and V_{EVENT} counter; the V_{EVENT} start/stop register enables the dynamic adjustment. HS enable/disable memory is included in the vertical memory area. A V_{EVENT} start command resets the V_{EVENT} counter (bit) at a specified line count.

Follow this recommended procedure to:

1. Select the V_{SIGNAL} for the event function. All $V_{SIGNALS}$ for a $V_{HIGH-SPEED}$ transfer must be enabled by a register setting, as shown in Table 60.
2. Select the V_{SIGNAL} for the event counter trigger. This signal counts up the event counter, as shown in Table 61. The last signal of the $V_{HIGH-SPEED}$ transfer is useful.
3. Provide toggling information in the HS memory.
4. Provide *HS start and stop* instruction in the HA memory. Refer to the *Horizontal Sequence* section for details.
5. Provide *Event* instruction in the VA memory. Refer to the *Vertical Sequence* section for details.
6. Set the event count value for an event start and stop, as shown in Table 62.

Table 60. V_{EVENT} Pin Register(1)

PARAMETER	REGISTER ADDRESS
V_{EVENT} pin	030h-032h

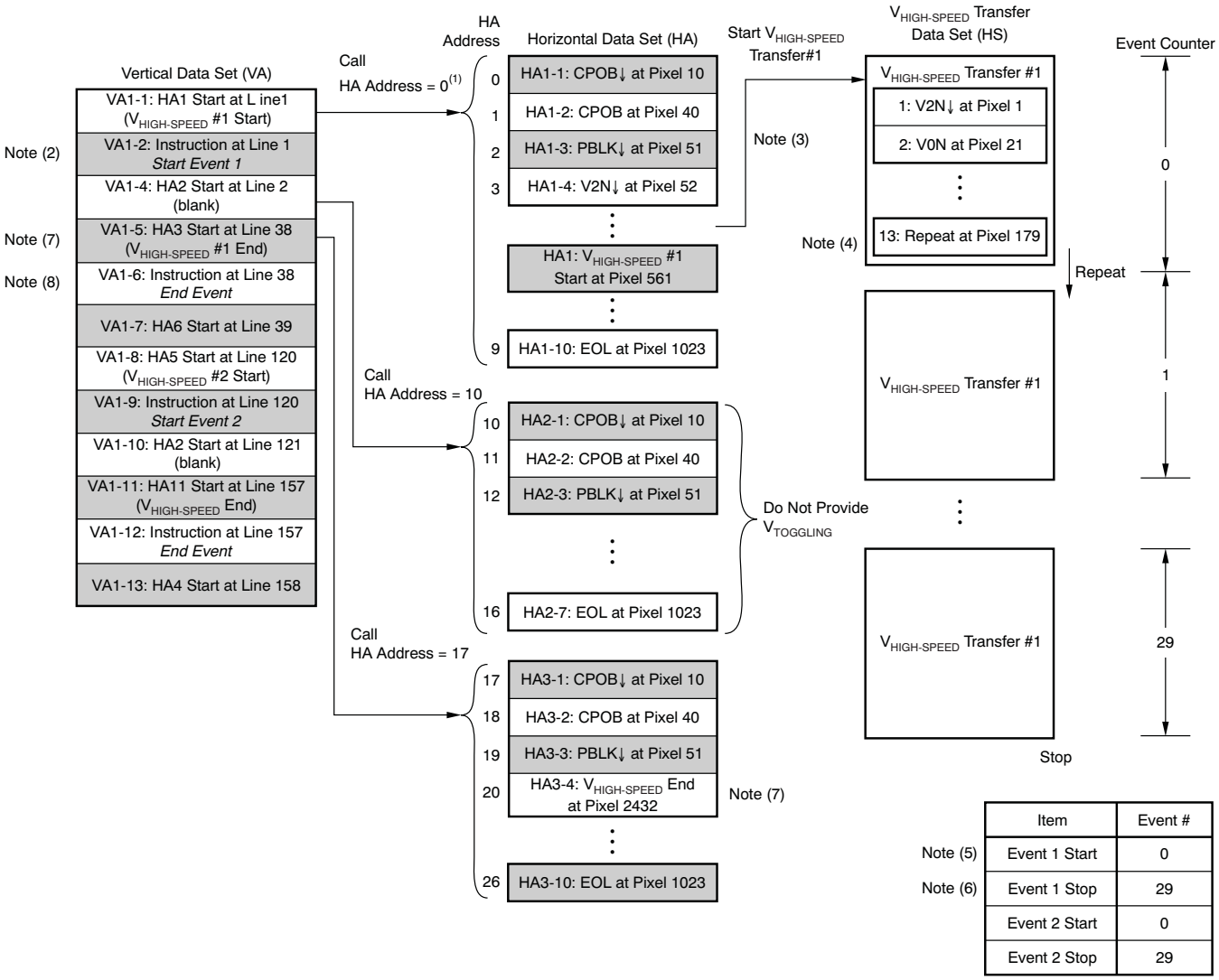
(1) Refer to the *Configuration Register* section for details.

Table 61. Event Counter Trigger Select Register

PARAMETER	REGISTER ADDRESS	DESCRIPTION
TRG pin	033h[4:0]	Terminal number (V0N-12N) Refer to the *Signal* section for details. Default = 00000b.
TRG edge	033h[5]	0 = Rising edge (default) 1 = Falling edge

Table 62. Event Start/Stop Register

PARAMETER		REGISTER ADDRESS
EVENT 1	Start	037h, 038h
	Stop	039h, 03Ah
EVENT 2	Start	03Bh, 03Ch
	Stop	03Dh, 03Eh



	Item	Event #
Note (5)	Event 1 Start	0
Note (6)	Event 1 Stop	29
	Event 2 Start	0
	Event 2 Stop	29

NOTE: Shaded cells indicate the area under discussion.

(1) The HA command block is called by the VA command.

(2) Event 1 is started by a VA command at same line number as that of note 1.

(3) The HS loop sequence is started by an HA command at the selected pixel number. However, the vertical signal does not output.

(4) The event counter is increased by one count a trigger vertical signal.

(5) When the event counter reaches the value of the *Event 1 Start* register, the vertical signal starts to output.

(6) When the event counter reaches the value of the *Event 1 Stop* register, the vertical signal stops outputting.

(7) The HS loop sequence is stopped by an HA command at the selected pixel number.

(8) The event is stopped by a VA command at the same line number as in note 7.

(9) Line number, pixel number, and start of the HA address are programmable. The operation of event 2 is the same as event 1.

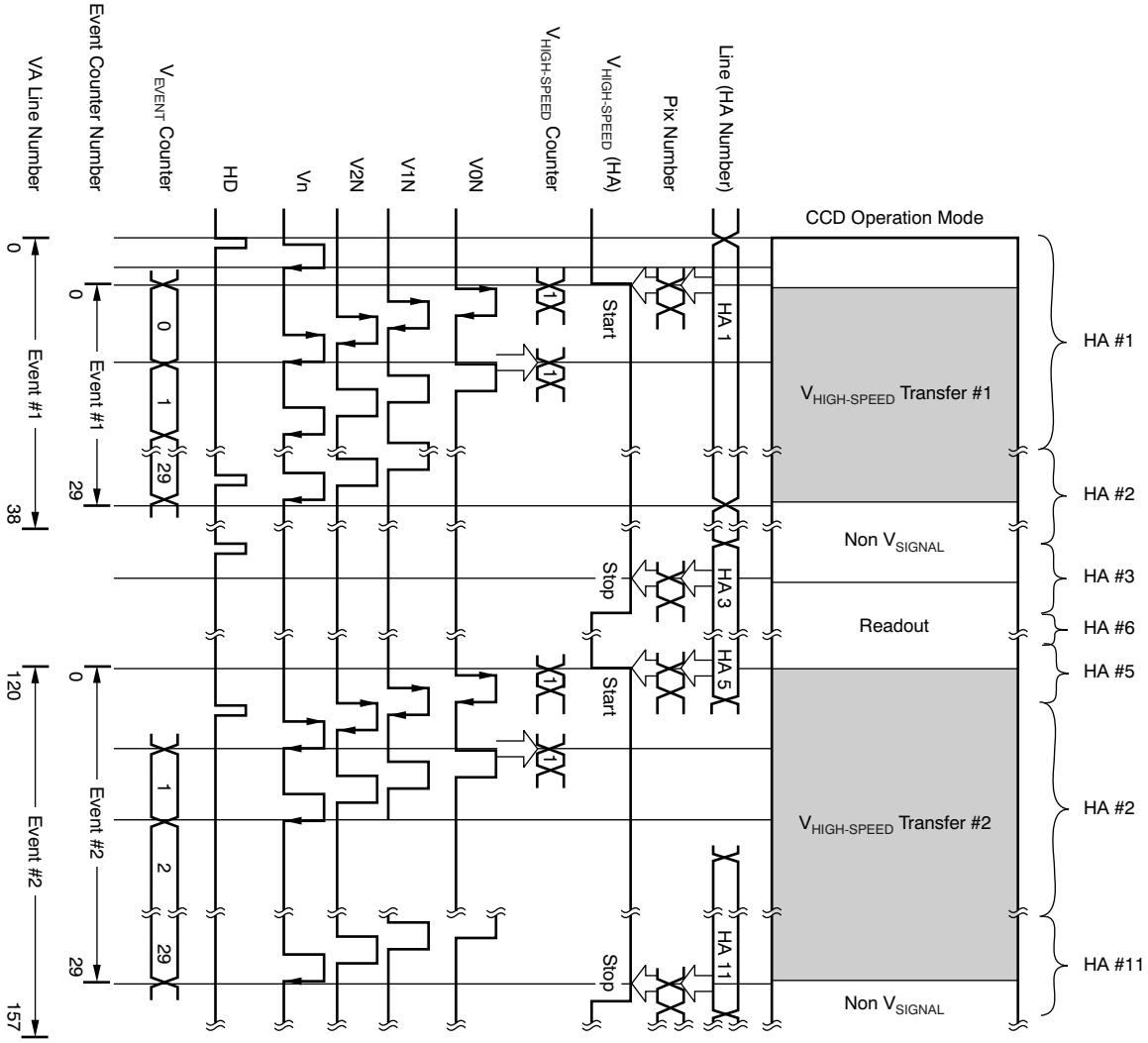
Figure 48. Register Dynamic Operation Mode Sequence

Table 63. Event Start/Stop(1)

PARAMETER	EVENT NUMBER
Event 1 start	0
Event 1 stop	29
Event 2 start	0
Event 2 stop	29

(1) The operation of Event 2 is the same as Event 1.

Vertical high-speed transfer has higher priority than any other vertical transfer instruction. Figure 49 shows the register dynamic operation mode for an electric zoom.



NOTE: Shaded cells indicate the area under discussion.

Figure 49. Register Dynamic Operation Mode for Electric Zoom Function

FRAME COUNT FUNCTION

The frame counter counts up by '1' for each VD update event. The frame counter range is from 1 to 63. This counter value is controlled by the following functions:

- SUBSW1 and SUBSW2 control
- MSHUT control
- Strobe control

A counter reset is accomplished by the following operation. The counter value is '1' after reset.

- VA instruction (Refer to the *Vertical Sequence* section for details.)
- TRIG (Refer to the *Trigger Function* section for details.)

If the counter value reaches the maximum value (63), the value can only be changed with a frame counter reset.

Table 64. Frame Counter Register

PARAMETER	REGISTER ADDRESS	DESCRIPTION
Frame Counter	022h[2]	0 = Disabled (default) 1 = Enabled

TG REGISTER UPDATE FUNCTION

Some registers of the TG section can be selected for update timing. Refer to the *Register Update* section of the *Common Section* for details.

PIXEL COUNTER PRESET

The preset value of the horizontal sequence pixel counter is set, as shown in Table 65.

Table 65. Pixel Counter Preset Register

PARAMETER	REGISTER ADDRESS	DESCRIPTION
Pixel Counter Preset	034h[3:0]	Slave = 6 (default) Master = 0 (recommend)

ELECTRIC SHUTTER FUNCTION

The electric shutter is operated by the SUBN pattern setting and SUBN pattern change setting.

SUBN Pattern Setting

The SUBN pattern has four types of toggling positions that are stored in the registers shown in Table 66. Patterns 2 and 3 enable fine pitch integration time control.

Table 66. SUBN Pattern Register(1)

PATTERN	REGISTER ADDRESS
Point 1 pixel number and polarity	08Ch-08Eh
Point 2 pixel number and polarity	08Fh-091h
Point 3 pixel number and polarity	092h-094h
Point 4 pixel number and polarity	095h-097h

(1) Refer to the *Configuration Register* section for details.

The SUBN pattern is specified by each point combination, as Table 67 shows.

Table 67. SUBN Pattern Description

PATTERN	DESCRIPTION
0	Non SUBN pulse
1	Operation of point 1 and point 2
2	Operation of point 3 and point 4
3	Operation of points 1 to 4

Table 68 describes an example SUBN pattern. Figure 50 shows a four-pattern example of an electric shutter.

Table 68. SUBN Pattern Example

TOGGLE POINT	PIXEL NUMBER	POLARITY
1	50	0
2	80	1
3	180	0
4	210	1

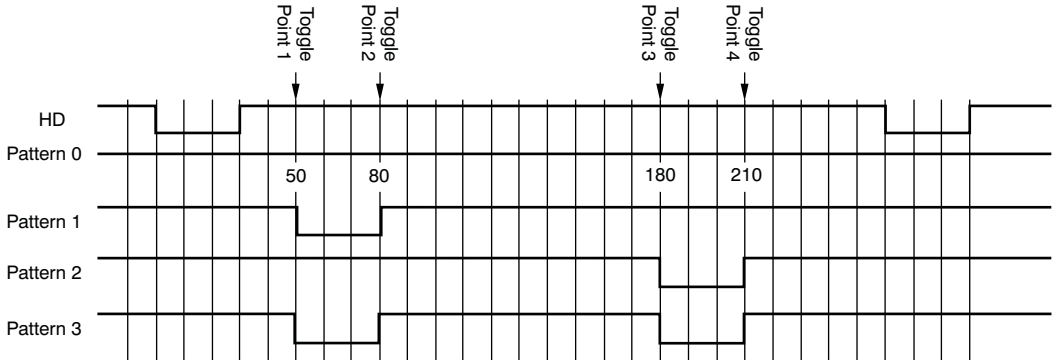


Figure 50. Electric Shutter Four-Pattern Example

SUBN Pattern Change

The electric shutter function has four sequential registers, as shown in Table 69. For each register, the SUBN pattern is assigned among four types of patterns and is selected at the pattern change point.

Table 69. SUBN Pattern Change(1)

PARAMETER	REGISTER ADDRESS
Pattern change point 1 line number and SUBN pattern number	098h-09Ah
Pattern change point 2 line number and SUBN pattern number	09Bh-09Dh
Pattern change point 3 line number and SUBN pattern number	09Eh-0A0h
Pattern change point 4 line number and SUBN pattern number	0A1h-0A3h

(1) Refer to the *Configuration Register* section for details.

Table 70 lists an electrical shutter example method with the register update function activated.

Table 70. Register Update Setting

PARAMETER	REGISTER ADDRESS	VALUE
TG Update	000h[3]	1 = VA Internal instruction (R_UPDATE)

This example method has three cases of exposure time within one frame cycle. Table 71 lists several electrical shutter parameters.

Table 71. Electrical Shutter Parameter

PARAMETER	LINE NUMBER	NOTE
SUBN operation term	A	Use with calculation of Table 72
Exposure time	B	
Read out	C	
1 frame cycle	D	
R_UPDATE	1	Should be provided at the VA internal instruction

Table 72. SUBN Start and End Line Number(1)

CASE	DESCRIPTION	LINE NUMBER		
		CONDITION	SUBN_START	SUBN_END
1	Line number 1 ≤ SUBN_Start < SUBN _End < Read_out	C – B – A ≥ 0	C – B – A	C – B
2	Line number 1 ≤ SUBN _End < Read_out < SUBN _Start	(C – B ≥ 0) and (C – B – A < 0)	D + (C – B – A)	C – B
3	Line number 1 < Read_out < SUBN _Start < SUBN _End	C – B < 0	D + (C – B – A)	D + (C – B)

(1) Line number ≠ Read_out, and Read_out ≠ SUBN _Start ≠ SUBN _End.

An actual value example is shown in Table 73.

Table 73. Example Parameter

PARAMETER	LINE NUMBER	VALUE
SUBN operation term	A	28
Read out	C	34
1 frame cycle	D	1259

Table 74. Example Parameter for Each Case(1)

CASE	DESCRIPTION	LINE NUMBER		
		INTEGRATION TIME	SUBN_START	SUBN_END
1	Line number 1 ≤ SUBN_Start < SUBN _End < Read_out	B = 2	C – B – A = 4	C – B = 32
2	Line number 1 ≤ SUBN _End < Read_out < SUBN _Start	B = 6	D + (C – B – A) = 1259	C – B = 28
3	Line number 1 < Read_out < SUBN _Start < SUBN _End	B = 1229	D + (C – B – A) = 36	D + (C – B) = 64

(1) Actual integration time is increased less than 1H by SUBN pattern three.

Case 1: Line Number 1 ≤ SUBN_Start < SUBN _End < Read_out

Table 75. Register Setting: Case 1

PATTERN CHANGE POINT	LINE NUMBER	SUBN PATTERN	NOTE
1	1	0 (non SUBN)	—
2	4	1	SUBN_Start
3	31	3	—
4	32	0 (non SUBN)	SUBN_End

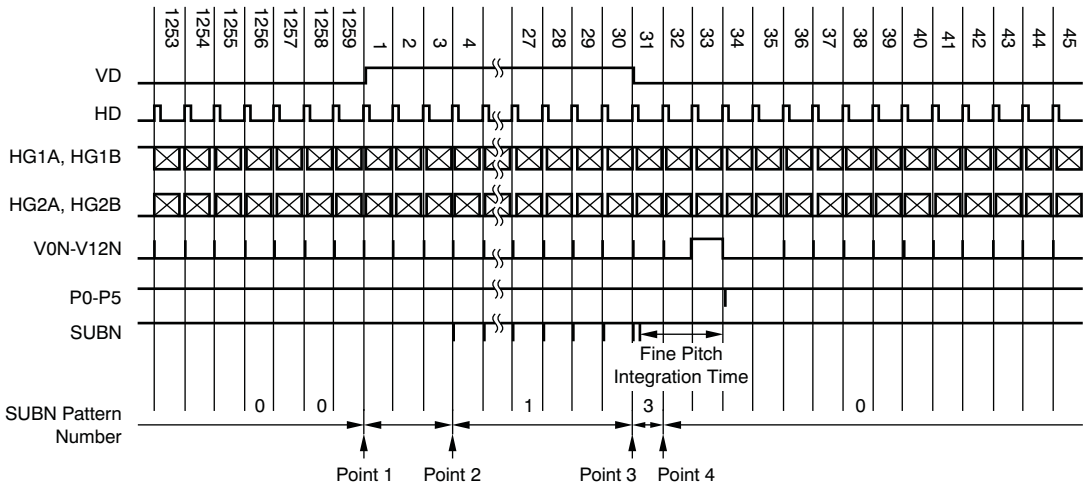


Figure 51. Electrical Shutter Timing: Case 1

Case 2: Line Number 1 ≤ SUBN_End < Read_out < SUBN _Start

Table 76. Register Setting: Case 2

PATTERN CHANGE POINT	LINE NUMBER	SUBN PATTERN	NOTE
1	1	1	—
2	27	3	—
3	28	0 (non SUBN)	SUBN_End
4	1259	1	SUBN_Start

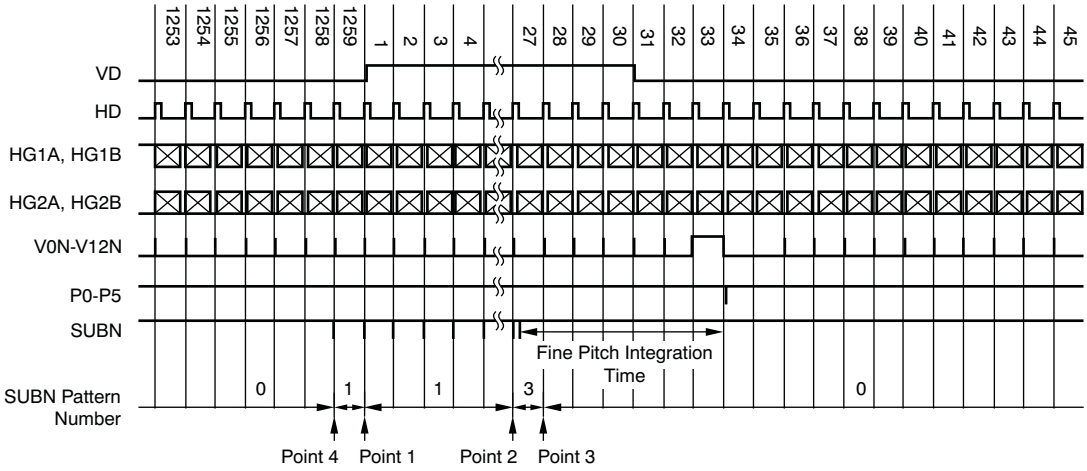


Figure 52. Electrical Shutter Timing: Case 2

Case 3: Line Number 1 < Read_out < SUBN_Start < SUBN _End

Table 77. Register Setting: Case 3

PATTERN CHANGE POINT	LINE NUMBER	SUBN PATTERN	NOTE
1	1	0 (non SUBN)	—
2	36	1	SUBN_Start
3	63	3	—
4	64	0 (non SUBN)	SUBN_End

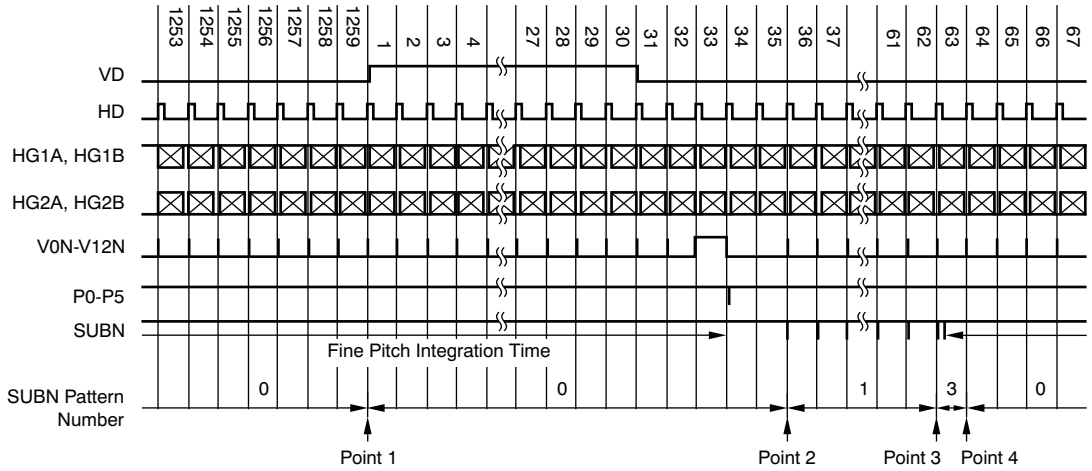


Figure 53. Electrical Shutter Timing: Case 3

SUBSW FUNCTION

The still mode uses an SUBSW1 and SUBSW2 function with two toggling registers for SUBSW1 and SUBSW2, respectively. The instruction consists of a frame number, line number, and polarity, as shown in Table 78.

Table 78. SUBSW Register(1)

PARAMETER			REGISTER ADDRESS
SUBSW1	Point 1	Line number	07Ch, 07Dh
		Frame number	07Eh
		Polarity	07Fh
	Point 2	Line number	080h, 081h
		Frame number	082h
		Polarity	083h
SUBSW2	Point 1	Line number	084h, 085h
		Frame number	086h
		Polarity	087h
	Point 2	Line number	088h, 089h
		Frame number	08Ah
		Polarity	08Bh

(1) Refer to the *Configuration Register* and *Frame Count Function* sections for details.

Table 79 and Figure 54 show an example SUBSW register and operation, respectively.

Table 79. SUBSW Register Example

PARAMETER			VALUE
SUBSW1	Point 1	Line number	1259
		Frame number	1
		Polarity	1
	Point 2	Line number	35
		Frame number	2
		Polarity	0

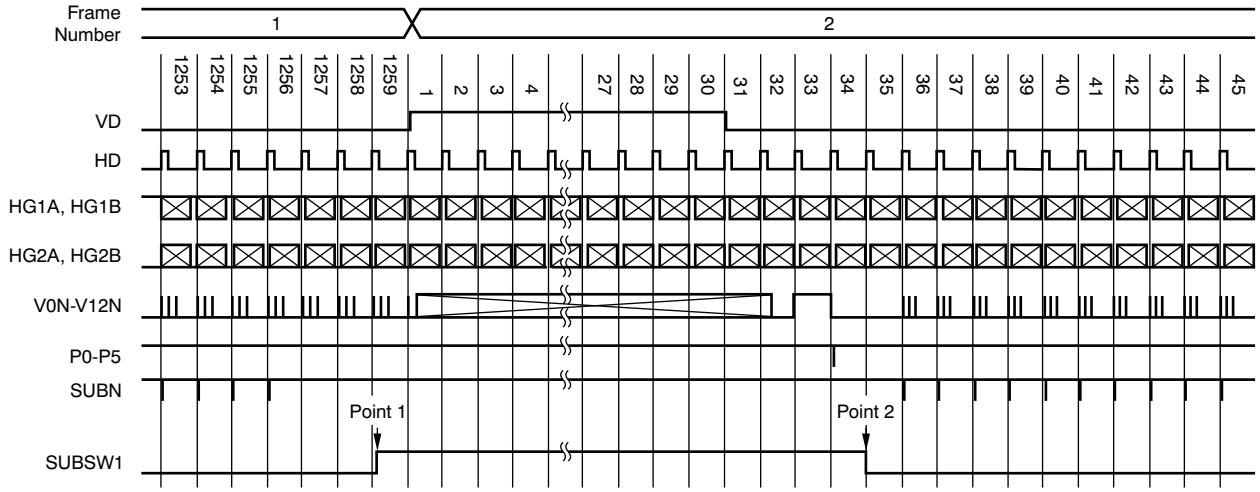


Figure 54. SUBSW Operation Example

MSHUT Function

The mechanical shutter function has a total of two words. The instruction consists of a frame number, line number, pixel number, and polarity, as shown in Table 80.

Table 80. MSHUT Register(1)

PARAMETER		REGISTER ADDRESS
Point 1	Pixel number, line number, frame number, and polarity	040h-045h
Point 2	Pixel number, line number, frame number, and polarity	046h-04Bh

(1) Refer to the *Configuration Register* and *Frame Count Function* sections for details.

Table 81 and Figure 55 show an example MSHUT register and operation, respectively.

Table 81. MSHUT Register Example

PARAMETER		VALUE
Point 1	Pixel number	900
	Line number	1253
	Frame number	1
	Polarity	1
Point 2	Pixel number	400
	Line number	1259
	Frame number	1
	Polarity	0

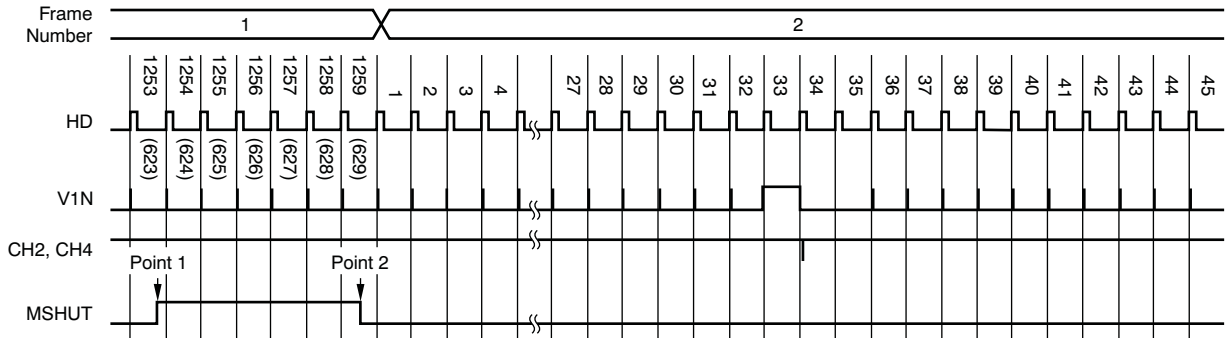


Figure 55. MSHUT Operation Example

STROBE FUNCTION

The strobe shutter function has eight words. The instruction consists of a frame number, line number, pixel number, and polarity, as shown in Table 82.

Table 82. Strobe Register(1)

PARAMETER		REGISTER ADDRESS
Point 1	Pixel number, line number, frame number, and polarity	04Ch-051h
Point 2	Pixel number, line number, frame number, and polarity	052h-057h
Point 3	Pixel number, line number, frame number, and polarity	058h-05Dh
Point 4	Pixel number, line number, frame number, and polarity	05Eh-063h
Point 5	Pixel number, line number, frame number, and polarity	064h-069h
Point 6	Pixel number, line number, frame number, and polarity	06Ah-06Fh
Point 7	Pixel number, line number, frame number, and polarity	070h-075h
Point 8	Pixel number, line number, frame number, and polarity	076h-07Bh

(1) Refer to the *Configuration Register* and *Frame Count Function* sections for details.

Table 83 and Figure 56 show an example strobe register and operation, respectively.

Table 83. Strobe Register Example

PARAMETER		VALUE
Point 1	Pixel number	200
	Line number	1257
	Frame number	1
	Polarity	1
Point 2	Pixel number	500
	Line number	1
	Frame number	2
	Polarity	0
Point 3	Pixel number	800
	Line number	4
	Frame number	2
	Polarity	1
Point 4	Pixel number	300
	Line number	31
	Frame number	2
	Polarity	0

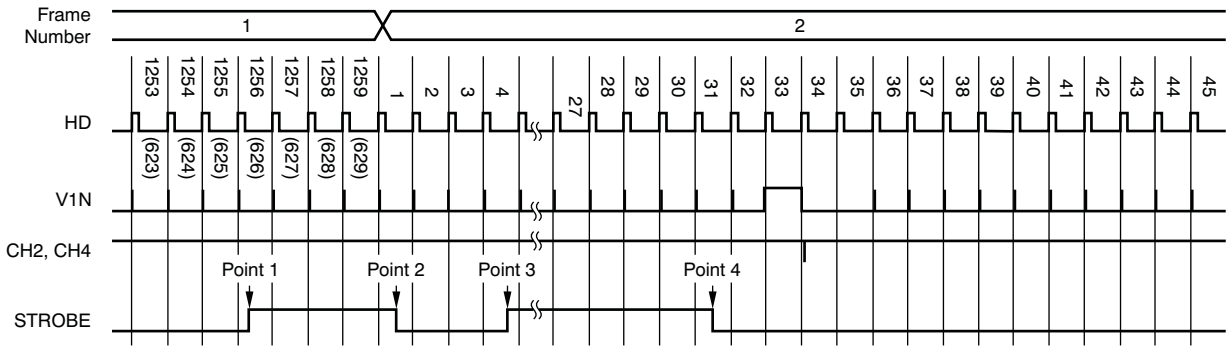


Figure 56. Strobe Operation Example

HBLK FUNCTION

The horizontal blank signal (HBLK) controls the H1, H2, and HL outputs. H1 and HL are high and H2 is low during blanking time. HBLK timing is provided by HA memory command. An example HBLK timing sequence is shown in Figure 57.

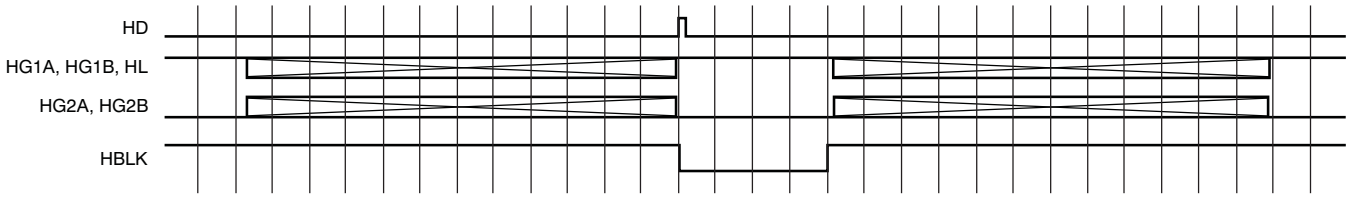


Figure 57. Horizontal Blanking Timing Example

HDIV FUNCTION

The motion picture CCD requires horizontal transfer during horizontal blanking. Select the horizontal transfer clock rate (divide H clock) from 2, 4, 6, 8, 10, or 12 by register (01Bh[2:0]). HDIV timing is provided by HA memory command. An example HDIV timing is shown in Figure 58.

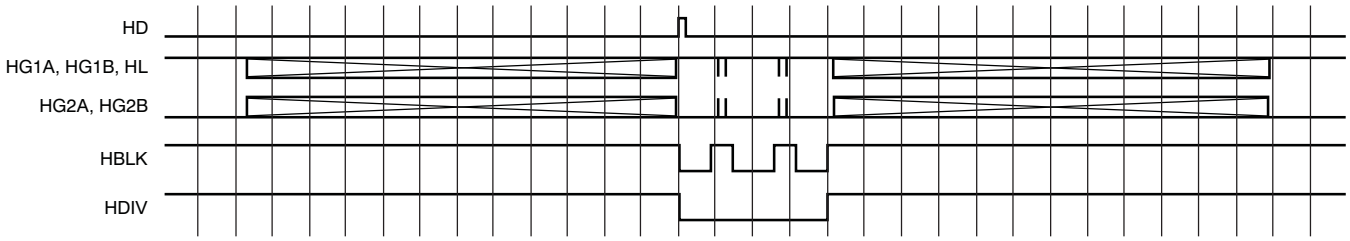


Figure 58. Motion Picture CCD Timing Example

SHP/SHD SKIPPING

An SHP and SHD skipping function is supported by VSP01M01 and VSP01M02. The skipping ratio is selected by the register, as shown in Table 84.

Table 84. SHP and SHD Skipping Register(1)

PARAMETER	REGISTER ADDRESS
SHP/SHD skipping	01Dh, 01Eh

(1) Refer to the *Configuration Register* section for details.

TRIGGER FUNCTION

Load TRIG Frame

The TRIG frame number is operated by the falling edge of the TRIG signal. The required register setting is shown in Table 85. For an example, refer to the *CCD Timing Composition* section.

Table 85. Load TRIG Frame Register Setting(1)

PARAMETER	REGISTER ADDRESS	VALUE
TRIG frame INCR	021h[2]	1 = Enabled
TRIG counter RST	021[3]	1 = Enabled
TRIG frame number	036h[5:3]	1-7

(1) Refer to the *Configuration Register* section for details.

TG Stop

TG is stopped by a TRIG signal polarity. The required register setting is shown in Table 86.

Table 86. TG Stop Register Setting(1)

PARAMETER	REGISTER ADDRESS	VALUE
MCK detect	020h[4]	0 = Disabled
TG CLK stop	021h[1]	1 = Enabled
TRIG POL	021h[0]	0 = High or 1 = Low

(1) Refer to the *Configuration Register* section for details.

Figure 59 shows a CCD timing composition example that operates the *Long Time Exposure by TRIG*. The falling edge of the TRIG (external trigger) signal reset line counter changes during the next frame. TG is stopped when the TRIG signal is high.

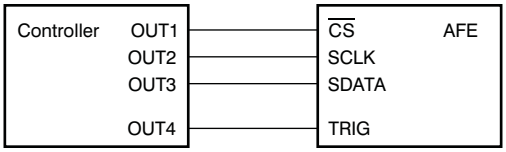
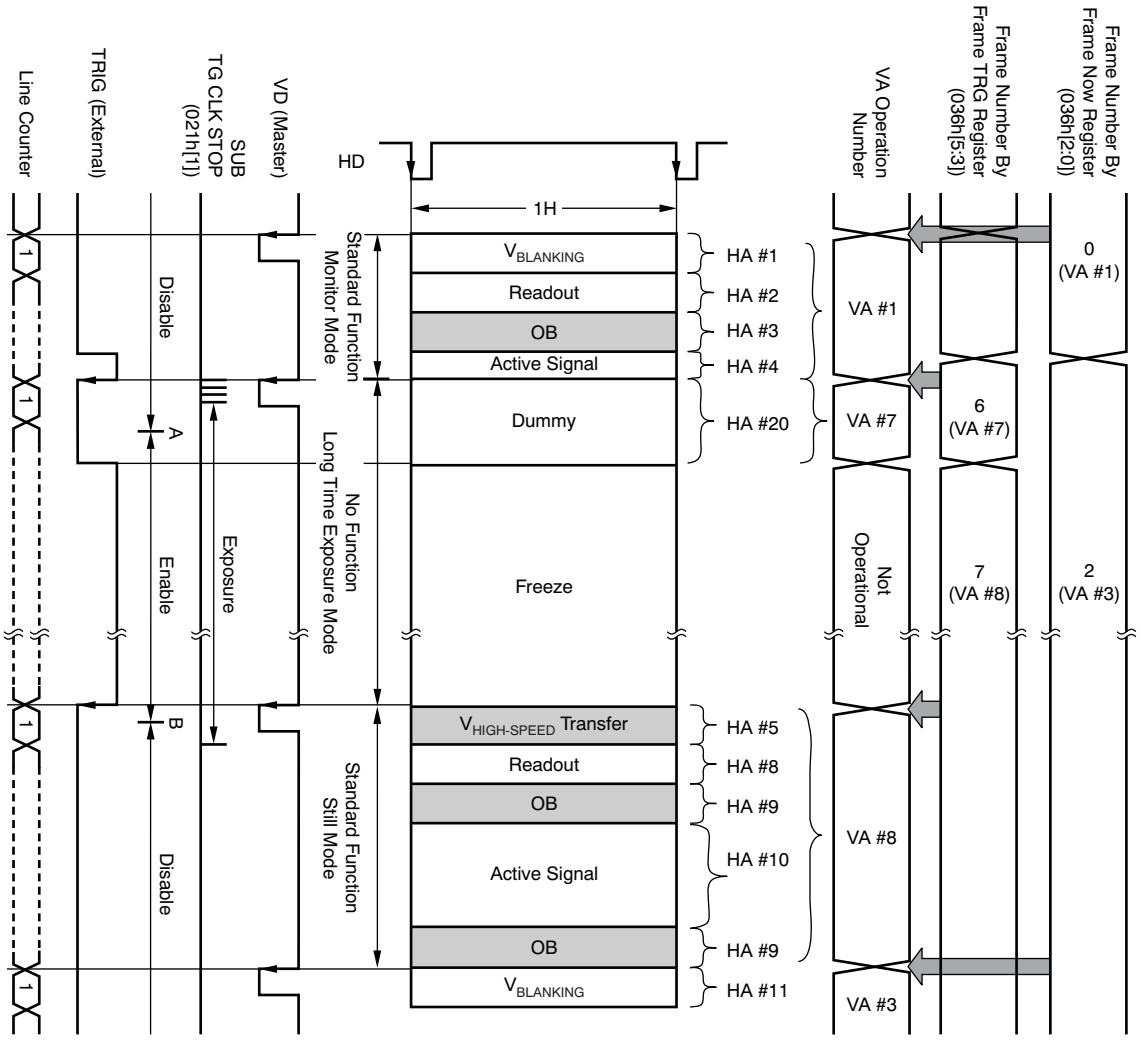


Figure 59. TRIG Signal Connection Example

Table 87. Long-Time Exposure by TRIG Example(1)

PARAMETER	REGISTER ADDRESS	VALUE
VD frame	022h[0]	1 = Enabled
TRIG frame INCR	021h[2]	1 = Enabled
TRIG counter RST	021h[3]	1 = Enabled
Static frame number	036h[2:0]	0 or 2
TRIG frame number	036h[5:3]	6 or 7
MCK detect	020h[4]	0 = Disabled
TG CLK stop	021h[1]	0 = Disabled 1 = Enabled (between A and B)
TRIG POL	021h[0]	0 = High

(1) Refer to the *Configuration Register* section for details.



NOTE: Shaded cells indicate the area under discussion.

Figure 60. Long-Time Exposure by TRIG Example

Frame Counter Reset

The frame counter is reset by the falling edge of the TRIG signal. The required register setting is shown in Table 88.

Table 88. Frame Counter Reset Register Setting(1)

PARAMETER	REGISTER ADDRESS	VALUE
Frame counter	022h[2]	1 = Enabled
Frame RST	021h[4]	1 = Enabled
TRIG counter RST	021h[3]	1 = Enabled

(1) Refer to the *Configuration Register* section for details.

V_{DRIVER} SECTION

Signal Connection and Truth Table

3-State Output

Table 89. 3-State Output

INPUT (TG OUTPUT)		OUTPUT (DEVICE PIN OUTPUT)
SIGNAL NAME		
VxN	Px	SIGNAL NAME
V1N	P1	
V3N	P2	
	P4	
V5N	P3	
	P5	
TRUTH TABLE		
VxN	Px	LEVEL
Low	Low	VH
	High	VM
High	Low	Hi-Z
	High	VL

2-State Output

Table 90. 2-State Output

INPUT (TG OUTPUT)	OUTPUT (DEVICE PIN OUTPUT)
SIGNAL NAME	
VxN	SIGNAL NAME
V2N	V2
V4N	V4
V6N	V6
TRUTH TABLE	
VxN	LEVEL
Low	VM
High	VL

SUB 2-State Output

Table 91. SUB 2-State Output

INPUT (TG OUTPUT)	OUTPUT (DEVICE PIN OUTPUT)
SIGNAL NAME	SIGNAL NAME
SUBN	SUB
TRUTH TABLE	
SUBN	LEVEL
Low	VH
High	VL

Output

Hi-Z = high impedance

VH = high level

VM = middle level

VL = low level

CONFIGURATION REGISTER

The 6-bit register area is described in Table 92. The addresses range from 000h to 0BFh.

Table 92. Register Section Overview

SECTION		REGISTER ADDRESS		UPDATE METHOD
		DEC	HEX	
Common	Update	0	000h	Real time
AFE	Standby	1	001h	Real Time, VD, or R_{LOAD} (selected by 000h[2:0])
	Data out	2	002h	
	S-delay	3	003h	
	OB clamp	4	004h	
	Hot-pixel rejection	5	005h	
	DPGA	6, 7	006h, 007h	
	CDS gain	8	008h	
	IDAC power	9	009h	
	DAC1 input	10, 11	00Ah, 00Bh	
	DAC2 input	12, 13	00Ch, 00Dh	
TG	High-speed timing	16-24	010h-018h	Real time
	ADCCK rise	25, 26	019h, 01Ah	
	HG1/HG2	27	01Bh	
	HG drive	28	01Ch	
	SHP/SHD pix skip	29, 30	01Dh, 01Eh	
	TG enable and sync	32	020h	
	TRG	33	021h	
	Frame field	34	022h	
	Pin enable	35-40	023h-028h	
	Pin initialize	41-46	029h-02Eh	VA initialization instruction
	ODD range	47	02Fh	Real time
	V_{EVENT} pin	48-51	030h-033h	
	Pixel counter	52	034h	
	Field	53	035h	
	Frame	54	036h	VD or F_{LOAD} (selected by 022h[1:0])
				TRIG is input when h021h[2] is enabled
	V_{EVENT}	55-62	037h-03Eh	Real Time or R_Update (selected by 000h[3])
	Mech shut	64-75	040h-04Bh	
	Strobe	76-123	04Ch-07Bh	
	SUBSW1	124-131	07Ch-083h	
	SUBSW2	132-139	084h-08Bh	
	SUBN	140-151	08Ch-097h	
	SUBN CHG	152-163	098h-0A3h	
	Monitor pin select	181	0B5h	

Table 93. Detailed Common Section

SECTION	ADDRESS		PARAMETER			DESCRIPTION		UPDATE METHOD
	DEC	HEX	BITS	PARAMETER	# OF BITS	DESCRIPTION	VALUE	
Update	0	—	—	—	—	—	0 = Real time 1 = External trigger (R_{LOAD} pin or VD)	Real time
			[2:1]	AFE UP POL	2	AFE register update signal and polarity	00b = R_{LOAD} input rising edge (default) 01b = R_{LOAD} input falling edge 10b = VD rising edge 11b = VD falling edge	
			[3]	TG update	1	TG register update timing	0 = Real time 1 = VA internal instruction (R_UPDATE) (default)	
			[5:4]	—	2	—	Reserved Default = 00b	

Table 94. Detailed AFE Section

SECTION	ADDRESS		PARAMETER			DESCRIPTION				UPDATE METHOD
	DEC	HEX	BITS	PARAMETER	# OF BITS	DESCRIPTION	VALUE			
Standby	1	1	[0]	AFE standby	1	AFE standby	0 = AFE functions normally (default) 1 = AFE standby			Real time, VD, or R_{LOAD} (selected by 000h[2:0])
			[1]	8-bit DAC1 standby	1	Independent 8-bit DAC1 standby	0 = Enabled 1 = Standby (default)			
			[2]	8-bit DAC2 standby	1	Independent 8-bit DAC2 standby				
			[3]	Monitor pin	1	Monitor pin enable	0 = Disabled (default) 1 = Enabled			
			[5:4]	—	2	—	Reserved Default = 00b			
Data out	2	2	[1:0]	Data out delay	2	Data out delay	00b = 0 ns (default) 01b = 2 ns 10b = 4 ns 11b = 6 ns			Real time, VD, or R_{LOAD} (selected by 000h[2:0])
			[2]	$\overline{OE}$	1	Data output enable	0 = Enabled (default) 1 = Disabled (high impedance)			
			[5:3]	—	3	—	Reserved Default = 000b			
S-DELAY	3	3	[1:0]	←	2	Sampling delay for SHP/SHD internal delay circuit	00b = 0 ns (default) 01b = 2 ns 10b = 4 ns 11b = 6 ns			Real time, VD, or R_{LOAD} (selected by 000h[2:0])
			[5:2]	—	4	—	Reserved Default = 0000b			
OB clamp	4	4	[4:0]	←	5	OB clamp level	**DATA**	**(DEC)**	**12-BIT**	**10-BIT**	Real time, VD, or R_{LOAD} (selected by 000h[2:0])
							00000b	(0)	64	16	
							00001b	(1)	72	18	
							—	—	—	—	
							00110b	(6)	112	28	
							00111b	(7)	120	30	
							01000b	(8)	128	32 (default)	
							01001b	(9)	136	34	
							—	—	—	—	
							01110b	(14)	176	44	
							01111b	(15)	184	46	
							—	—	—	—	
							11110b	(30)	304	76	
							11111b	(31)	312	78	
							Step	—	8	2	
			[5]	—	1	—	Reserved Default = 0				
Hot-pixel rejection	5	5	[4:0]	HOT PIX LEVEL	5	Hot-pixel rejection level	R_L (LSB) = 16 × (code[4:0] + 1) (R_L is the difference from OB level of 10-bit equivalent)				Real time, VD, or R_{LOAD} (selected by 000h[2:0])
			[5]	HOT PIX EN	1	Hot-pixel rejection enable/disable	0 = Disabled (default) 1 = Enabled				

Table 94. Detailed AFE Section (continued)

SECTION	ADDRESS		PARAMETER				DESCRIPTION				UPDATE METHOD
	DEC	HEX	BITS	PARAMETER		# OF BITS	DESCRIPTION	VALUE			
DPGA	6	6	[5:0]	LSB	←	10	Digital programmable gain	DATA	(DEC)	GAIN	Real time, VD, or R_{LOAD} (selected by 000h[2:0])
	7	7	[3:0]	MSB				00 0000 0000b — 00 1100 0000b — 11 1111 1111b	(0) — (192) — (1023)	–6 dB — 0 dB (default) — 26 dB	
								Gain (dB) = data × 0.03125(dB/step) – 60.03125 dB/step			
			[5:4]	—		2	—	Reserved Default = 00b			
CDS gain	8	8	[2:0]	←		3	Analog programmable gain	000b = 0 dB (default) 001b = 6 dB 010b = 12 dB 011b = 18 dB 111b = –3 dB			Real time, VD, or R_{LOAD} (selected by 000h[2:0])
			[5:3]	—		3	—	Reserved Default = 000b			
IDAC power	9	9	[1:0]	←		2	IDAC output current	00b = ×1 (default) 01b = ×2 10b = ×4 11b = ×8			Real time, VD, or R_{LOAD} (selected by 000h[2:0])
			[5:2]	—		4	—	Reserved Default = 0000b			
DAC1 input	10	A	[5:0]	LSB	←	8	Independent DAC1 input code	DATA	OUT (V)		Real time, VD, or R_{LOAD} (selected by 000h[2:0])
								0000 0000b — 1111 1111b	0.1 — 2.9		
	11	B	[1:0]	MSB				Out (V) = 0.01094 × data + 0.1 Default = 0 (DEC)			
			[5:2]	—		4	—	Reserved Default = 0000b			
DAC2 input	12	C	[5:0]	LSB	←	8	Independent DAC2 input code	DATA	OUT (V)		Real time, VD, or R_{LOAD} (selected by 000h[2:0])
								0000 0000b — 1111 1111b	0.1 — 2.9		
	13	D	[1:0]	MSB				Out (V) = 0.01094 × data + 0.1 Default = 0 (DEC)			
			[5:2]	—		4	—	Reserved Default = 0000b			
—	14	E	[5:0]	—		6	—	Reserved Default = 0 (DEC)			Real time, VD, or R_{LOAD} (selected by 000h[2:0])
—	15	F	[5:0]	—		6	—	Reserved Default = 0 (DEC)			Real time, VD, or R_{LOAD} (selected by 000h[2:0])

Table 95. Detailed TG Section

SECTION	ADDRESS		PARAMETER			DESCRIPTION				UPDATE METHOD
	DEC	HEX	BITS	PARAMETER	# OF BITS	DESCRIPTION	VALUE			
High-speed timing	16	10	[4:0]	HG1 rising	5	HG1A, HG1B, HL rising edge				Real time
			[5]	—	1	Reserved				
	17	11	[4:0]	HG1 falling	5	HG1A, HG1B, HL falling edge				
			[5]	—	1	Reserved				
	18	12	[4:0]	HG2 falling	5	HG2A, HG2B, falling edge	DATA	(DEC)	STEP	
			[5]	—	1	Reserved	10000b 10001b — 11111b 00000b 00001b — 01110b 01111b	(16) (17) — (31) (0) (default) (1) — (14) (15)	–16 –15 — –1 0 (default) 1 — 14 15	
	19	13	[4:0]	HG2 rising	5	HG2A, HG2B, rising edge				
			[5]	—	1	Reserved				
	20	14	[4:0]	RG falling	5	RG falling edge				
			[5]	—	1	Reserved				
	21	15	[4:0]	SHP falling	5	SHP falling edge				
			[5]	—	1	Reserved				
	22	16	[4:0]	SHP rising	5	SHP rising edge				
			[5]	—	1	Reserved				
	23	17	[4:0]	SHD falling	5	SHD falling edge	Step is twos complement of data. 1 step = (1 pixel clock term)/100.			
			[5]	—	1	Reserved				
	24	18	[5:0]	SHD rising	5	SHD rising edge				
			[0]	—	1	Reserved				
ADCCK delay	25	19	[5:0]	LSB	7	ADCCK delay	Data[6:0] = 01Ah[0] × 26 + 019h[5:0]			Real time
	26	1A	[0]	MSB ←			01Ah[0]	019h[5:0]	(DEC)	STEP
							1 — 1 1 1 — 1 0 0 — 0 0 0 — 0	00 0000b — 00 1101b 00 1110b 00 1111b — 11 1111b 00 0000b 00 0001b — 11 0000b 11 0001b 11 0010b — 11 1111b	(64) — (77) (78) (79) — (127) (0) (default) (1) — (48) (49) (50) — (63)	Reserved — Reserved –50 –49 — –1 0 (default) 1 — 48 49 Reserved — Reserved
							Step is twos complement of data. 1 step = (1 pixel clock term)/100.			
			[5:1]	—	5	Reserved	Reserved Default = 0 (DEC)			
HG1/HG2	27	1B	[2:0]	DIV	3	High-speed pulse divide rate	000b = Divide by 16 (default) 001b = Divide by 2 — 111b = Divide by 14			Real time
			[3]	Enable	1	HG1A, HG2A, HG1B, HG2B, HL enable/standby	0 = Enabled (default) 1 = Standby			
			[4]	HG1 POL	1	HG1A, HG1B, HL polarity during a TG standby condition	0 = High (default) 1 = Low			
			[5]	—	1	Reserved	Reserved Default = 0			

Table 95. Detailed TG Section (continued)

SECTION	ADDRESS		PARAMETER			DESCRIPTION			UPDATE METHOD
	DEC	HEX	BITS	PARAMETER	# OF BITS	DESCRIPTION	VALUE		
HG drive	28	1C	[1:0]	H current	2	H1, H2 output drive current	00b = Minimum 01b = Default (default) 10b = Mid-range 11b = Maximum		Real time
			[2]	HGB enable	1	HG1B, HG2B enable/disable	0 = Disabled (Z) (default) 1 = Enabled		
			[5:3]	—	3	Reserved	Reserved Default = 011b		
SHP/SHD PIX SKIP	29	1D	[2:0]	Ratio	3	RG, SHP, SHD pixel skipping ratio	**DATA** 000b (default) 001b 010b 011b 100b 101b 110b 111b	**RATIO** No skip 2 pixels 3 pixels 4 pixels 5 pixels 6 pixels 7 pixels 8 pixels	Real time
			[5:3]	Start	3	RG, SHP, SHD pixel skipping start point. Count from HD edge	Pixel number Default = 000b		
	30	1E	[0]	CLPDM	1	RG, SHP, SHD pixel skipping when CLPDM is active	0 = Continue 1 = Stop (default)		
			[1]	CLPOB	1	RG, SHP, SHD pixel skipping when CLPOB is active			
			[5:2]	—	4	Reserved	Reserved Default = 0000b		
—	31	1F	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)		Real time
TG enable and sync	32	20	[0]	TG enable	1	TG function enable/disable	0 = TG function disabled (standby) (default) 1 = TG function enabled		Real time
			[1]	Master/slave	1	Master/slave mode	0 = Slave mode (HD, VD input) (default) 1 = Master mode (HD, VD output)		
			[2]	VH, HD, MCK edge	1	VD, HD signal latch by MCK	0 = MCK rising edge (default) 1 = MCK falling edge		
			[3]	VD, HD, TRG edge	1	VD, HD signal trigger	0 = Falling edge (default) 1 = Rising edge		
			[4]	MCK detect	1	Detect MCK stop and set output default	0 = Disabled 1 = Enabled (default)		
			[5]	—	1	Reserved	Reserved Default = 0		
TRG	33	21	[0]	POL	1	Trigger polarity for TG CLK STOP (021h[1])	0 = Active high (default) 1 = Active low		Real time
			[1]	CLK stop	1	Trigger state (021h[0]) stops MCK for TG circuit (020h[4] does not work)	0 = Disabled (default) 1 = Enabled		
			[2]	Frame INC	1	Trigger falling edge sets the frame (defined by 036h[5:3]) when this bit is enabled			
			[3]	Counter RST	1	Trigger falling edge resets the line and pixel counter			
			[4]	Frame RST	1	Trigger falling edge resets the frame counter when 021h[3] = 1			
			[5]	—	1	Reserved	Reserved Default = 0		

Table 95. Detailed TG Section (continued)

SECTION	ADDRESS		PARAMETER			DESCRIPTION		UPDATE METHOD
	DEC	HEX	BITS	PARAMETER	# OF BITS	DESCRIPTION	VALUE	
Frame field	34	22	[0]	VD	1	Restart frame by VD	0 = Disabled 1 = Enabled (default)	Real time
			[1]	F_{LOAD}	1	Restart frame by F_{LOAD} of VA	0 = Disabled (default) 1 = Enabled	
			[2]	Frame, CNT, RST	1	Reset and start frame counter	0 = Disabled (default) 1 = Enabled	
			[3]	Field SET	1	Field setting selection	0 = VD/HD phase (default) 1 = Register setting	
			[4]	Field POL	1	Field polarity	0 = Low when ODD (default) 1 = High when EVEN	
			[5]	VD Even	1	VD edge trigger in EVEN field	0 = Disabled (default) 1 = Enabled	
Pin enable	35	23	[0]	V0N	1	Pin enable selection	0 = Disabled (default) 1 = Enabled	Real time
			[1]	V1N	1			
			[2]	V2N	1			
			[3]	V3N	1			
			[4]	V4N	1			
			[5]	V5N	1			
	36	24	[0]	V6N	1	Pin enable selection	0 = Disabled (default) 1 = Enabled	
			[1]	V7N	1			
			[2]	V8N	1			
			[3]	V9N	1			
			[4]	V10N	1			
			[5]	V11N	1			
	37	25	[0]	V12N	1	Pin enable selection	0 = Disabled (default) 1 = Enabled	
			[1]	—	1			
			[2]	—	1			
			[3]	P0	1			
			[4]	P1	1			
			[5]	P2	1			
	38	26	[0]	P3	1	Pin enable selection	0 = Disabled (default) 1 = Enabled	
			[1]	P4	1			
			[2]	P5	1			
			[3]	—	1			
			[4]	—	1			
			[5]	CLPDM	1			
	39	27	[0]	CLPOB	1	Pin enable selection	0 = Disabled (default) 1 = Enabled	Real time
			[1]	PBLK	1			
			[2]	HBLK	1			
			[3]	HDIV	1			
			[4]	VD	1			
			[5]	HD	1			
	40	28	[0]	Field	1	Pin enable selection	0 = Disabled (default) 1 = Enabled	
			[1]	SUBN	1			
			[2]	Strobe	1			
			[3]	MSHUT	1			
			[4]	SUBSW1	1			
			[5]	SUBSW2	1			

Table 95. Detailed TG Section (continued)

SECTION	ADDRESS		PARAMETER			DESCRIPTION		UPDATE METHOD
	DEC	HEX	BITS	PARAMETER	# OF BITS	DESCRIPTION	VALUE	
Pin initialization	41	29	[0]	V0N	1	Pin initialization polarity	0 = Low 1 = High (default)	VA initialization instruction
			[1]	V1N	1			
			[2]	V2N	1			
			[3]	V3N	1			
			[4]	V4N	1			
			[5]	V5N	1			
	42	2A	[0]	V6N	1			
			[1]	V7N	1			
			[2]	V8N	1			
			[3]	V9N	1			
			[4]	V10N	1			
			[5]	V11N	1			
	43	2B	[0]	V12N	1			
			[1]	—	1			
			[2]	—	1			
			[3]	P0	1			
			[4]	P1	1			
			[5]	P2	1			
	44	2C	[0]	P3	1			
			[1]	P4	1			
			[2]	P5	1			
			[3]	—	1			
			[4]	—	1			
			[5]	CLPDM	1	Pin initialization polarity	0 = Low (default) 1 = High	
	45	2D	[0]	CLPOB	1			
			[1]	PBLK	1			
			[2]	HBLK	1			
			[3]	HDIV	1			
			[4]	VD	1			
			[5]	HD	1			
	46	2E	[0]	Field	1			
			[1]	SUBN	1	Pin initialization polarity	0 = Low 1 = High (default)	
			[2]	Strobe	1	Pin initialization polarity	0 = Low (default) 1 = High	
			[3]	MSHUT	1			
			[4]	SUBSW1	1			
			[5]	SUBSW2	1			
ODD range	47	2F	[2:0]	ODD HD-VD	3	HD-VD delay for ODD detection	0-7 pixel delay Default = 001b	Real time
			[5:3]	ODD VD-HD	3	VD-HD delay for ODD detection	0-8 pixel delay Default = 001b	

Table 95. Detailed TG Section (continued)

SECTION	ADDRESS		PARAMETER			DESCRIPTION		UPDATE METHOD
	DEC	HEX	BITS	PARAMETER	# OF BITS	DESCRIPTION	VALUE	
V_{EVENT} pin	48	30	[0]	V0N	1	Pin used for vertical event control	0 = Disabled (default) 1 = Enabled	Real time
			[1]	V1N	1			
			[2]	V2N	1			
			[3]	V3N	1			
			[4]	V4N	1			
			[5]	V5N	1			
	49	31	[0]	V6N	1			
			[1]	V7N	1			
			[2]	V8N	1			
			[3]	V9N	1			
			[4]	V10N	1			
			[5]	V11N	1			
V_{EVENT} pin	50	32	[0]	V12N	1	Pin used for vertical event control	0 = Disabled (default) 1 = Enabled	Real time
			[1]	—	1			
			[2]	—	1			
			[5:3]	—	3	Reserved	Reserved Default = 000b	
	51	33	[4:0]	TRG pin	5	Vertical event trigger pin	Terminal number. Refer to the *Signal* section for details. Default = 0 (DEC)	
			[5]	TRG edge	1	Vertical event trigger	0 = Rising edge (default) 1 = Falling edge	
Pixel counter	52	34	[3:0]	Pixel count	4	Pin counter start offset	Pixel number. Slave mode = 0110 (default) Master mode = 0	Real time
			[5:4]	—	2	Reserved	Reserved Default = 00b	
Field	53	35	[0]	ODD/EVEN	1	Field index	0 = ODD (default) 1 = EVEN	Real time
			[5:1]	—	5	Reserved	Reserved Default = 0 (DEC)	
Frame	54	36	[2:0]	Frame now	3	Set current frame number	Frame number. Default = 000b VA: VA1 (180h), VA2 (190h), VA3 (1A0h), VA4 (1B0h), VA5 (1C0h), VA6 (1D0h), VA7 (1E0h), VA8 (1F0h) FRAME NUMBER: 0, 1, 2, 3, 4, 5, 6, 7	VD or F_{LOAD} (selected by 022h[1:0])
			[5:3]	Frame TRG	3	Set frame number when trigger input		TRIG input when 021[2] is enabled
$V_{EVENT}1$	55	37	[5:0]	LSB	Start	12	Vertical event start 1	Event number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	56	38	[5:0]	MSB				
	57	39	[5:0]	LSB	Stop	12	Vertical event stop 1	
	58	3A	[5:0]	MSB				
$V_{EVENT}2$	59	3B	[5:0]	LSB	Start	12	Vertical event start 2	
	60	3C	[5:0]	MSB				
	61	3D	[5:0]	LSB	Stop	12	Vertical event stop 2	
	62	3E	[5:0]	MSB				
—	63	3F	[5:0]	—		6	Reserved	Reserved Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])

Table 95. Detailed TG Section (continued)

SECTION	ADDRESS		PARAMETER				DESCRIPTION		UPDATE METHOD
	DEC	HEX	BITS	PARAMETER		# OF BITS	DESCRIPTION	VALUE	
MECH SHUT1	64	40	[5:0]	LSB	PIX	13	Mechanical shutter 1 toggling pix	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	65	41	[5:0]	MID					
	66	42	[0]	MSB					
			[5:1]	LSB	Line	12	Mechanical shutter 1 toggling line	Line number Default = 0 (DEC)	
	67	43	[5:0]	MID					
	68	44	[0]	MSB					
			[5:1]	LSB	Frame	6	Mechanical shutter 1 toggling frame	Frame number Default = 0 (DEC)	
	69	45	[0]	MSB					
			[1]	POL		1	Mechanical shutter 1 toggling polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
MECH SHUT2	70	46	[5:0]	LSB	PIX	13	Mechanical shutter 2 toggling pix	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	71	47	[5:0]	MID					
	72	48	[0]	MSB					
			[5:1]	LSB	Line	12	Mechanical shutter 2 toggling line	Line number Default = 0 (DEC)	
	73	49	[5:0]	MID					
	74	4A	[0]	MSB					
			[5:1]	LSB	Frame	6	Mechanical shutter 2 toggling frame	Frame number Default = 0 (DEC)	
	75	4B	[0]	MSB					
			[1]	POL		1	Mechanical shutter 2 toggling polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
Strobe 1	76	4C	[5:0]	LSB	PIX	13	Strobe 1 toggling pix	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	77	4D	[5:0]	MID					
	78	4E	[0]	MSB					
			[5:1]	LSB	Line	12	Strobe 1 toggling line	Line number Default = 0 (DEC)	
	79	4F	[5:0]	MID					
	80	50	[0]	MSB					
			[5:1]	LSB	Frame	6	Strobe 1 toggling frame	Frame number Default = 0 (DEC)	
	81	51	[0]	MSB					
			[1]	POL		1	Strobe 1 toggling polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
Strobe 2	82	52	[5:0]	LSB	PIX	13	Strobe 2 toggling pix	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	83	53	[5:0]	MID					
	84	54	[0]	MSB					
			[5:1]	LSB	Line	12	Strobe 2 toggling line	Line number Default = 0 (DEC)	
	85	55	[5:0]	MID					
	86	56	[0]	MSB					
			[5:1]	LSB	Frame	6	Strobe 2 toggling frame	Frame number Default = 0 (DEC)	
	87	57	[0]	MSB					
			[1]	POL		1	Strobe 2 toggling polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	

Table 95. Detailed TG Section (continued)

SECTION	ADDRESS		PARAMETER			# OF BITS	DESCRIPTION		UPDATE METHOD
	DEC	HEX	BITS	PARAMETER			DESCRIPTION	VALUE	
Strobe 3	88	58	[5:0]	LSB	PIX	13	Strobe 3 toggling pix	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	89	59	[5:0]	MID					
	90	5A	[0]	MSB					
			[5:1]	LSB	Line	12	Strobe 3 toggling line	Line number Default = 0 (DEC)	
	91	5B	[5:0]	MID					
	92	5C	[0]	MSB					
			[5:1]	LSB	Frame	6	Strobe 3 toggling frame	Frame number Default = 0 (DEC)	
	93	5D	[0]	MSB					
			[1]	POL		1	Strobe 3 toggling polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
Strobe 4	94	5E	[5:0]	LSB	PIX	13	Strobe 4 toggling pix	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	95	5F	[5:0]	MID					
	96	60	[0]	MSB					
			[5:1]	LSB	Line	12	Strobe 4 toggling line	Line number Default = 0 (DEC)	
	97	61	[5:0]	MID					
	98	62	[0]	MSB					
			[5:1]	LSB	Frame	6	Strobe 4 toggling frame	Frame number Default = 0 (DEC)	
	99	63	[0]	MSB					
			[1]	POL		1	Strobe 4 toggling polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
Strobe 5	100	64	[5:0]	LSB	PIX	13	Strobe 5 toggling pix	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	101	65	[5:0]	MID					
	102	66	[0]	MSB					
			[5:1]	LSB	Line	12	Strobe 5 toggling line	Line number Default = 0 (DEC)	
	103	67	[5:0]	MID					
	104	68	[0]	MSB					
			[5:1]	LSB	Frame	6	Strobe 5 toggling frame	Frame number Default = 0 (DEC)	
	105	69	[0]	MSB					
			[1]	POL		1	Strobe 5 toggling polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
Strobe 6	106	6A	[5:0]	LSB	PIX	13	Strobe 6 toggling pix	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	107	6B	[5:0]	MID					
	108	6C	[0]	MSB					
			[5:1]	LSB	Line	12	Strobe 6 toggling line	Line number Default = 0 (DEC)	
	109	6D	[5:0]	MID					
	110	6E	[0]	MSB					
			[5:1]	LSB	Frame	6	Strobe 6 toggling frame	Frame number Default = 0 (DEC)	
	111	6F	[0]	MSB					
			[1]	POL		1	Strobe 6 toggling polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	

Table 95. Detailed TG Section (continued)

SECTION	ADDRESS		PARAMETER				DESCRIPTION		UPDATE METHOD
	DEC	HEX	BITS	PARAMETER		# OF BITS	DESCRIPTION	VALUE	
Strobe 7	112	70	[5:0]	LSB	PIX	13	Strobe 7 toggling pix	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	113	71	[5:0]	MID					
	114	72	[0]	MSB					
			[5:1]	LSB	Line	12	Strobe 7 toggling line	Line number Default = 0 (DEC)	
	115	73	[5:0]	MID					
	116	74	[0]	MSB					
			[5:1]	LSB	Frame	6	Strobe 7 toggling frame	Frame number Default = 0 (DEC)	
	117	75	[0]	MSB					
			[1]	POL		1	Strobe 7 toggling polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
Strobe 8	118	76	[5:0]	LSB	PIX	13	Strobe 8 toggling pix	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	119	77	[5:0]	MID					
	120	78	[0]	MSB					
			[5:1]	LSB	Line	12	Strobe 8 toggling line	Line number Default = 0 (DEC)	
	121	79	[5:0]	MID					
	122	7A	[0]	MSB					
			[5:1]	LSB	Frame	6	Strobe 8 toggling frame	Frame number Default = 0 (DEC)	
	123	7B	[0]	MSB					
			[1]	POL		1	Strobe 8 toggling polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
SUBSW1-1	124	7C	[5:0]	LSB	Line	12	SUBSW1-1 toggling line	Line number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	125	7D	[5:0]	MSB					
	126	7E	[5:0]	Frame		6	SUBSW1-1 toggling frame	Frame number Default = 0 (DEC)	
	127	7F	[0]	POL		1	SUBSW1-1 polarity	0 = Low (default) 1 = High	
			[5:1]	—		5	Reserved	Reserved Default = 0 (DEC)	
SUBSW1-2	128	80	[5:0]	LSB	Line	12	SUBSW1-2 toggling line	Line number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	129	81	[5:0]	MSB					
	130	82	[5:0]	Frame		6	SUBSW1-2 toggling frame	Frame number Default = 0 (DEC)	
	131	83	[0]	POL		1	SUBSW1-2 polarity	0 = Low (default) 1 = High	
			[5:1]	—		5	Reserved	Reserved Default = 0 (DEC)	
SUBSW2-1	132	84	[5:0]	LSB	Line	12	SUBSW2-1 toggling line	Line number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	133	85	[5:0]	MSB					
	134	86	[5:0]	Frame		6	SUBSW2-1 toggling frame	Frame number Default = 0 (DEC)	
	135	87	[0]	POL		1	SUBSW2-1 polarity	0 = Low (default) 1 = High	
			[5:1]	—		5	Reserved	Reserved Default = 0 (DEC)	
SUBSW2-2	136	88	[5:0]	LSB	Line	12	SUBSW2-2 toggling line	Line number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	137	89	[5:0]	MSB					
	138	8A	[5:0]	Frame		6	SUBSW2-2 toggling frame	Frame number Default = 0 (DEC)	
	139	8B	[0]	POL		1	SUBSW2-2 polarity	0 = Low (default) 1 = High	
			[5:1]	—		5	Reserved	Reserved Default = 0 (DEC)	

Table 95. Detailed TG Section (continued)

SECTION	ADDRESS		PARAMETER			# OF BITS	DESCRIPTION		UPDATE METHOD
	DEC	HEX	BITS	PARAMETER			DESCRIPTION	VALUE	
SUBN 1	140	8C	[5:0]	LSB	PIX	13	SUBN 1 toggling pixel	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	141	8D	[5:0]	MID					
	142	8E	[0]	MSB					
			[1]	POL		1	SUBN 1 polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
SUBN 2	143	8F	[5:0]	LSB	PIX	13	SUBN 2 toggling pixel	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	144	90	[5:0]	MID					
	145	91	[0]	MSB					
			[1]	POL		1	SUBN 2 polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
SUBN 3	146	92	[5:0]	LSB	PIX	13	SUBN 3 toggling pixel	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	147	93	[5:0]	MID					
	148	94	[0]	MSB					
			[1]	POL		1	SUBN 3 polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
SUBN 4	149	95	[5:0]	LSB	PIX	13	SUBN 4 toggling pixel	Pixel number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	150	96	[5:0]	MID					
	151	97	[0]	MSB					
			[1]	POL		1	SUBN 4 polarity	0 = Low (default) 1 = High	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
SUBN CHG 1	152	98	[5:0]	LSB	Line	12	Electric shutter 1 toggling line	Line number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	153	99	[5:0]	MSB					
	154	9A	[1:0]	Pattern		2	Electric shutter 1 SUBN pattern	Pattern number Default = 00b	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
SUBN CHG 2	155	9B	[5:0]	LSB	Line	12	Electric shutter 2 toggling line	Line number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	156	9C	[5:0]	MSB					
	157	9D	[1:0]	Pattern		2	Electric shutter 2 SUBN pattern	Pattern number Default = 00b	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
SUBN CHG 3	158	9E	[5:0]	LSB	Line	12	Electric shutter 3 toggling line	Line number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	159	9F	[5:0]	MSB					
	160	A0	[1:0]	Pattern		2	Electric shutter 3 SUBN pattern	Pattern number Default = 00b	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	
SUBN CHG 4	161	A1	[5:0]	LSB	Line	12	Electric shutter 4 toggling line	Line number Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
	162	A2	[5:0]	MSB					
	163	A3	[1:0]	Pattern		2	Electric shutter 4 SUBN pattern	Pattern number Default = 00b	
			[5:2]	—		4	Reserved	Reserved Default = 0000b	

Table 95. Detailed TG Section (continued)

SECTION	ADDRESS		PARAMETER			DESCRIPTION		UPDATE METHOD
	DEC	HEX	BITS	PARAMETER	# OF BITS	DESCRIPTION	VALUE	
—	164	A4	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	Real time or R_Update (selected by 000h[3])
—	165	A5	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	166	A6	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	167	A7	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	168	A8	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	169	A9	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	170	AA	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	171	AB	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	172	AC	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	173	AD	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	174	AE	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	175	AF	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	176	B0	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	177	B1	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	178	B2	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	179	B3	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	180	B4	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
Monitor pin select	181	B5	[3:0]	←	4	Monitor pin selection	1000b = TPP = SHP, TPD = SHD 1001b = TPP = CLPOB, TPD = CLPDM 1010b = TPP = PBLK, TPD = HDIV 1011b = TPP =HBLK, TPD = (na) Default = 0000b	Real time or R_Update (selected by 000h[3])
			[5:4]	—	2	Reserved	Reserved Default = 00b	Real time or R_Update (selected by 000h[3])
—	182	B6	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	183	B7	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	184	B8	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	185	B9	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	186	BA	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	187	BB	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	188	BC	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	189	BD	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	190	BE	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	
—	191	BF	[5:0]	—	6	Reserved	Reserved Default = 0 (DEC)	

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VSP01M01ZWD	OBSOLETE	NFBGA	ZWD	100		TBD	Call TI	Call TI	0 to 85	VSP01M01	
VSP01M01ZWDR	NRND	NFBGA	ZWD	100	1000	Pb-Free (RoHS)	SNAGCU	Level-2-260C-1 YEAR	0 to 85	VSP01M01	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

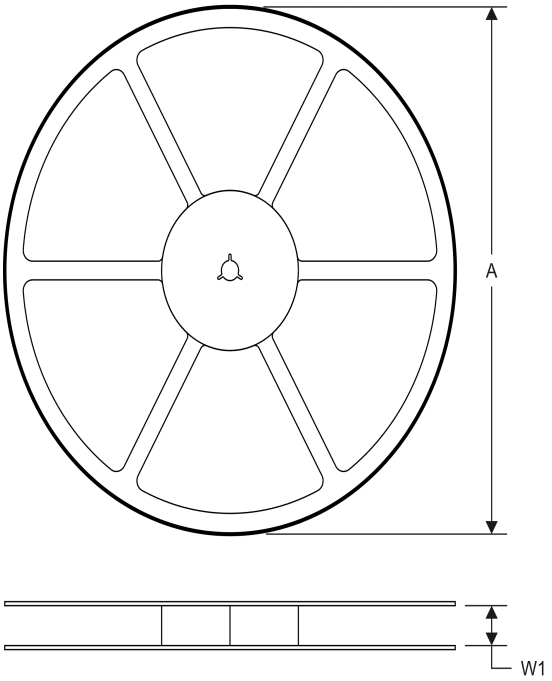
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

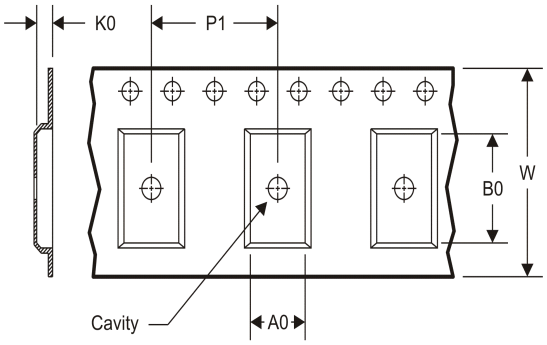
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



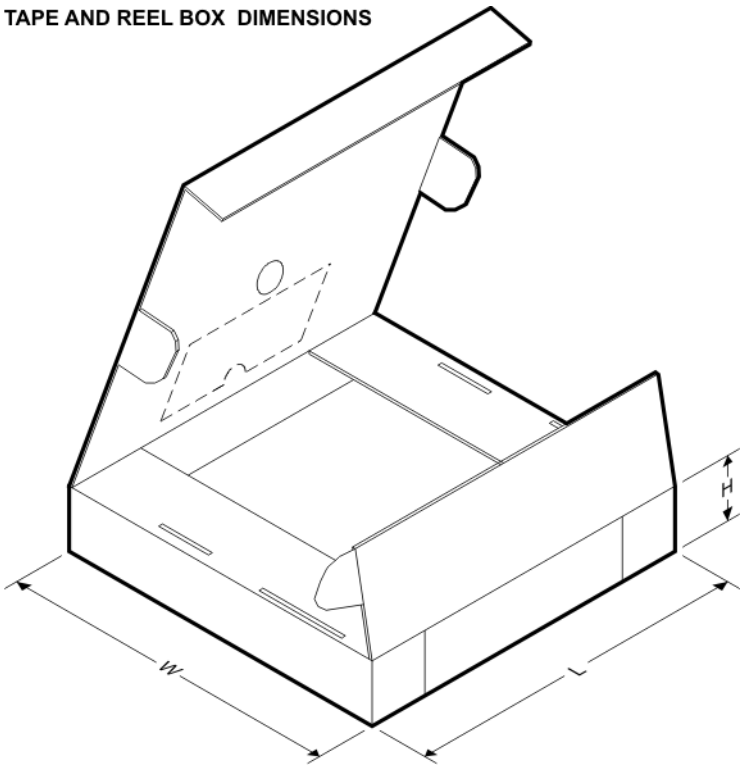
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP01M01ZWDR	NFBGA	ZWD	100	1000	330.0	16.4	7.3	7.3	2.2	12.0	16.0	Q1

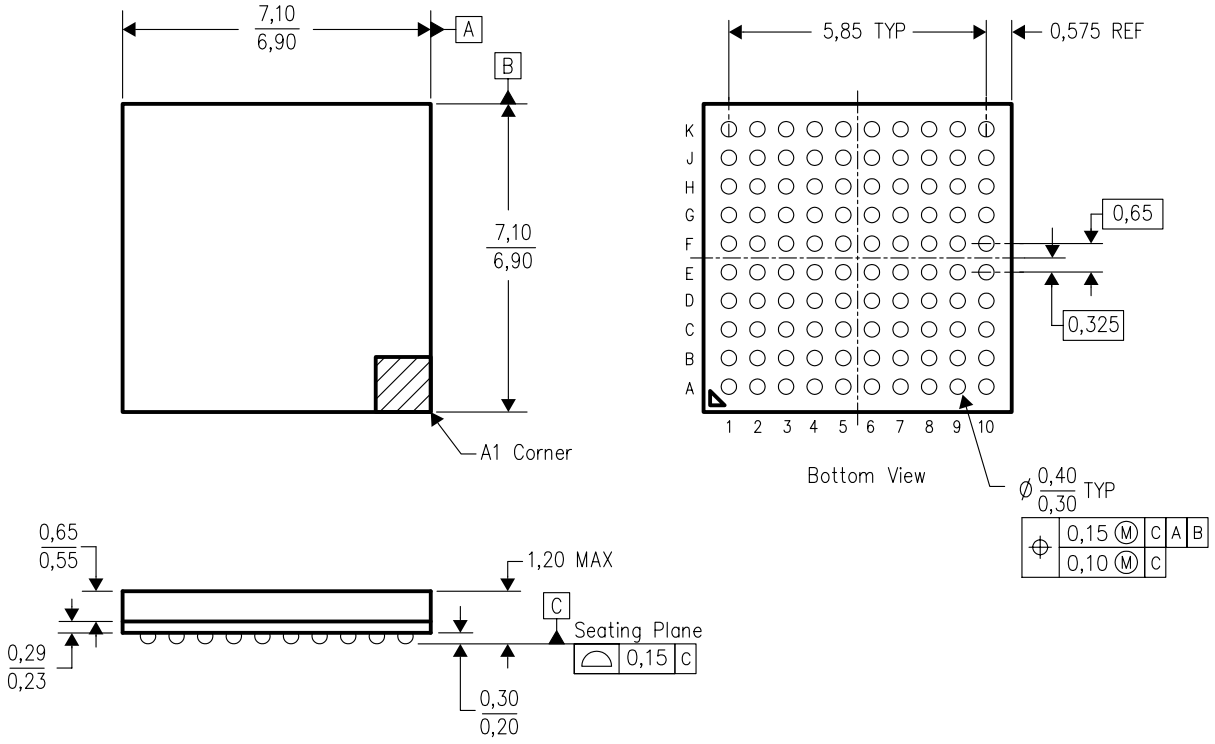
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP01M01ZWDR	NFBGA	ZWD	100	1000	342.0	336.0	34.0

ZWD (S–PBGA–N100) PLASTIC BALL GRID ARRAY



4206873/A 03/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead–free.

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