阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

ADC0801S040

Single 8 bits ADC, up to 40 MHz

Rev. 02 — 18 August 2008 Product data sheet

1. General description

The ADC0801S040 is an 8-bit universal analog-to-digital converter (ADC) for video and general purpose applications. It converts the analog input signal from 2.7 V to 5.5 V into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are CMOS/Transistor-Transistor Logic (TTL) compatible. A sleep mode allows reduction of the device power consumption to 4 mW.

2. Features

- 8-bit resolution
- Operation between 2.7 V and 5.5 V
- Sampling rate up to 40 MHz
- DC sampling allowed
- High signal-to-noise ratio over a large analog input frequency range (7.3 effective bits at 4.43 MHz full-scale input at f_{clk} = 40 MHz)
- CMOS/TTL compatible digital inputs and outputs
- External reference voltage regulator
- Power dissipation only 30 mW (typical value)
- Low analog input capacitance, no buffer amplifier required
- Sleep mode (4 mW)
- No sample-and-hold circuit required

3. Applications

- Video data digitizing
- Camera
- Camcorder
- Radio communication
- Car alarm system

4. Quick reference data

Table 1. Quick reference data

V_{DDA} = V5 to V6 = 3.3 V; V_{DDD} = V3 to V4 = 3.3 V; V_{DDO} = V20 to V11 = 3.3 V; V_{SSA}, V_{SSD} and V_{SSO} shorted together; $V_{i(a)(p-p)}$ = 1.84 V; C_L = 20 pF; T_{amb} = 0 °C to 70 °C; typical values measured at T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	analog supply voltage		2.7	3.3	5.5	V
V_{DDD}	digital supply voltage		2.7	3.3	5.5	V
V_{DDO}	output supply voltage		2.5	3.3	5.5	V
ΔV_{DD}	supply voltage difference	$V_{DDA} - V_{DDD}$	–0.2	-	+0.2	V
		$V_{DDD} - V_{DDO}$	–0.2	-	+2.25	V
I_{DDA}	analog supply current		-	4	6	mA
I_{DDD}	digital supply current		-	5	8	mA
I_{DDO}	output supply current	f_{clk} = 40 MHz; ramp input; C_L = 20 pF	-	1	2	mA
INL	integral non-linearity	ramp input; see Figure 6	-	±0.5	±0.75	LSB
DNL	differential non-linearity	ramp input; see Figure 7	-	±0.25	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency		40	-	-	MHz
P_{tot}	total power dissipation	$V_{DDA} = V_{DDD} = V_{DDO}$ = 3.3 V	-	30	53	mW

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
ADC0801S040TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

6. Block diagram

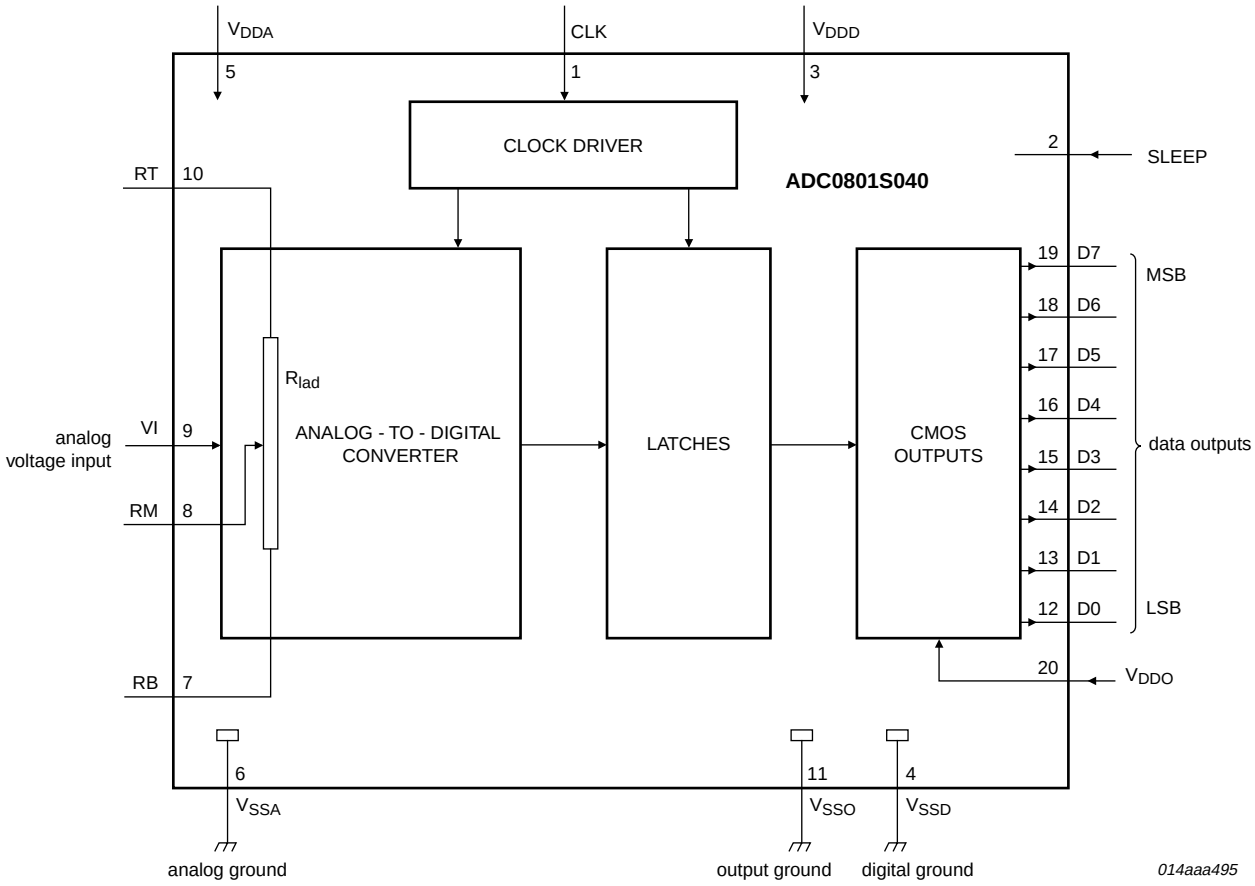


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

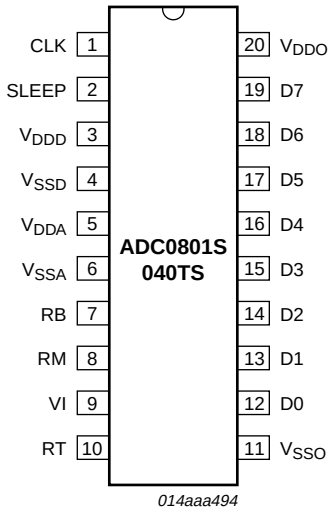


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CLK	1	clock input
SLEEP	2	sleep mode input
V_{DDD}	3	digital supply voltage (2.7 V to 5.5 V)
V_{SSD}	4	digital ground
V_{DDA}	5	analog supply voltage (2.7 V to 5.5 V)
V_{SSA}	6	analog ground
RB	7	reference voltage BOTTOM input
RM	8	reference voltage MIDDLE
VI	9	analog input voltage
RT	10	reference voltage TOP input
V_{SSO}	11	output stage ground
D0	12	data output; bit 0 (Least Significant Bit (LSB))
D1	13	data output; bit 1
D2	14	data output; bit 2
D3	15	data output; bit 3
D4	16	data output; bit 4
D5	17	data output; bit 5

Table 3. Pin description *...continued*

Symbol	Pin	Description
D6	18	data output; bit 6
D7	19	data output; bit 7 (Most Significant Bit (MSB))
V_{DDO}	20	positive supply voltage for output stage (2.7 V to 5.5 V)

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDA}	analog supply voltage		[1]	–0.3	+7.0	V
V_{DDD}	digital supply voltage		[1]	–0.3	+7.0	V
V_{DDO}	output supply voltage		[1]	–0.3	+7.0	V
ΔV_{DD}	supply voltage difference	$V_{DDA} - V_{DDD}$; $V_{DDD} - V_{DDO}$; $V_{DDA} - V_{DDO}$		–0.1	+4.0	V
V_I	input voltage	referenced to V_{SSA}		–0.3	+7.0	V
$V_{i(clk)(p-p)}$	peak-to-peak clock input voltage	referenced to V_{SSD}		-	V_{DDD}	V
I_O	output current			-	10	mA
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–20	+75	°C
T_j	junction temperature			-	150	°C

[1] The supply voltages V_{DDA}, V_{DDD} and V_{DDO} may have any value between –0.3 V and +7.0 V provided that the supply voltage ΔV_{DD} remains as indicated.

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Condition	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	120	K/W

10. Characteristics

Table 6. Characteristics

V_{DDA} = V5 to V6 = 3.3 V; V_{DDD} = V3 to V4 = 3.3 V; V_{DDO} = V20 to V11 = 3.3 V; V_{SSA}, V_{SSD} and V_{SSO} shorted together; $V_{i(a)(p-p)}$ = 1.84 V; C_L = 20 pF; T_{amb} = 0 °C to 70 °C; typical values measured at T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDA}	analog supply voltage		2.7	3.3	5.5	V
V_{DDD}	digital supply voltage		2.7	3.3	5.5	V
V_{DDO}	output supply voltage		2.5	3.3	5.5	

Table 6. Characteristics *...continued*

V_{DDA} = V5 to V6 = 3.3 V; V_{DDD} = V3 to V4 = 3.3 V; V_{DDO} = V20 to V11 = 3.3 V; V_{SSA}, V_{SSD} and V_{SSO} shorted together; $V_{i(a)(p-p)}$ = 1.84 V; C_L = 20 pF; T_{amb} = 0 °C to 70 °C; typical values measured at T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔV_{DD}	supply voltage difference	$V_{DDA} - V_{DDD}$		–0.2	-	+0.2	V
		$V_{DDD} - V_{DDO}$		–0.2	-	+2.25	V
I_{DDA}	analog supply current			-	4	6	mA
I_{DDD}	digital supply current			-	5	8	mA
I_{DDO}	output supply current	f_{clk} = 40 MHz; ramp input; C_L = 20 pF		-	1	2	mA
P_{tot}	total power dissipation	$V_{DDA} = V_{DDD} = V_{DDO}$ = 3.3 V		-	30	53	mW
Inputs							
Clock input CLK (Referenced to V_{SSD})[1]							
V_{IL}	LOW-level input voltage			0	-	0.3 V_{DDD}	V
V_{IH}	HIGH-level input voltage	$V_{DDD} \leq$ 3.6 V		0.6 V_{DDD}	-	V_{DDD}	V
		V_{DDD} > 3.6 V		0.7 V_{DDD}	-	V_{DDD}	V
I_{IL}	LOW-level input current	V_{clk} = 0.3 V_{DDD}		–1	0	+1	µA
I_{IH}	HIGH-level input current	V_{clk} = 0.7 V_{DDD}		-	-	5	µA
Z_i	input impedance	f_{clk} = 40 MHz		-	4	-	kΩ
C_i	input capacitance	f_{clk} = 40 MHz		-	3	-	pF
Input SLEEP (Referenced to V_{SSD}); see Table 8							
V_{IL}	LOW-level input voltage			0	-	0.3 V_{DDD}	V
V_{IH}	HIGH-level input voltage	$V_{DDD} \leq$ 3.6 V		0.6 V_{DDD}	-	V_{DDD}	V
		V_{DDD} > 3.6 V		0.7 V_{DDD}	-	V_{DDD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.3 V_{DDD}		–1	-	-	µA
I_{IH}	HIGH-level input current	V_{IH} = 0.7 V_{DDD}		-	-	+1	µA
Analog input VI (Referenced to V_{SSA})							
I_{IL}	LOW-level input current	$V_I = V_{RB}$		-	0	-	µA
I_{IH}	HIGH-level input current	$V_I = V_{RT}$		-	9	-	µA
Z_i	input impedance	f_i = 1 MHz		-	20	-	kΩ
C_i	input capacitance	f_i = 1 MHz		-	2	-	pF
Reference voltages for the resistor ladder; see Table 7							
V_{RB}	voltage on pin RB			1.1	1.2	-	V
V_{RT}	voltage on pin RT	$V_{RT} \leq V_{DDA}$		2.7	3.3	V_{DDA}	V
$V_{ref(dif)}$	differential reference voltage	$V_{RT} - V_{RB}$		1.5	2.1	2.7	V
I_{ref}	reference current			-	0.95	-	mA
R_{lad}	ladder resistance			-	2.2	-	kΩ
TC_{Rlad}	ladder resistor temperature coefficient			-	4092	-	mΩ/K
V_{offset}	offset voltage	BOTTOM	[2]	-	170	-	mV
		TOP	[2]	-	170	-	mV
$V_{i(a)(p-p)}$	peak-to-peak analog input voltage		[3]	1.4	1.76	2.4	V

Table 6. Characteristics *...continued*

V_{DDA} = V5 to V6 = 3.3 V; V_{DDD} = V3 to V4 = 3.3 V; V_{DDO} = V20 to V11 = 3.3 V; V_{SSA}, V_{SSD} and V_{SSO} shorted together; $V_{i(a)(p-p)}$ = 1.84 V; C_L = 20 pF; T_{amb} = 0 °C to 70 °C; typical values measured at T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Digital outputs D7 to D0 and IR (Referenced to V_{SSD})							
V_{OL}	LOW-level output voltage	I_O = 1 mA		0	-	0.5	V
V_{OH}	HIGH-level output voltage	I_O = –1 mA		V_{DDO} – 0.5	-	V_{DDO}	V
I_{OZ}	OFF-state output current	0.4 V < V_O < V_{DDO}		–20	-	+20	µA
Clock input CLK; see Figure 4 [1]							
$f_{clk(max)}$	maximum clock frequency			40	-	-	MHz
$t_{w(clk)H}$	HIGH clock pulse width			9	-	-	ns
$t_{w(clk)L}$	LOW clock pulse width			9	-	-	ns
Analog signal processing (f_{clk} = 40 MHz)							
Linearity							
INL	integral non-linearity	ramp input; see Figure 6		-	±0.5	±0.75	LSB
DNL	differential non-linearity	ramp input; see Figure 7		-	±0.25	±0.5	LSB
Bandwidth							
B	bandwidth	full-scale sine wave	[4]	-	10		MHz
		75 % full-scale sine wave		-	13		MHz
		50 % full-scale sine wave		-	20		MHz
		small signal at mid scale; V_i = ±10 LSB at code 128		-	350		MHz
Input set response; see Figure 8 [5]							
$t_{s(LH)}$	LOW to HIGH settling time	full-scale square wave		-	3	5	ns
$t_{s(HL)}$	HIGH to LOW settling time	full-scale square wave		-	3	5	ns
Harmonics; see Figure 9 [6]							
THD	total harmonic distortion	f_i = 4.43 MHz		-	–50	-	dB
Signal-to-Noise ratio; see Figure 9 [6]							
S/N	signal-to-noise ratio	without harmonics; f_i= 4.43 MHz		-	47	-	dB
Effective bits; see Figure 9 [6]							
ENOB	effective number of bits	f_i = 300 MHz		-	7.8	-	bits
		f_i = 4.43 MHz		-	7.3	-	bits
Differential gain [7]							
G_{dif}	differential gain	PAL modulated ramp		-	1.5	-	%

Table 6. Characteristics *...continued*

V_{DDA} = V5 to V6 = 3.3 V; V_{DDD} = V3 to V4 = 3.3 V; V_{DDO} = V20 to V11 = 3.3 V; V_{SSA}, V_{SSD} and V_{SSO} shorted together; $V_{i(a)(p-p)}$ = 1.84 V; C_L = 20 pF; T_{amb} = 0 °C to 70 °C; typical values measured at T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Differential phase[7]						
φ_{dif}	differential phase	PAL modulated ramp	-	0.25	-	deg
Timing (f_{clk} = 40 MHz; C_L = 20 pF); see Figure 4[8]						
$t_{d(s)}$	sampling delay time		-	-	5	ns
$t_{h(o)}$	output hold time		5	-	-	ns
$t_{d(o)}$	output delay time	V_{DDO} = 4.75 V	8	12	15	ns
		V_{DDO} = 3.15 V	8	17	20	ns
		V_{DDO} = 2.7 V	8	18	21	ns
3-state output delay times; see Figure 5						
t_{dHZ}	active HIGH to float delay time		-	14	18	ns
t_{dZL}	float to active LOW delay time		-	16	20	ns
t_{dZH}	float to active HIGH delay time		-	16	20	ns
t_{dLZ}	active LOW to float delay time		-	14	18	ns

[1] In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.

[2] Analog input voltages producing code 0 up to and including code 255:

a) V_{offset} BOTTOM is the difference between the analog input which produces data equal to 00 and the reference voltage on pin RB (V_{RB}) at T_{amb} = 25 °C.

b) V_{offset} TOP is the difference between the reference voltage on pin RT (V_{RT}) and the analog input which produces data outputs equal to code 255 at T_{amb} = 25 °C.

[3] To ensure the optimum linearity performance of such a converter architecture the lower and upper extremities of the converter reference resistor ladder are connected to pins RB and RT via offset resistors R_{OB} and R_{OT} as shown in Figure 3.

a) The current flowing into the resistor ladder is $I = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$ and the full-scale input range at the converter, to cover code 0 to 255 is $V_I = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} + V_{RB}) = 0.838 \times (V_{RT} - V_{RB})$

b) Since R_L, R_{OB} and R_{OT} have similar behavior with respect to process and temperature variation, the ratio $\frac{R_L}{R_{OB} + R_L + R_{OT}}$ will be kept reasonably constant from device to device. Consequently variation of the output codes at a given input voltage depends mainly on the difference $V_{RT} - V_{RB}$ and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is optimized.

[4] The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSB, nor any significant attenuation is observed in the reconstructed signal.

[5] The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square wave signal) in order to sample the signal and obtain correct output data.

[6] Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8000 acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (Nyquist frequency). Conversion to signal-to-noise ratio: S/N = ENOB × 6.02 + 1.76 dB.

[7] Measurement carried out using video analyzer VM700A, where video analog signal is reconstructed through a DAC.

[8] Output data acquisition: the output data is available after the maximum delay time of $t_{d(o)}$.

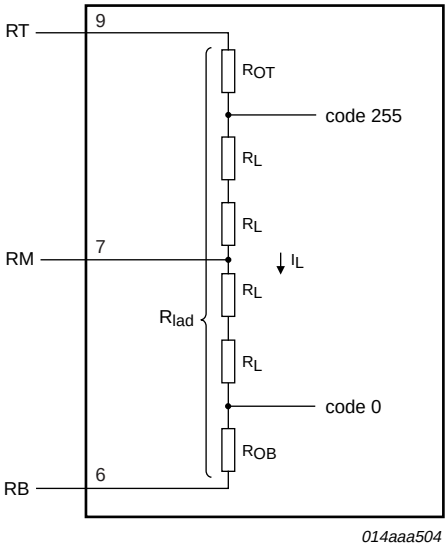


Fig 3. Explanation of Table 6 Table note 3

11. Additional information relating to Table 6

Table 7. Output coding and input voltage (typical values; referenced to V_{SSA})

Code	$V_{i(a)(p-p)}$ (V)	Binary outputs D7 to D0
Underflow	< 1.37	00 0000 00
0	1.37	00 0000 00
1	-	00 0000 01
↓	-	↓
254	-	11 11 11 10
255	3.13	11 11 11 11
Overflow	> 3.13	11 11 11 11

Table 8. Mode selection

SLEEP	D7 to D0	I_{DDA} + I_{DDD} (typ)
1	high impedance	1.2 mA
0	active	9 mA

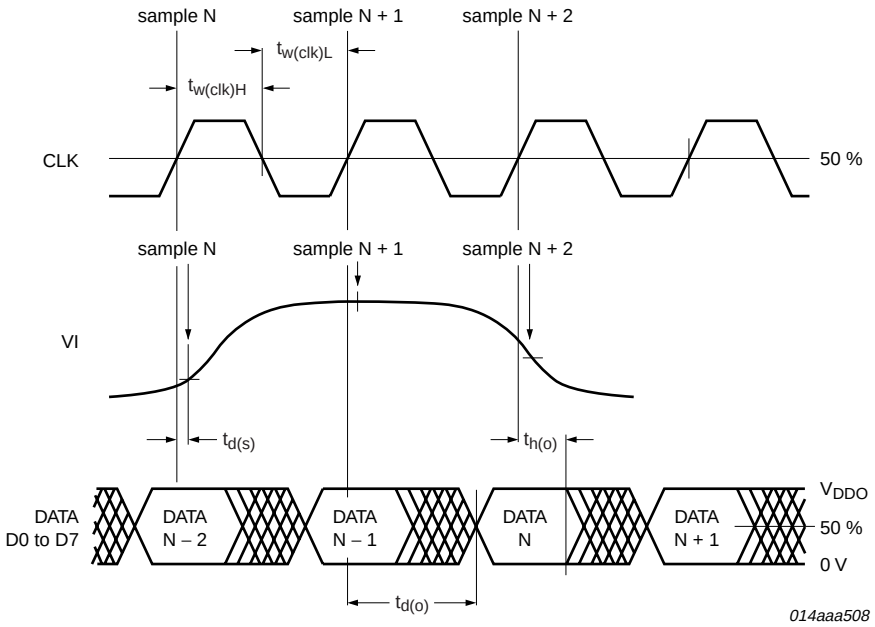
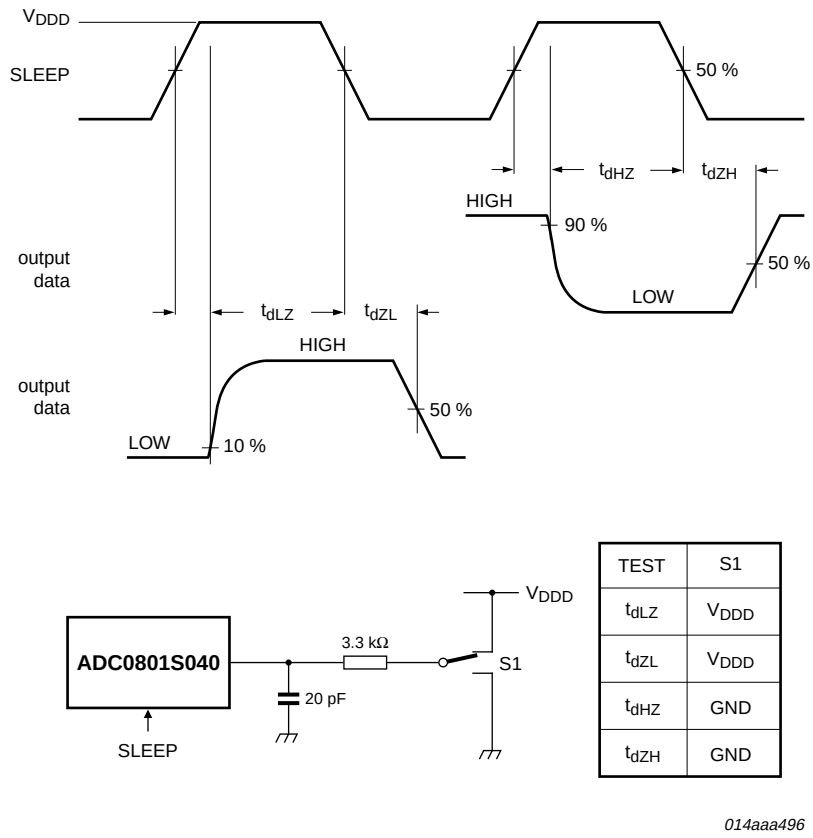


Fig 4. Timing diagram



TEST	S1
t_{dLZ}	V_{DDD}
t_{dZL}	V_{DDD}
t_{dHZ}	GND
t_{dZH}	GND

frequency on pin SLEEP = 100 kHz.

Fig 5. Timing diagram and test conditions of 3-state output delay time

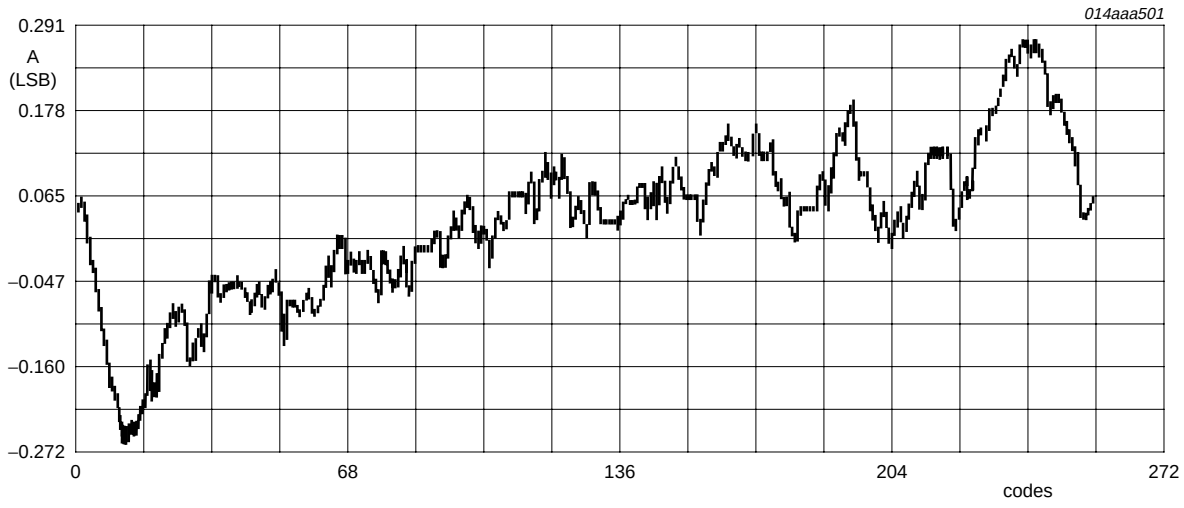


Fig 6. Typical Integral Non-Linearity (INL) performance

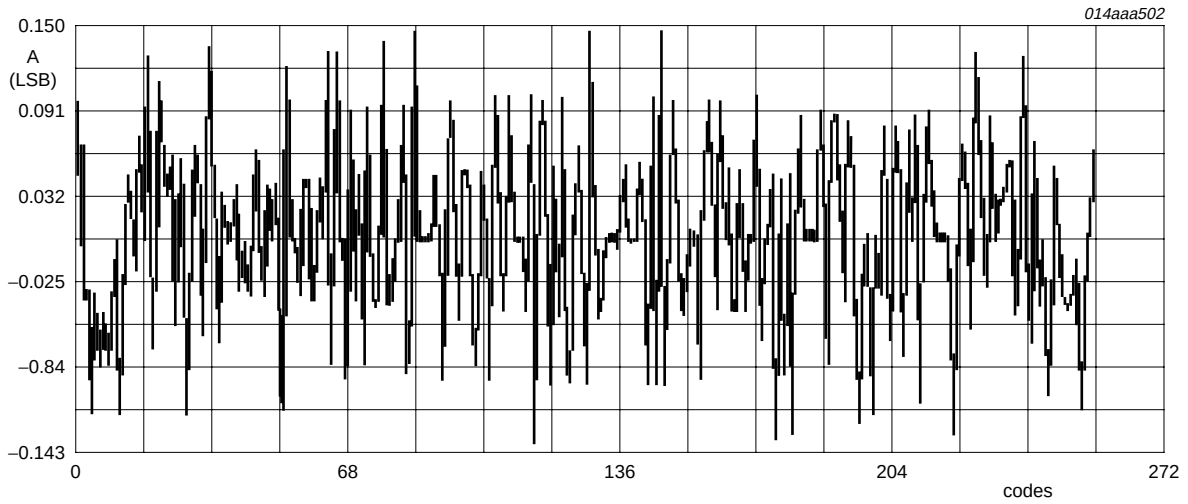


Fig 7. Typical Differential Non-Linearity (DNL) performance

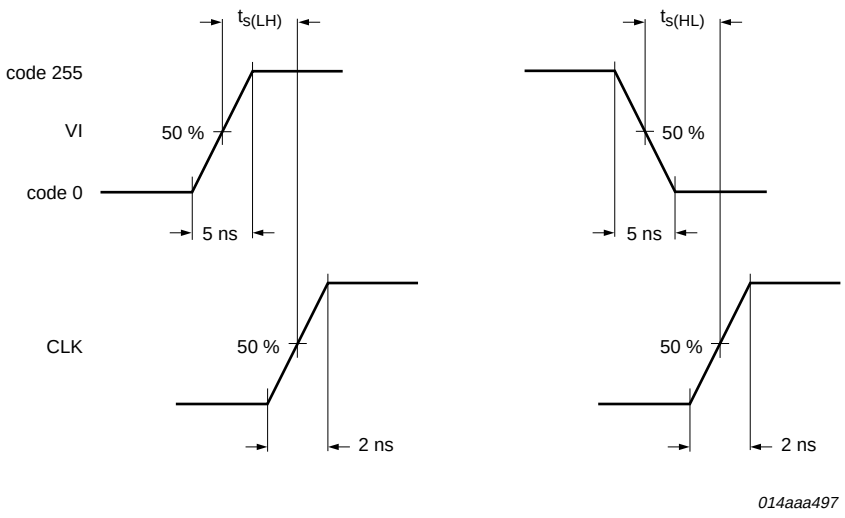
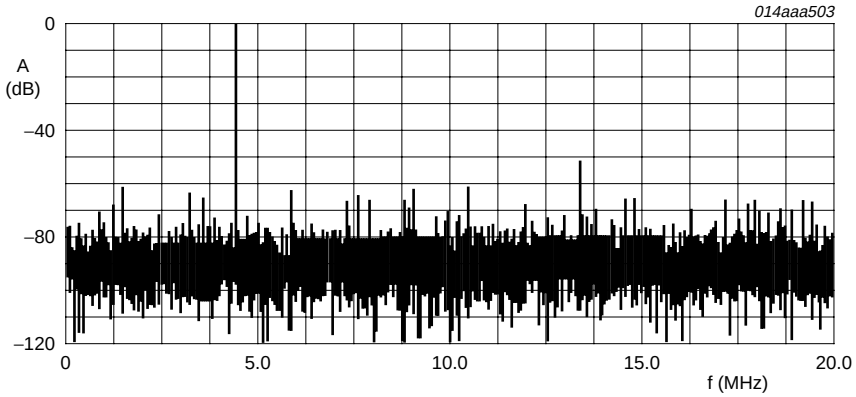


Fig 8. Analog input settling-time diagram



Effective bits: 7.32; THD = –51.08 dB.

Harmonic levels (dB): 2nd = –68.99; 3rd = –51.62; 4th = –66.05; 5th = –63.23; 6th = –72.79.

Fig 9. Typical fast Fourier transform (f_{clk} = 40 MHz; f_i = 4.43 MHz)

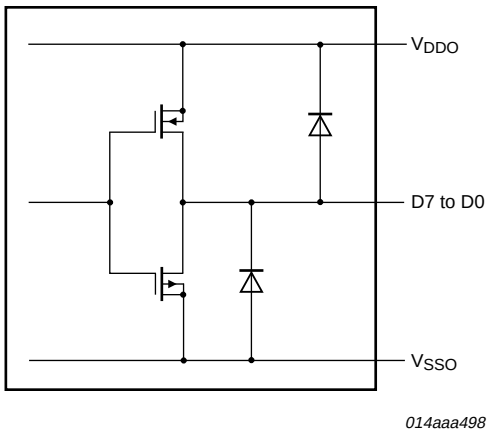


Fig 10. CMOS data outputs

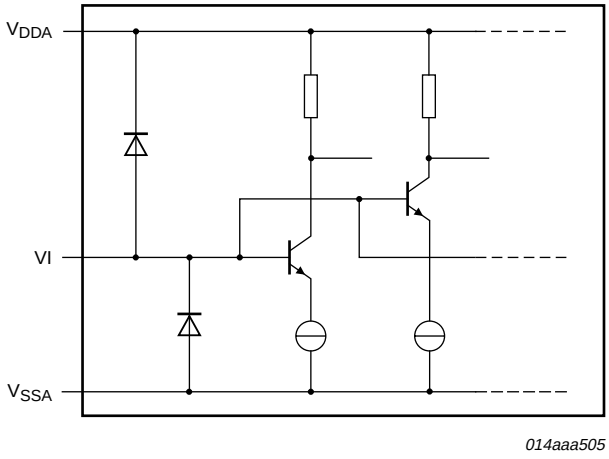


Fig 11. VI analog input

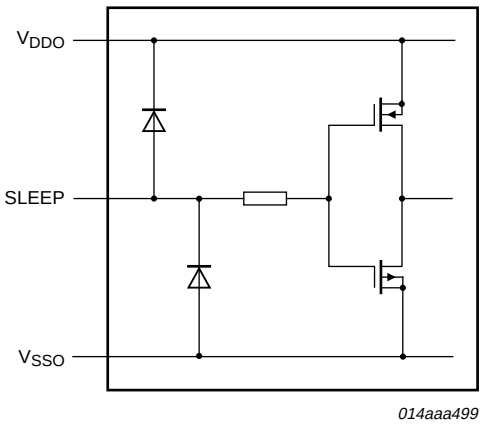


Fig 12. SLEEP 3-state input

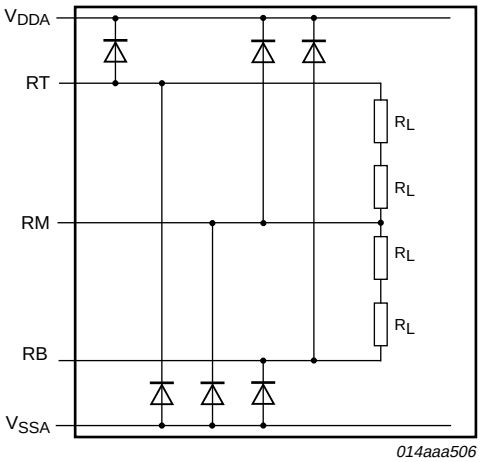


Fig 13. RB, RM and RT inputs

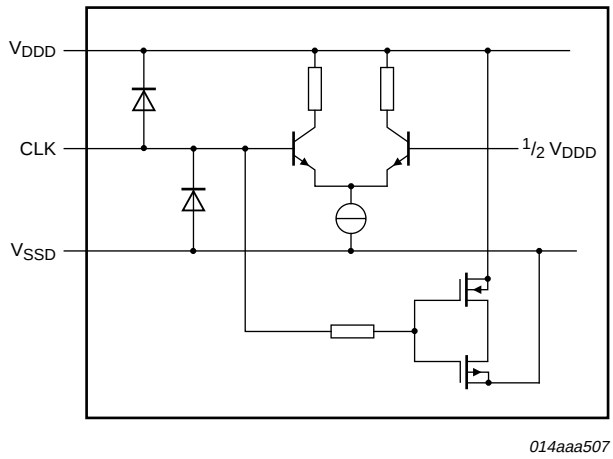
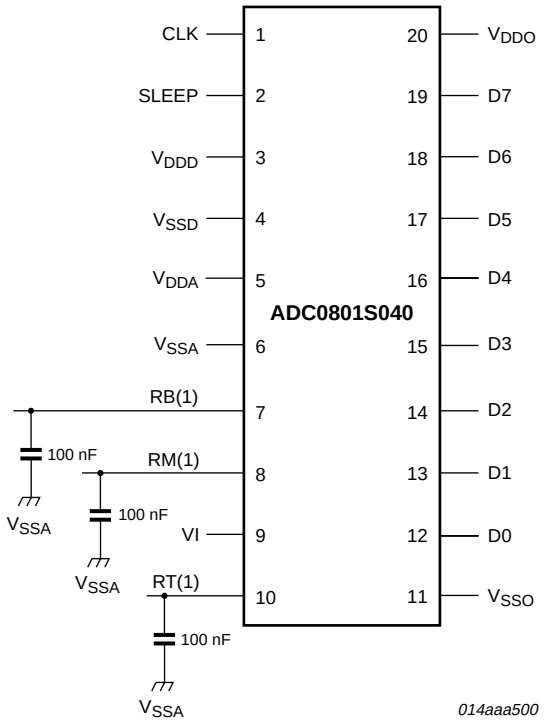


Fig 14. CLK input

12. Application information

12.1 Application diagrams



The analog and digital supplies should be separated and decoupled.

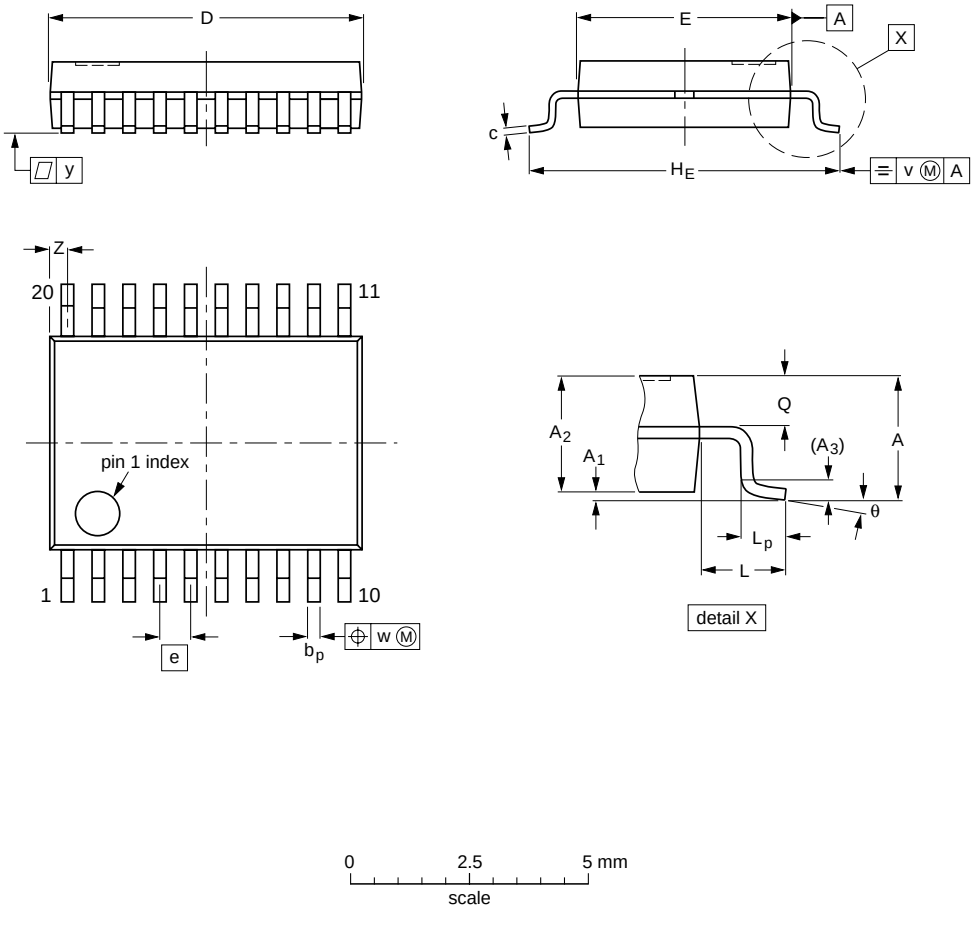
The external voltage reference generator must be built in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated V_{DDA} supply through a resistor bridge and a decoupling capacitor.

(1) RB, RM, RT are decoupled to V_{SSA}.

Fig 15. Application diagram

13. Package outline

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT266-1		MO-152				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT266-1 (SSOP20)

14. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC0801S040_2	20080818	Product data sheet	-	ADC0801S040_1
Modifications:	• Corrections made to table notes in Figure 1. • Corrections made to Table 3. • Corrections made to symbol in Table 4. • Corrections made to Table 6. • Corrections made to Figure 13			
ADC0801S040_1	20080612	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

17. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 18 August 2008
Document identifier: ADC0801S040_2