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AS1530, AS1531

Data Sheet

12-Bit, Single-Supply, Low-Power, 400/300ksps, 8-Channel A/D Converters

1 General Description

The AS1530/AS1531 are low-power,8/4-channel, 400/300ksps, 12-bit analog-to-digital (A/D) converters specifically designed to operate with single-supply devices. Superior AC characteristics, very low power consumption, and highly-reliable packaging make these ultra-small devices perfect for battery-powered remote-sensor and data-acquisition devices.

The successive-approximation register (SAR), high-speed sampling, high-bandwidth track/hold circuitry, and multi-mode operation combine to make these devices highly-flexible and configurable.

Both devices require low supply current (2.8mA @ 400ksps, AS1530; 2.2mA @ 300ksps, AS1531) and feature a reduced-power mode and a power-down mode to lower power consumption at slower throughput rates.

The devices operate from a single supply (+4.5 to +5.5V, AS1530; +2.7 to +3.6V, AS1531). Both devices contain an internal 2.5V reference, an integrated reference buffer, and feature support for an external reference (1V to V_{DD}).

Data accesses are made via the high-speed, 4-wire, SPI, QSPI-, and Microwire-compatible serial interface.

The devices are available in a 20-pin TSSOP package.

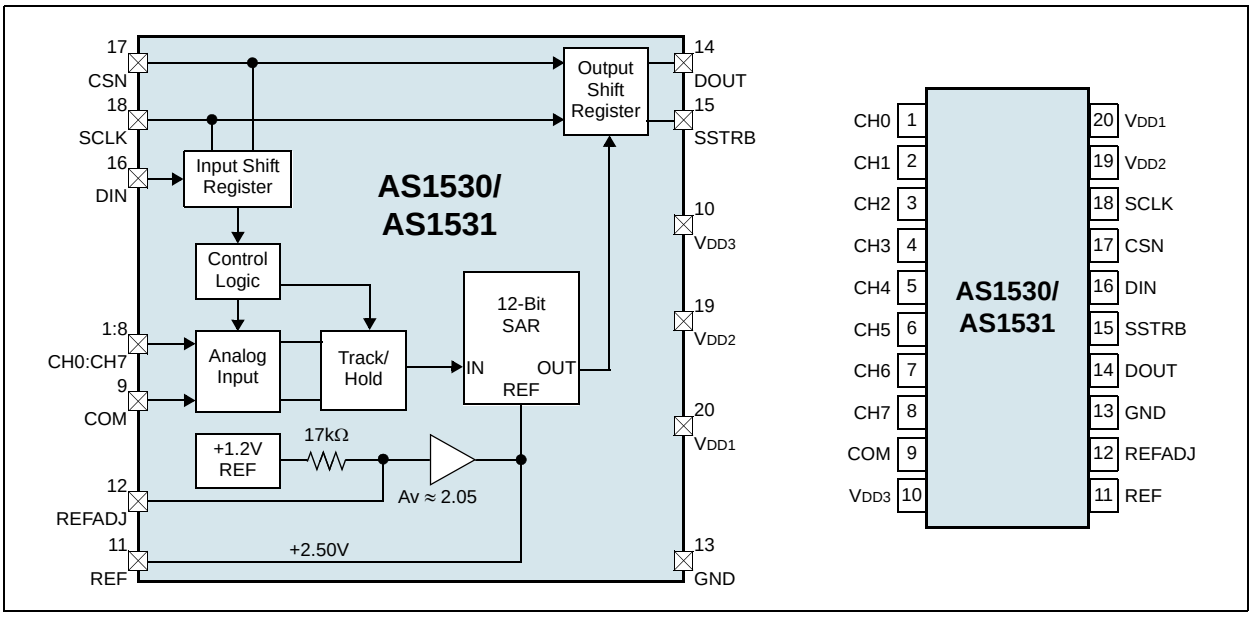
2 Key Features

- Single-Supply Operation:
  - +4.5 to +5.5V (AS1530)
  - +2.7 to +3.6V (AS1531)
- Sampling Rate:
  - 400ksps (AS1530)
  - 300ksps (AS1531)
- Software-Configurable Analog Input Types:
  - 8-Channel Single-Ended
  - 8-Channel Pseudo Differential Referenced to COM
  - 4-Channel Pseudo Differential
  - 4-Channel Fully Differential
- Software-Configurable Input Range
- Internal +2.5V Reference
- Low-Current Operation:
  - 2.8mA @ 400ksps (AS1530)
  - 2.2mA @ 300ksps (AS1531)
  - 0.4mA in Reduced-Power Mode
  - 0.5µA in Full Power-Down Mode
- SPI/QSPI/Microwire/TMS320-Compatible
- 20-pin TSSOP Package

3 Applications

The devices are ideal for remote sensors, data-acquisition and data-logging devices, pen-digitizers, process control, or any other space-limited A/D application with low power-consumption requirements.

Figure 1. Block Diagram and Pin Assignments



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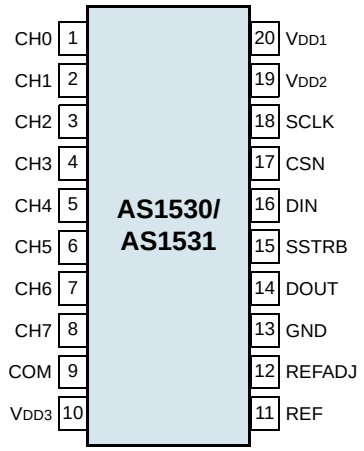
4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1:8	CH0:CH7	**Analog Sampling Inputs.** These eight pins serve as analog sampling inputs.
9	COM	**Common Analog Inputs**. Tie this pin to ground in single-ended mode.
10	V_{DD3}	**Positive Supply Voltage**
11	REF	**Reference-Buffer Output/A/DC Reference Input**. This pin serves as the reference voltage for analog-to-digital conversions. In internal reference mode, the reference buffer provides a +2.50V nominal output, externally adjustable at pin REFADJ. In external reference mode, disable the internal buffer by pulling pin REFADJ to V_{DD1}.
12	REFADJ	**Reference-Buffer Amplifier Input**. To disable the reference-buffer amplifier, tie this pin to V_{DD1}.
13	GND	**Analog and Digital Ground**
14	DOUT	**Serial Data Output**. Data is clocked out at the rising edge of pin SCLK. DOUT is high impedance when CSN is high.
15	SSTRB	**Serial Strobe Output**. SSTRB pulses high for one clock period before the MSB is clocked out. SSTRB is high impedance when CSN is high.
16	DIN	**Serial Data Input**. Data is clocked in at the rising edge of SCLK.
17	CSN	**Active-Low Chip Select**. Data will not be clocked into pin DIN unless CSN is low. When CSN is high, pins DOUT and SSTRB are high impedance.
18	SCLK	**Serial Clock Input**. This pin clocks data into and out of the serial interface, and is used to set the conversion speed. **Note:** The duty cycle must be between 40 and 60%.
19	V_{DD2}	**Positive Supply Voltage**
20	V_{DD1}	**Positive Supply Voltage**

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
V_{DD1}, V_{DD2}, V_{DD3} to GND	-0.3	+7	V	
V_{DD1} to V_{DD2} to V_{DD3}	-0.3	+0.3	V	
CH0:CH7, COM to GND	-0.3	V_{DD1} + +0.3	V	
REF, REFADJ to GND	-0.3	V_{DD1} + +0.3	V	
DIN, SCLK, CSN, to GND	-0.3	V_{DD2} + +0.3	V	
DOUT, SSTRB to GND	-0.3	V_{DD2} + +0.3	V	
DOUT, SSTRB Sink Current		25	mA	
Continuous Power Dissipation (T_{AMB} = +70ºC)		559	mW	Derate 7.0mW/ºC above +70ºC
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-60	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

AS1530 Electrical Characteristics

V_{DD1} = V_{DD2} = V_{DD3} = +4.5 to +5.5V, COM = GND, f_{SCLK}= 6.4MHz, 50% duty cycle, 16 clocks/conversion cycle (400ksps), external +2.5V at REF, REFADJ = V_{DD1}, T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified). Typ values at T_{AMB} = +25ºC.

Table 3. AS1530 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy [1]						
	Resolution		12			Bits
INL	Relative Accuracy [2]		-1		+1	LSB
DNL	Differential Nonlinearity	No missing codes over temperature	-1		+1	LSB
	Offset Error		-6		+6	LSB
	Gain Error [3]		-6		+6	LSB
	Gain-Error Temperature Coefficient			±1.6		ppm/ °C
	Channel-to-Channel Offset Error Matching			±0.2		LSB
Dynamic Specifications: 100kHz sinewave input, 2.5Vp-p, 400ksps, 6.4MHz clock, bit RANGE (page 15) = 0, pseudo-differential input mode						
SINAD	Signal-to-Noise plus Distortion Ratio			70		dB
THD	Total Harmonic Distortion	Up to the 5th harmonic		-82		dB
SFDR	Spurious-Free Dynamic Range			83		dB
IMD	Intermodulation Distortion	f_{IN1} = 99kHz, f_{IN2} = 102kHz		76		dB
	Channel-to-Channel Crosstalk [4]	f_{IN} = 200kHz, V_{IN} = 2.5Vp-p		-85		dB
	Full-Power Bandwidth	-3dB point		6		MHz
	Full-Linear Bandwidth	SINAD > 68dB		450		kHz
Conversion Rate						
t_{CONV}	Conversion Time [5]		2.5			µs
t_{ACQ}	Track/Hold Acquisition Time				390	ns
t_{AD}	Aperture Delay			7		ns
t_{AJ}	Aperture Jitter			<50		ps
f_{SCLK}	Serial Clock Frequency		0.5		6.4	MHz
	Duty Cycle		40		60	%
Analog Inputs: CH0:CH7, COM						
V_{CHx} - V_{CHy} (COM)	Input Voltage Range: Single-Ended, Pseudo-Differential, and Differential [6]	Bit RANGE (page 15) = 1	0		V_{REF}	V
		Bit RANGE (page 15) = 0	-V_{REF} /2		+V_{REF} /2	
	Multiplexer Leakage Current	On/off leakage current, V_{CHx} = 0 or V_{DD1}	-1	±0.001	+1	µA
	Input Capacitance			18		pF
Internal Reference						
V_{REF}	REF Output Voltage	T_{AMB} = +25ºC	2.48	2.50	2.52	V
	REF Short-Circuit Current			30		mA
T_{CVREF}	REF Output Temperature Coefficient			±25		ppm/ °C
	Load Regulation [7]	0 to 1mA output load		1.2	4.0	mV/ mA
C_{BYPREF}	Capacitive Bypass at REF		4.7		10	µF

Table 3. AS1530 Electrical Characteristics (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$C_{BYPREF ADJ}$	Capacitive Bypass at REFADJ			0.01		10	µF
	REFADJ Output Voltage				1.22		V
	REFADJ Input Range	For small adjustments, from 1.22V			±100		mV
	REFADJ Buffer Disable Threshold	To power down the internal reference		1.4		V_{DD1} - 1	V
	Buffer Voltage Gain				2.045		V/V
External Reference: Reference buffer disabled, reference applied to pin REF							
	REF Input Voltage Range [8]			1.0		V_{DD1} + 50mV	V
	REF Input Current	V_{REF} = 2.50V, f_{SCLK} = 6.4MHz			200	350	µA
		V_{REF} = 2.50V, f_{SCLK} = 0				320	
		Power-Down, f_{SCLK} = 0				5	
Digital Inputs: DIN, SCLK, CSN							
V_{INH}	Input High Voltage			0.7 x V_{DD}			V
V_{INL}	Input Low Voltage					0.3 x V_{DD}	V
V_{HYST}	Input Hysteresis				0.2		V
I_{IN}	Input Leakage	V_{IN} = 0 or V_{DD2}		-1		+1	µA
C_{IN}	Input Capacitance				5		pF
Digital Outputs: DOUT, SSTRB							
V_{OL}	Output Voltage Low	I_{SINK} = 5mA				0.45	V
V_{OH}	Output Voltage High	I_{SOURCE} = 1mA		4			V
I_L	Tri-State Leakage Current	CSN = V_{DD2}		-10		+10	µA
C_{OUT}	Tri-State Output Capacitance	CSN = V_{DD2}			5		pF
Power Supply							
V_{DD1}, V_{DD2}, V_{DD3}	Positive Supply Voltage [9]			4.5		5.5	V
I_{VDD1}, I_{VDD2}, I_{VDD3}	Supply Current	V_{DD1} = V_{DD2} = V_{DD3} = 5.5V	Normal Operation with External Reference [10]		2.8	3.3	mA
			Normal Operation with Internal Reference [10]		3.3	3.8	
			Reduced-Power Mode [11]		0.4	0.8	
			Full Power-Down Mode		0.5	2	µA
PSR	Power-Supply Rejection	V_{DD1} = V_{DD2} = V_{DD3} = 5V ±10%		-2	±0.1	+2	mV

1. Tested at V_{DD1} = V_{DD2} = V_{DD3} = +5V, COM = GND, bit RANGE (page 15) = 1, single-ended input mode.
2. Relative accuracy is the deviation of the analog value at any code from its theoretical value after the gain error and offset error have been nulled.
3. Offset nulled.
4. Ground on channel; sinewave applied to all off channels.
5. Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
6. The absolute voltage range for the analog inputs (CH0:CH7, and COM) is from GND to V_{DD1}.
7. External load should not change during conversion for specified accuracy. Guaranteed specification of 4mV/mA is a result of production test limitations.
8. AS1530/AS1531 performance is limited by the device noise floor, typically 300µVp-p.

9. Electrical characteristics are guaranteed from $V_{DD1(MIN)}$ = $V_{DD2(MIN)}$ = $V_{DD3(MIN)}$ to $V_{DD1(MAX)}$ = $V_{DD2(MAX)}$ = $V_{DD3(MAX)}$. For operations beyond this range, see Typical Operating Characteristics on page 11. For guaranteed specifications beyond the limits, contact austriamicrosystems, AG.
10. AIN = mid-scale; bit RANGE (page 15) = 1; tested with 20pF on DOUT, 20pF on SSTRB, and f_{SCLK} = 6.4MHz @ GND to V_{DD2}.
11. SCLK = DIN = GND, CSN = V_{DD2}.

AS1531 Electrical Characteristics

V_{DD1} = V_{DD2} = V_{DD3} = +2.7 to +3.6V, COM = GND, f_{SCLK} = 4.8MHz, 50% duty cycle, 16 clocks/conversion cycle (300ksps), external +2.5V at REF, REFADJ = V_{DD1}, T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified). Typ values at T_{AMB} = +25ºC.

Table 4. AS1531 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy [1]						
	Resolution		12			Bits
INL	Relative Accuracy [2]		-1		+1	LSB
DNL	Differential Nonlinearity	No missing codes over temperature	-1		+1	LSB
	Offset Error		-6		+6	LSB
	Gain Error [3]		-6		+6	LSB
	Gain-Error Temperature Coefficient			±1.6		ppm/°C
	Channel-to-Channel Offset Error Matching			±0.2		LSB
Dynamic Specifications: 75kHz sinewave input, 2.5Vp-p, 300ksps, 4.8MHz clock, bit RANGE (page 15) = 0, pseudo-differential input mode						
SINAD	Signal-to-Noise plus Distortion Ratio			70		dB
THD	Total Harmonic Distortion	Up to the 5th harmonic		-81		dB
SFDR	Spurious-Free Dynamic Range			84		dB
IMD	Intermodulation Distortion	f_{IN1} = 73kHz, f_{IN2} = 77kHz		76		dB
	Channel-to-Channel Crosstalk [4]	f_{IN} = 150kHz, V_{IN} = 2.5Vp-p		-80		dB
	Full-Power Bandwidth	-3dB point		6		MHz
	Full-Linear Bandwidth	SINAD > 68dB		350		kHz
Conversion Rate						
t_{CONV}	Conversion Time [5]	Normal operation	3.3			µs
t_{ACQ}	Track/Hold Acquisition Time	Normal operation			520	ns
t_{AD}	Aperture Delay			7		ns
t_{AJ}	Aperture Jitter			<50		ps
f_{SCLK}	Serial Clock Frequency	Normal operation	0.5		4.8	MHz
	Duty Cycle		40		60	%
Analog Inputs: CH0:CH7, COM						
V_{CHx} - V_{CHy} (COM)	Input Voltage Range: Single-Ended, Pseudo-Differential, and Differential [6]	Bit RANGE (page 15) = 1	0		V_{REF}	V
		Bit RANGE (page 15) = 0	-V_{REF}/2		+V_{REF}/2	
	Multiplexer Leakage Current	On/off leakage current, V_{CHx} = 0 or A_{VDD}	-1	±0.001	+1	µA
	Input Capacitance			18		pF
Internal Reference						
V_{REF}	REF Output Voltage	T_{AMB} = +25°C	2.48	2.50	2.52	V
	REF Short-Circuit Current			30		mA

Table 4. AS1531 Electrical Characteristics (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
T_{CVREF}	REF Output Temperature Coefficient				±25		ppm/°C
	Load Regulation [7]	0 to 0.75mA output load			0.6	2.0	mV/mA
C_{BYPREF}	Capacitive Bypass at REF			4.7		10	µF
$C_{BYPREF\ ADJ}$	Capacitive Bypass at REFADJ			0.01		10	µF
	REFADJ Output Voltage				1.22		V
	REFADJ Input Range	For small adjustments, from 1.22V			±100		mV
	REFADJ Buffer Disable Threshold	To power down the internal reference		1.4		V_{DD1} - 1	V
	Buffer Voltage Gain				2.045		V/V
External Reference: Reference buffer disabled, reference applied to REF							
	REF Input Voltage Range [8]			1.0		V_{DD1} + 50mV	V
	REF Input Current	V_{REF} = 2.50V, f_{SCLK}= 4.8MHz			200	350	µA
		V_{REF} = 2.50V, f_{SCLK} = 0				320	
		In power-down, f_{SCLK} = 0				5	
Digital Inputs: DIN, SCLK, CSN							
V_{INH}	Input High Voltage			0.7 x V_{DD}			V
V_{INL}	Input Low Voltage					0.3 x V_{DD}	V
V_{HYST}	Input Hysteresis				0.8		V
I_{IN}	Input Leakage	V_{IN} = 0 or V_{DD2}		-1		+1	µA
C_{IN}	Input Capacitance				5		pF
Digital Outputs: DOUT, SSTRB							
V_{OL}	Output Voltage Low	I_{SINK} = 5mA				0.45	V
V_{OH}	Output Voltage High	I_{SOURCE} = 0.5mA		V_{DD2} - 0.5V			V
I_L	Tri-State Leakage Current	CSN = V_{DD2}		-10		+10	µA
C_{OUT}	Tri-State Output Capacitance	CSN = V_{DD2}			5		pF
Power Supply							
V_{DD1}, V_{DD2}, V_{DD3}	Positive Supply Voltage [9]			2.7		3.6	V
I_{VDD1}, I_{VDD2}, I_{VDD3}	Supply Current	V_{DD1} = V_{DD2} = V_{DD3} = 5.5V	Normal Operation with External Reference [10]		2.2	2.7	mA
			Normal Operation with Internal Reference [10]		2.7	3.2	
			Reduced-Power Mode [11]		0.4	0.8	
			Full Power-Down Mode [11]		0.5	2	µA
PSR	Power-Supply Rejection		V_{DD1} = V_{DD2} = V_{DD3} = 2.7 to 3.6V, Mid-Scale Input	-2	±0.1	+2	mV

1. Tested at V_{DD1} = V_{DD2} = V_{DD3} = +3V; COM = GND; bit RANGE (page 15) = 1, single-ended input mode.

2. Relative accuracy is the deviation of the analog value at any code from its theoretical value after the gain error and offset error have been nulled.
3. Offset nulled.
4. Ground on channel; sinewave applied to all off channels.
5. Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
6. The absolute voltage range for the analog inputs (CH0:CH7, and COM) is from GND to V_{DD1}.
7. External load should not change during conversion for specified accuracy. Guaranteed specification of 2mV/mA is a result of production test limitations.
8. AS1530/AS1531 performance is limited by the device noise floor, typically 300µVp-p.
9. Electrical characteristics are guaranteed from $V_{DD1(MIN)}$ = $V_{DD2(MIN)}$ = $V_{DD3(MIN)}$ to $V_{DD1(MAX)}$ = $V_{DD2(MAX)}$ = $V_{DD3(MAX)}$. For operations beyond this range, see Typical Operating Characteristics on page 11. For guaranteed specifications beyond the limits, contact austriamicrosystems, AG.
10. AIN = mid-scale; bit RANGE (page 15) = 1; tested with 20pF on DOUT, 20pF on SSTRB, and f_{SCLK} = 4.8MHz @ GND to V_{DD2}.
11. SCLK = DIN = GND, CSN = V_{DD2}.

Timing Characteristics

Table 5. AS1530 Timing Characteristics – (Figures 3, 4, 21, 23; V_{DD1} = V_{DD2} = V_{DD3} = +4.5 to +5.5V; T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CP}	SCLK Period		156			ns
t_{CH}	SCLK Pulse Width High		62			ns
t_{CL}	SCLK Pulse Width Low		62			ns
t_{DS}	DIN to SCLK Setup		35			ns
t_{DH}	DIN to SCLK Hold		0			ns
t_{CSS}	CSN Fall to SCLK Rise Setup		35			ns
t_{CS0}	SCLK Rise to CSN Fall Ignore		35			ns
t_{DOH}	SCLK Rise to DOUT Hold	C_{LOAD} = 20pF	10	20		ns
t_{STH}	SCLK Rise to SSTRB Hold	C_{LOAD} = 20pF	10	20		ns
t_{STV}	SCLK Rise to DOUT Valid	C_{LOAD} = 20pF			80	ns
t_{DOV}	SCLK Rise to SSTRB Valid	C_{LOAD} = 20pF			80	ns
t_{DOD}	CSN Rise to DOUT Disable	C_{LOAD} = 20pF	10		65	ns
t_{STD}	CSN Rise to SSTRB Disable	C_{LOAD} = 20pF	10		65	ns
t_{DOE}	CSN Fall to DOUT Enable	C_{LOAD} = 20pF			65	ns
t_{STE}	CSN Fall to SSTRB Enable	C_{LOAD} = 20pF			65	ns
t_{CSW}	CSN Pulse Width High		100			ns

Table 6. AS1531 Timing Characteristics – (Figures 3, 4, 21, 23; V_{DD1} = V_{DD2} = V_{DD3} = +2.7 to +3.6V; T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CP}	SCLK Period		208			ns
t_{CH}	SCLK Pulse Width High		83			ns
t_{CL}	SCLK Pulse Width Low		83			ns
t_{DS}	DIN to SCLK Setup		45			ns
t_{DH}	DIN to SCLK Hold		0			ns
t_{CSS}	CSN Fall to SCLK Rise Setup		45			ns
t_{CS0}	SCLK Rise to CSN Fall ignore		45			ns
t_{DOH}	SCLK Rise to DOUT Hold	C_{LOAD} = 20pF	13	20		ns
t_{STH}	SCLK Rise to SSTRB Hold	C_{LOAD} = 20pF	13	20		ns

Table 6. AS1531 Timing Characteristics – (Figures 3, 4, 21, 23; V_{DD1} = V_{DD2} = V_{DD3} = +2.7 to +3.6V; T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified). (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DOV}	SCLK Rise to DOUT Valid	C_{LOAD} = 20pF			100	ns
t_{STV}	SCLK Rise to SSTRB Valid	C_{LOAD} = 20pF			100	ns
t_{DOD}	CSN Rise to DOUT Disable	C_{LOAD} = 20pF	13		85	ns
t_{STD}	CSN Rise to SSTRB Disable	C_{LOAD} = 20pF	13		85	ns
t_{DOE}	CSN Fall to DOUT Enable	C_{LOAD} = 20pF			85	ns
t_{STE}	CSN Fall to SSTRB Enable	C_{LOAD} = 20pF			85	ns
t_{CSW}	CSN Pulse Width High		100			ns

Figure 3. DOUT Enable-Time Load Circuits

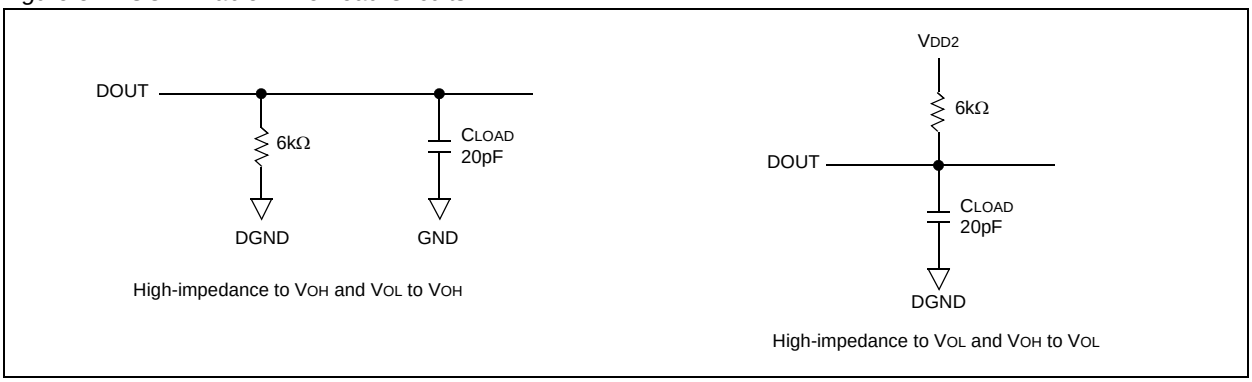
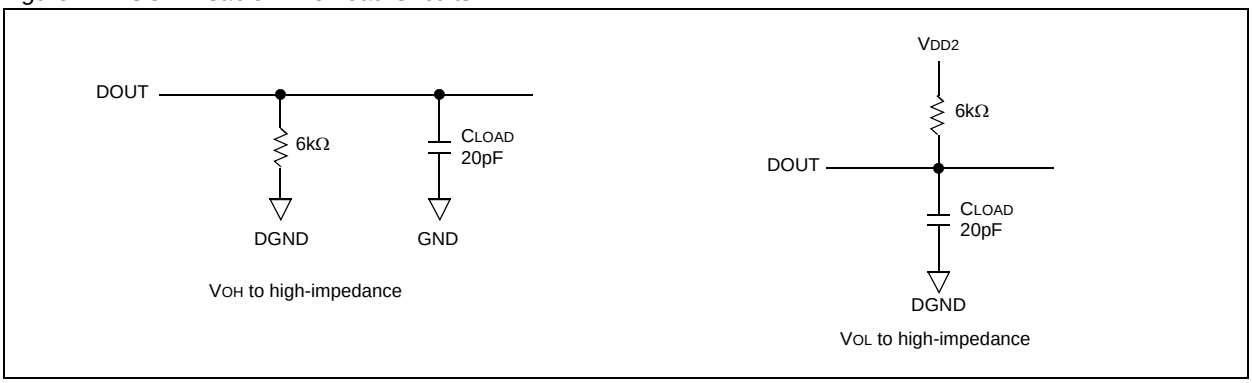


Figure 4. DOUT Disable-Time Load Circuits



7 Typical Operating Characteristics

Same conditions as stated in Electrical Characteristics on page 5.

Figure 5. INL vs. Digital Output Code

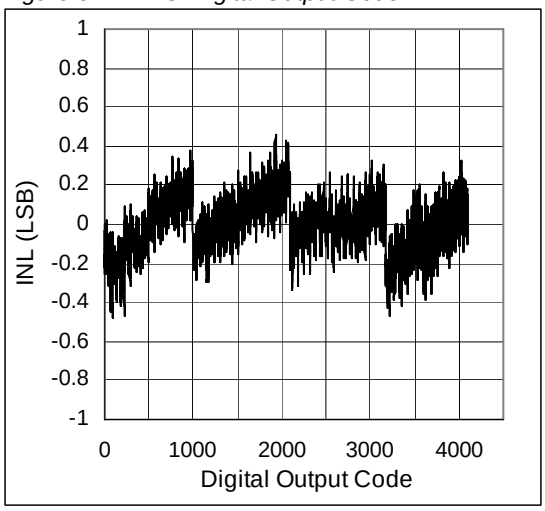


Figure 6. DNL vs. Digital Output Code

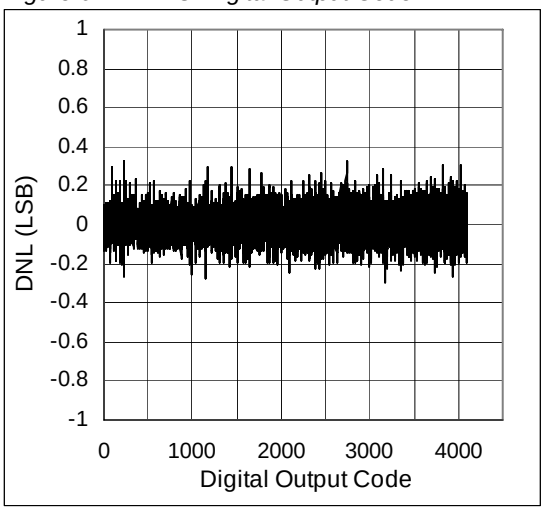


Figure 7. FFT @ 10kHz; RANGE = 1, MODE = 1

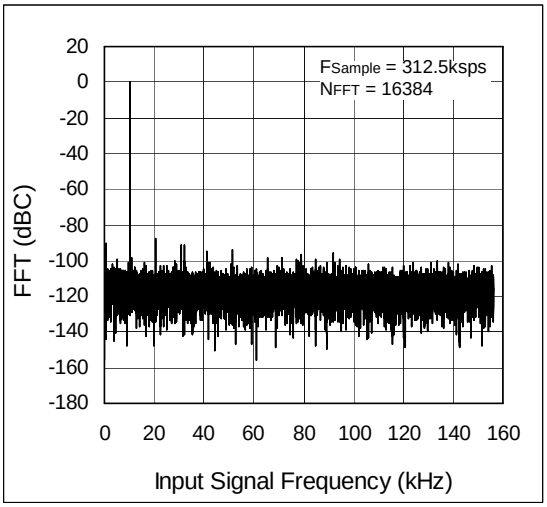


Figure 8. FFT @ 75kHz; RANGE = 0, MODE = 1

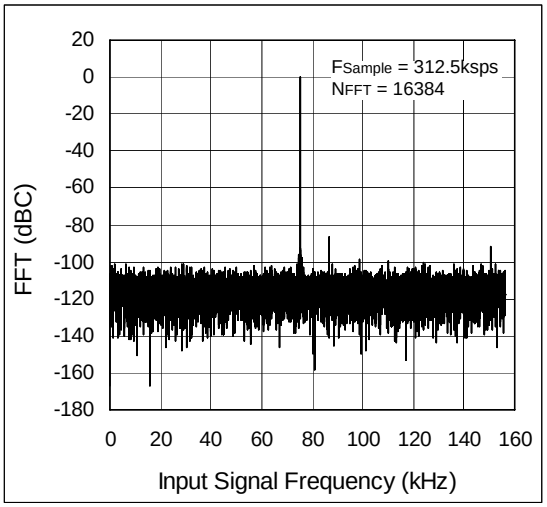


Figure 9. ENOB vs. V_{REF}; 1st Order 300kHz Low Pass Filter

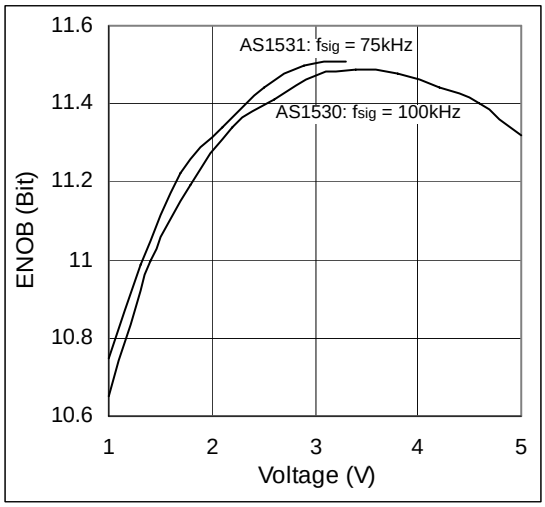


Figure 10. ENOB vs. Input Signal Frequency; 1st Order 1MHz Low Pass Filter

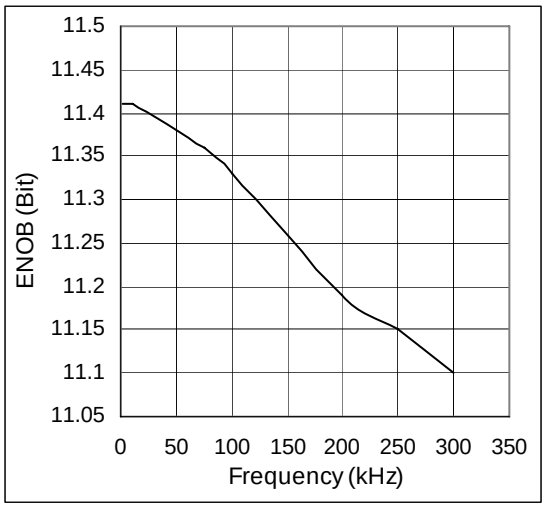


Figure 11. IVDD vs. VDD (Static)

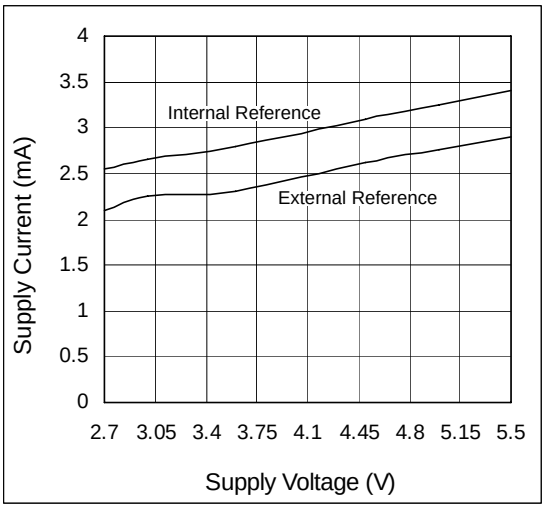


Figure 12. IVDD vs. Temperature; Internal Reference

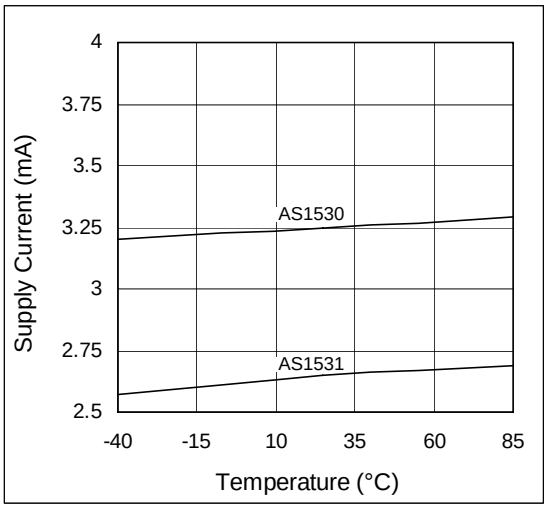


Figure 13. IVDD vs. VDD (Converting)

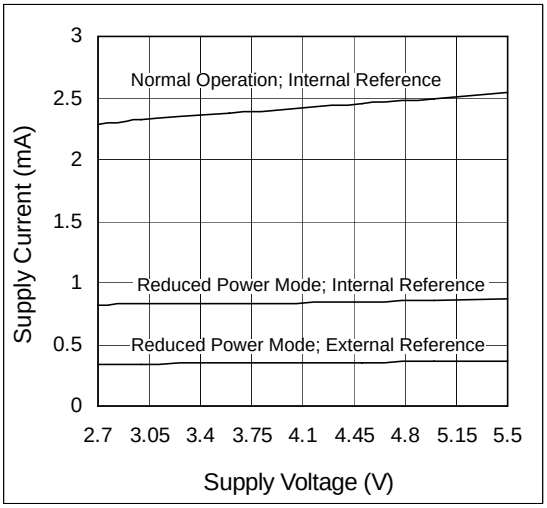


Figure 14. IVDD vs. Temperature (Static)

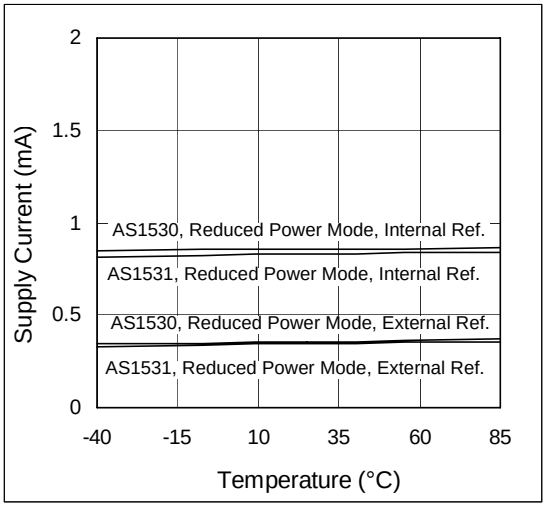


Figure 15. VREF vs. Temperature

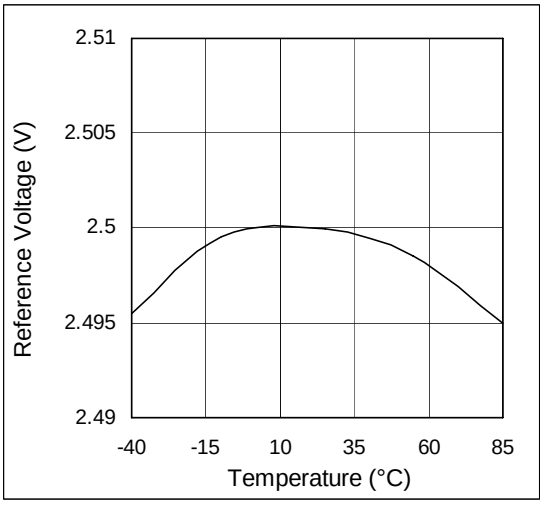


Figure 16. Offset Error vs. Temperature

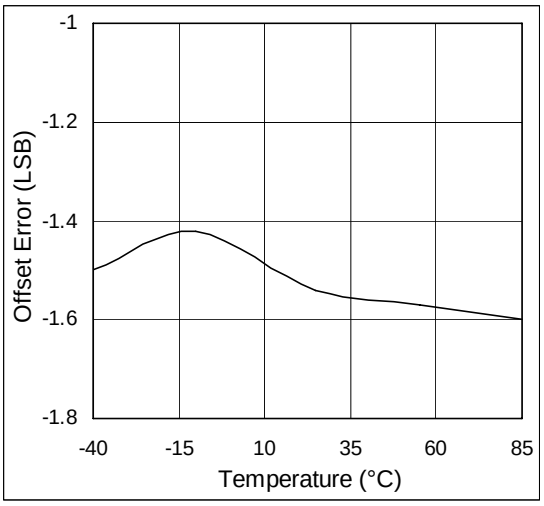


Figure 17. Offset Error vs. V_{DD}

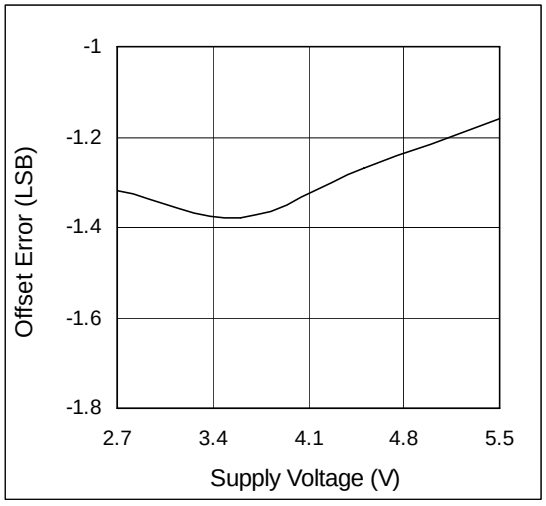


Figure 18. Gain Error vs. Temperature

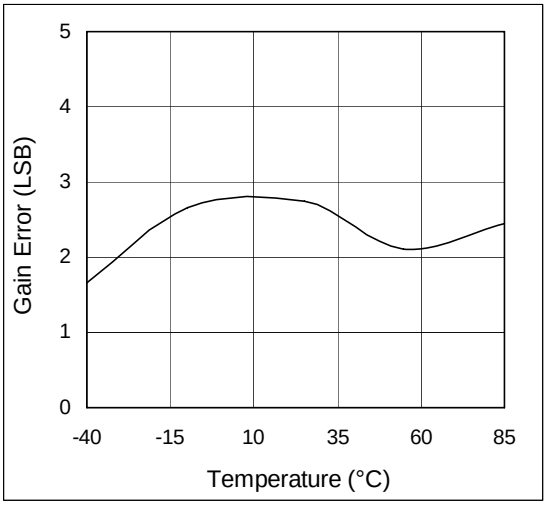
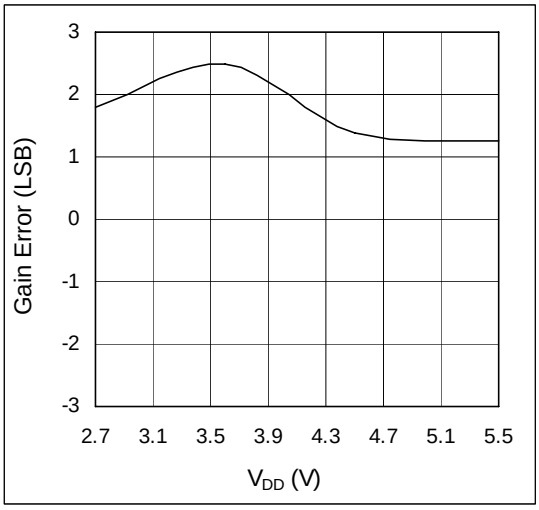


Figure 19. Gain Error vs. V_{DD}

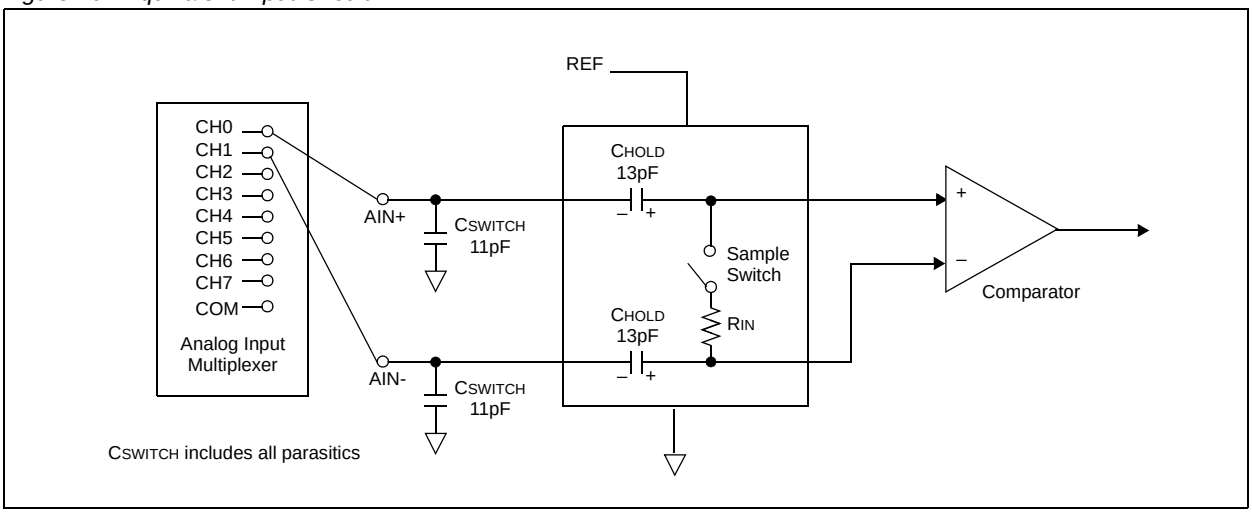


8 Detailed Description

Analog Input

The equivalent input circuit (Figure 20) shows the input architecture: track/hold circuitry, input multiplexer, input comparator, switched-capacitor DAC, and internal reference. A flexible serial interface provides easy connections to various microprocessors.

Figure 20. Equivalent Input Circuit



The input tracking circuitry has a 6MHz small-signal bandwidth, thus it is possible to under-sample (digitize high-speed transient events) and measure periodic signals modulated at frequencies exceeding the AS1530/AS1531 sampling rate.

Note: To avoid high-frequency signals being aliased into the frequency band of interest, antialias filtering is recommended

Input Protection

Internal protection diodes (which clamp the analog input to V_{DD1} and GND) allow the channel inputs to swing from (GND to 0.3V) to (V_{DD1} + 0.3V) without damaging the devices. However, for accurate conversions near full scale, the inputs must not exceed V_{DD1} by more than 50mV or be lower than GND by 50mV.

Note: If the analog input exceeds 50mV beyond the supply voltage, do not allow the input current to exceed 2mA.

Track/Hold

The track/hold stage enters tracking mode on the rising edge of SCLK which clocks in bit MODE of the 8-bit control byte (see Figure 21 on page 17). The track/hold stage enters hold mode on the falling clock edge after bit PD0 of the 8-bit control byte has been shifted in.

The time required for the track/hold circuit to acquire an input signal is a function of how quickly the input capacitance is charged. If the input signal source impedance is high, the acquisition time lengthens. The acquisition time (t_{ACQ}) is the maximum time the device takes to acquire the signal and is also the minimum time needed for the signal to be acquired.

t_{ACQ} is never less than 390ns (AS1530) or 520ns (AS1531), and is calculated by:

$$tACQ = 9(RS + RIN)18pF \qquad (EQ\ 1)$$

Where::

R_{IN} = 800Ω
R_S = the source impedance of the input signal.

Note: Source impedances below 2kΩ do not significantly affect the AC performance of the devices.

Control Register

The control register on the AS1530/AS1531 is a 8-bit, write-only register. Data is written to this register using the CSN, DIN and SCLK pins. The control register format is shown in Table 7 and the function of the bits are defined in Table 8.

The AS1530/AS1531 operating modes are selected by sending an 8-bit data word to the internal shift register via pin DIN. After pin CSN is pulled low, the first logic 1 on pin DIN is interpreted as a start bit. A start bit is defined as one of the following:

- The first logic 1 bit clocked into pin DIN (with CSN low) any time the AS1530/AS1531 is idle, e.g., after V_{DD1} and V_{DD2} are applied.
- The first logic 1 bit clocked into pin DIN after bit 6 of a conversion in progress is clocked out of pin DOUT.

Figure 22 on page 17 shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles. If CSN is tied low and SCLK is continuous, guarantee a start bit by first clocking in sixteen 0s. The fastest speed at which the devices can operate is 16 clocks per conversion (with CSN held low between conversions).

Table 7. Control Byte Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
START (MSB)	SEL2	SEL1	SEL0	RANGE	MODE	PD1	PD0 (LSB)

Table 8. Bit Descriptions

Bit	Name	Description
7	START	The first logic 1 bit after CSN goes low signifies the start of a control byte.
6:4	SEL2:SEL0	These three bits select which of the eight channels and pin COM are used for the conversion (see Table 10 and Table 11).
3	RANGE	This bit selects the analog input range of the AS1530/AS1531. 0 = The analog input range extends from $-V_{REF}/2$ to $+V_{REF}/2$. 1= The analog input range extends from 0V to V_{REF}.
2	MODE	This bit in conjunction with bit RANGE changes the analog input configuration. 0 = The voltage difference between two selectable channels is converted. This setting selects two's complement coding (see Table 10 on page 16 and Table 11 on page 16). 1 = One of the eight input channels is referenced to COM. This setting also selects binary coding.
1:0	PD1:PD0	Selects the AS1530/AS1531 operating mode: **PD1 PD0 Mode** 0 0 Full power-down mode. 0 1 Reduced-power mode. 1 0 Reduced-power mode. 1 1 Normal operation.

Analog Input Configuration

Table 9. Analog Input Configuration

Analog Input Configuration	Mode	Range	Coding	Comments
8-Channel Single-Ended	1	1	Binary	AIN+ from 0 to V_{REF}. COM should be tied to GND.
8-Channel Pseudo Differential referenced to COM	1	1	Binary	AIN+ from COM to COM + V_{REF}
8-Channel Pseudo Differential referenced to COM	1	0	Binary	AIN+ from $-V_{REF}/2$+COM to + $V_{REF}/2$+COM
4-Channel Pseudo Differential	0	1	Two's Complement	AIN+ - AIN- from 0 to V_{REF}
4-Channel Pseudo Differential	0	0	Two's Complement	AIN+ - AIN- from $-V_{REF}/2$ to $+V_{REF}/2$
4-Channel Fully Differential	0	0	Two's Complement	AIN+ - AIN- from $-V_{REF}/2$ to $+V_{REF}/2$, fully differential input signal.

Channel Selection

Depending on the setting of bit MODE (page 15), the internal inputs of the ADC (AIN+ and AIN-) are connected differently to the input channels (CH0:CH7 and COM).

Single-Ended Input

Table 10. Input Channel Selection for MODE = 1

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	AIN+								AIN-
0	0	1			AIN+						AIN-
0	1	0					AIN+				AIN-
0	1	1							AIN+		AIN-
1	0	0		AIN+							AIN-
1	0	1				AIN+					AIN-
1	1	0						AIN+			AIN-
1	1	1								AIN+	AIN-

Note: In single-ended mode pin COM should be connected to GND pin.

Differential Input

Table 11. Input Channel Selection for MODE = 0

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	AIN+	AIN-						
0	0	1			AIN+	AIN-				
0	1	0					AIN+	AIN-		
0	1	1							AIN+	AIN-
1	0	0	AIN-	AIN+						
1	0	1			AIN-	AIN+				
1	1	0					AIN-	AIN+		
1	1	1							AIN-	AIN+

Starting a Conversion

A conversion is started by clocking a control byte into pin DIN.

With CSN low, each rising edge on SCLK clocks a bit from DIN into the internal shift register, starting with the MSB. A conversion will only start when a logic 1 is written to the START bit of the 8-bit control register.

Figure 21. Single Conversion Timing Waveforms

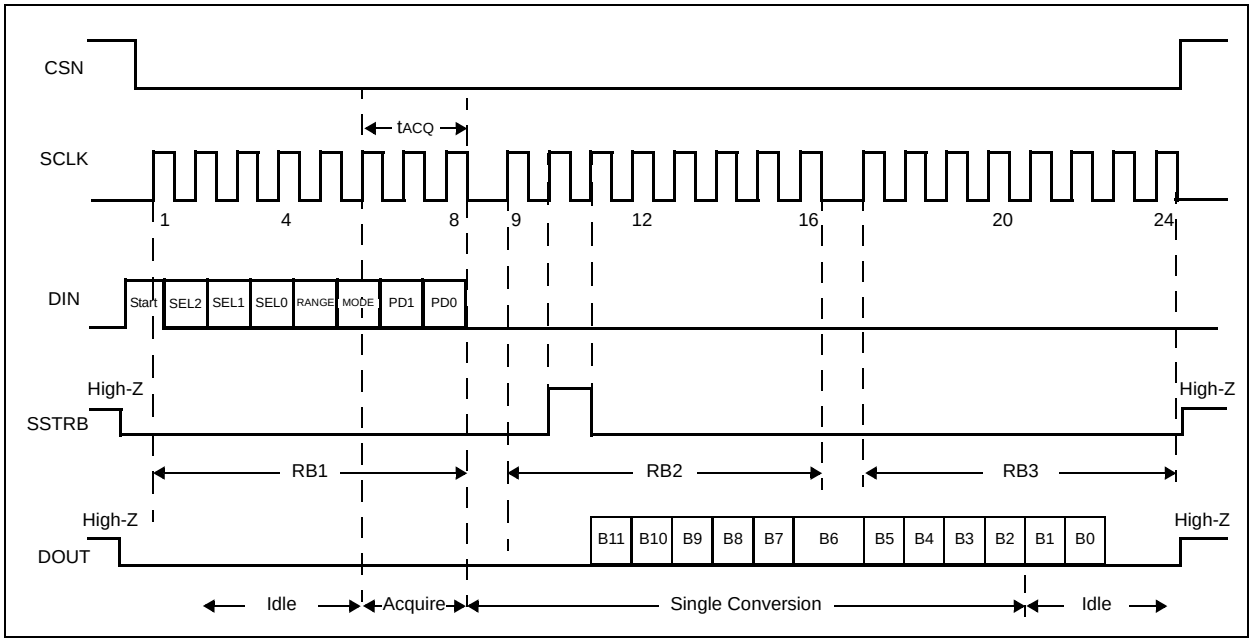


Figure 22. Continuous 16-Clock Conversion Timing Waveforms

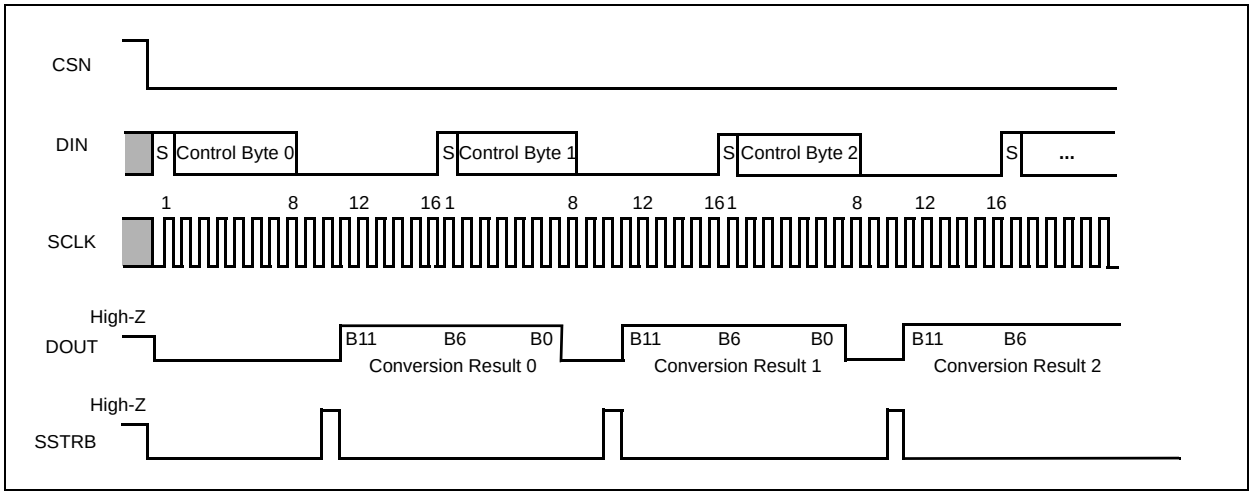
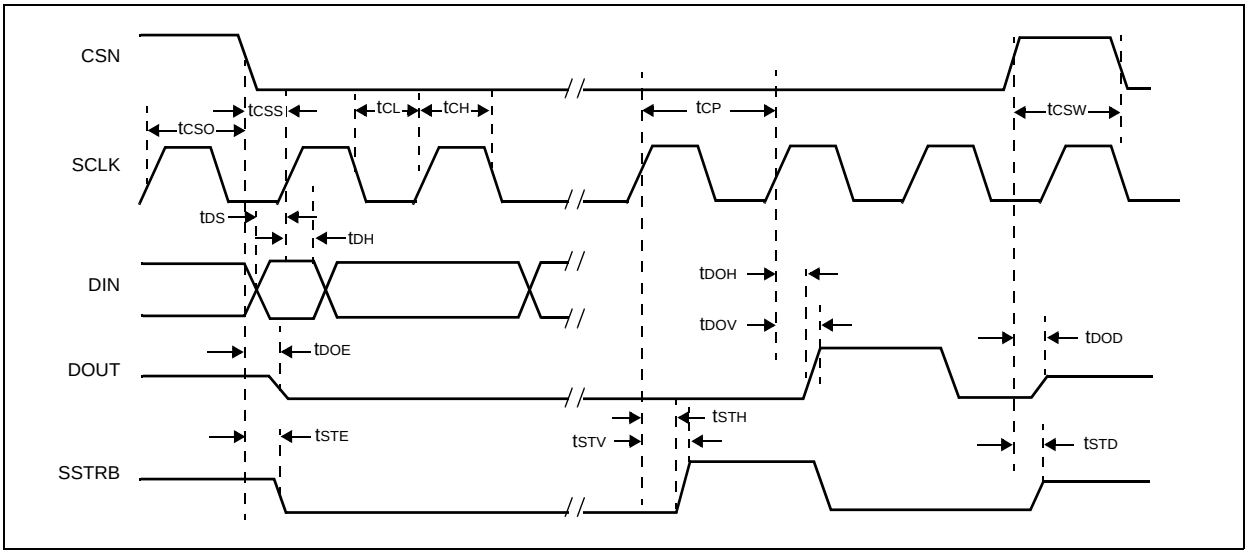


Figure 23. Detailed Serial Interface Timing Waveforms



The external serial clock shifts data in and out of the devices and drives the analog-to-digital conversion steps. Two clock periods after the last bit of the control byte is written the output pin SSTRB pulses high for one clock period.

The serial data is shifted out at DOUT on each of the next 12 SCLK rising edges (see Figure 21 on page 17).

Pins SSTRB and DOUT go into a high-impedance state when CSN goes high. The conversion must complete in 120µs or less, or consequently, droop on the sample-and-hold capacitors may degrade conversion results. Figure 23 shows detailed serial-interface timing waveforms.

Transfer Functions

Output coding and transfer function depend on the control register bits MODE (page 15) and RANGE (page 15).

Figure 24. Straight Binary Transfer Function for RANGE = 1 and MODE = 1

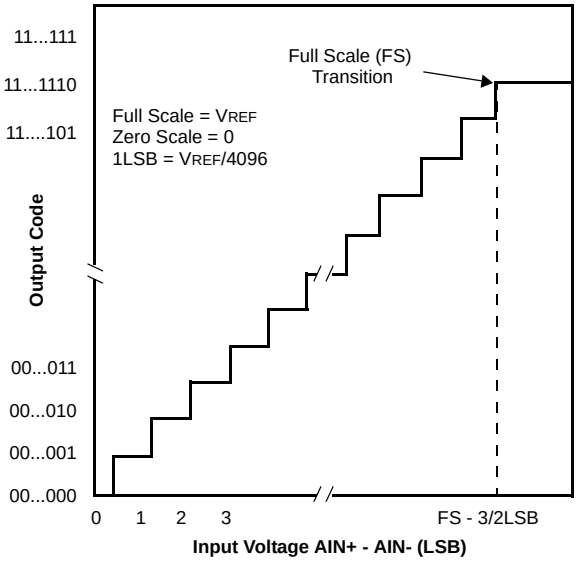


Figure 25. Straight Binary Transfer Function for RANGE = 0 and MODE = 1

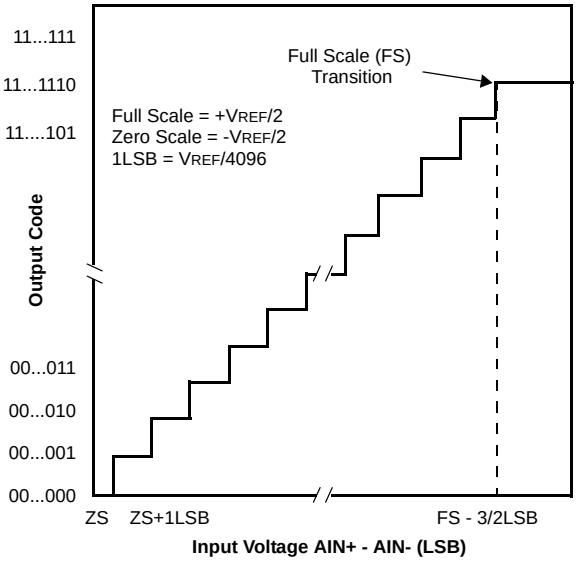


Figure 26. Two's Complement Transfer Function for RANGE = 1 and MODE = 0

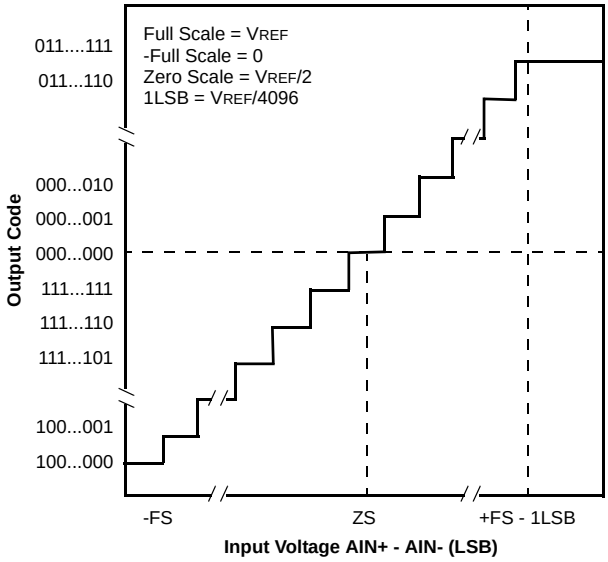
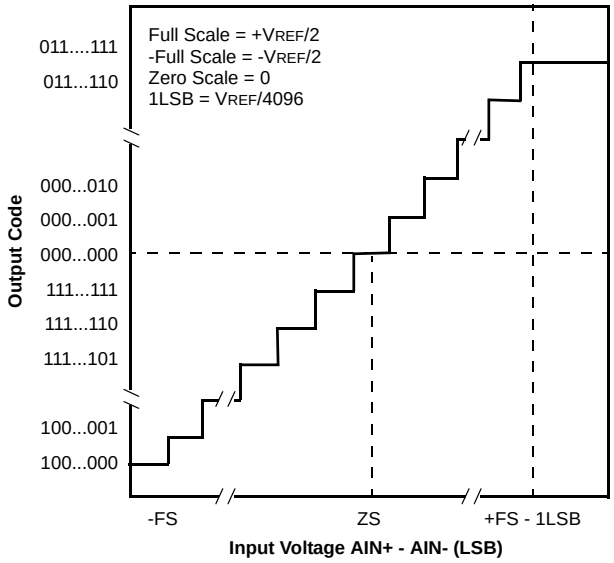


Figure 27. Two's Complement Transfer Function for RANGE = 0 and MODE = 0



Power Modes

Power consumption can be reduced by placing the AS1530/AS1531 in reduced power mode or in full power-down mode between conversions.

The power mode is selected using bits PD1 and PD0 of the 8-bit control byte.

Table 12 lists the three operating modes with the corresponding supply current and active device circuits. For data rates achievable in full power-down mode see Full Power-Down Mode on page 20.

Table 12. Software Controlled Power Modes

PD1/PD0 (page 23)	Mode	Total Supply Current				Device Circuits *	
		During Conversion		After Conversion		Input Comparator	Reference
		AS1530	AS1531	AS1530	AS1531		
00	Full Power-Down Mode	2.8mA	2.2mA	0.5µA	0.5µA	Off	Off
01	Reduced-Power Mode	2.8mA	2.2mA	0.4mA	0.4mA	Reduced Power	On
10							
11	Normal Operation	2.8mA	2.2mA	2.0mA	1.8mA	Full Power	On

* Circuit operation between conversions; during conversion all circuits are fully powered up.

The selected power-down mode (as shown in Table 12) is initiated after an analog-to-digital conversion is completed.

In all power modes the serial interface remains active, waiting for a new control byte to start conversion (see Figure 30 on page 21). Once the conversion is completed, the AS1530/AS1531 goes into the selected power mode until a new control byte is shifted in. In reduced power mode the AS1530/AS1531 will be able to start conversion immediately when running at decreased clock rates. In full power down mode wait until the internal reference has stabilized (dependant on the values of the capacitance of REF and REFADJ).

During initialization the AS1530/AS1531 immediately go into normal operation mode and are ready to convert after 4µs when using an external reference. When using the internal reference, wait until the internal reference has stabilized (dependant on the values of the capacitance of REF and REFADJ).

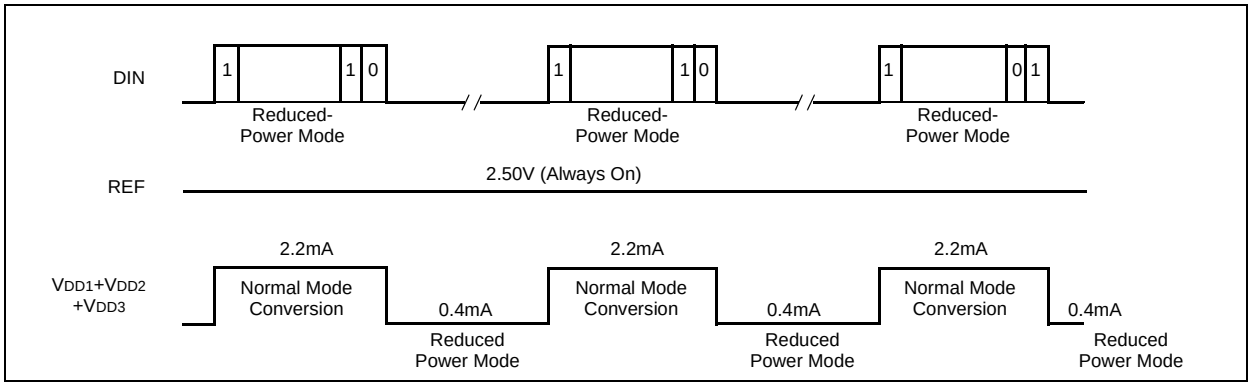
Reduced Power Mode

Reduced power mode is activated using bits PD1 and PD0 (see Table 12). When reduced power mode is asserted, the AS1530/AS1531 completes any conversion in progress and enters reduced power mode.

The next start of conversion puts the AS1530/AS1531 into normal operation mode. The 8-bit control byte shifted into the control register determines the next power mode. For example, if the 8-bit control byte contains PD1 = 0 and PD0 = 1, reduced power mode starts immediately after the conversion (see Figure 28).

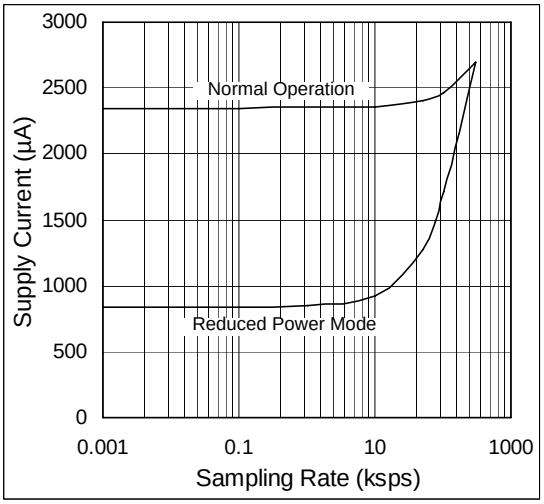
The reduced-power mode achieves the lowest power consumption at speeds close to the maximum sample rate. Figure 29 shows the AS1531 power consumption in reduced-power mode and normal operating mode (see Table 12 on page 19) with the internal reference and maximum clock speed.

Figure 28. Reduced-Power Mode Timing Waveforms (AS1531)



Note: The clock speed in reduced-power mode should be limited to 4.8MHz. Full power-down mode may provide increased power savings in applications where the devices are inactive for long periods of time, where intermittent bursts of high-speed conversions are required.

Figure 29. Normal Operation and Reduced Power Mode using Internal Reference (AS1531)



Full Power-Down Mode

Full power-down is activated using bits PD1 and PD0 (see Table 12). Full power-down mode offers the lowest power consumption at up to 1000 conversions per-channel per-second. When full power-down is asserted, the AS1530/AS1531 completes any conversion in progress and powers down into specified low-quiescent current state.

The start of the next conversion puts the AS1530/AS1531 into normal operation mode. The 8-bit control byte shifted into the control register determines the next power mode. For example, if the 8-bit control byte contains PD1 = 0 and PD0 = 0, full power-down mode starts immediately after the conversion (see Figure 30 on page 21)

A 0.01µF bypass capacitor plus the internal 17kΩ reference resistor at REFADJ form an R/C filter with a 170µs time constant. To achieve full 12-bit accuracy, 9 time constants (1.8ms) are required after power-up if the bypass capacitor is fully discharged between conversions. Waiting this 1.8ms in reduced-power mode instead of normal operation mode can further reduce power consumption. This is achieved by using the sequence shown in Figure 30 on page 21.

Figure 31 on page 21 shows the AS1531 power consumption for conversions using full power-down mode (PD1 = PD0 = 0 (see Table 12), an external reference, and the maximum clock speed. One dummy conversion to power-up the device is required, but no wait-time is necessary to start the second conversion, thereby achieving lower power consumption up to the full sampling rate.

Figure 30. Full Power-Down Timing Waveforms (AS1531)

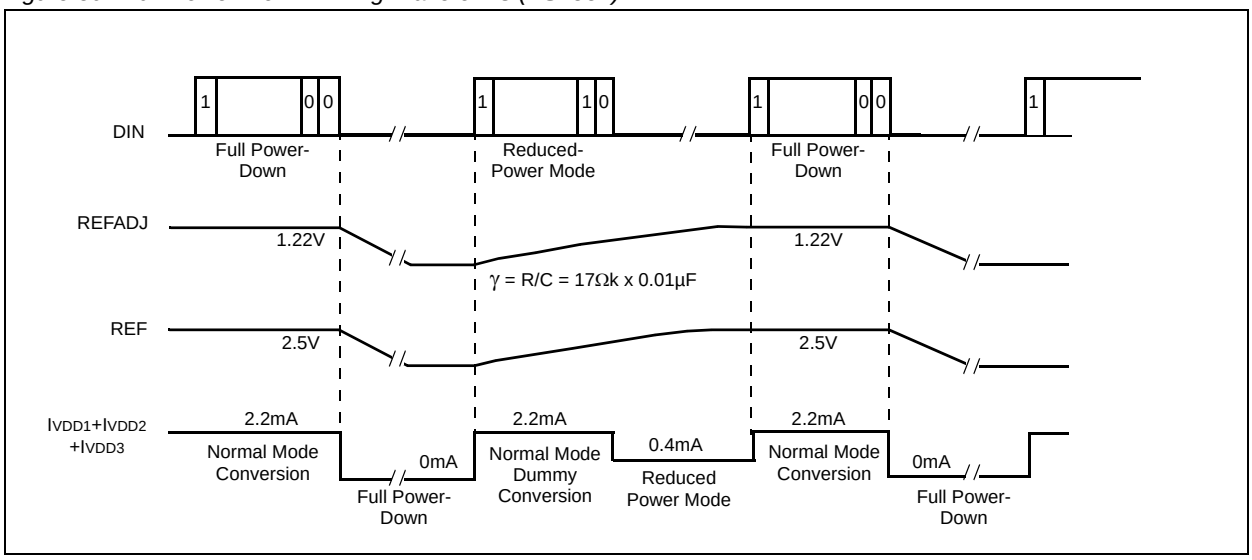
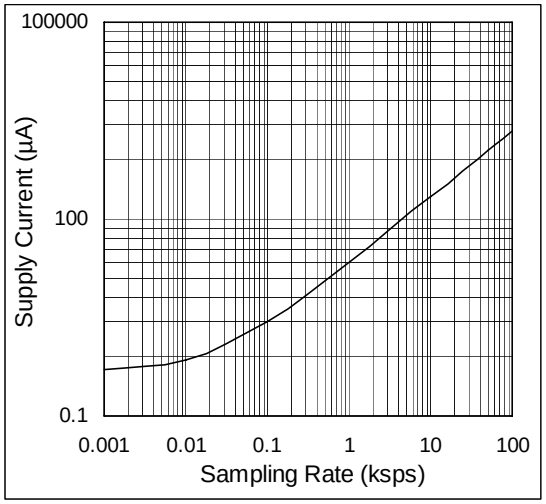


Figure 31. Average Supply Current vs. Sampling Rate (AS1531, FULLPD, and External Reference)



Reference

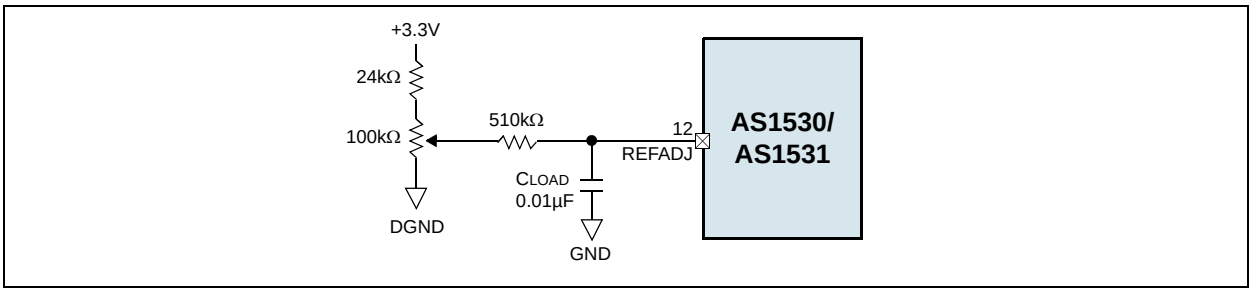
The AS1530/AS1531 can operate with the internal or an external reference.

Internal Reference

The internal reference is selected by placing a capacitor between REFADJ and GND. The internally trimmed 1.22V bandgap voltage available at REFADJ is buffered with a gain of 2.045V/V to pin REF, where 2.5V are available. A decoupling capacitor is needed at pin REF.

Additionally the bandgap voltage can be adjusted about ±100mV by forcing a voltage to the REFADJ pin. The REFADJ input impedance is typically 17kΩ. Figure 32 shows a possible arrangement.

Figure 32. Reference Adjust Circuit



External Reference

An external reference can be connected directly at pin REF. To use the external reference, the internal buffer must be disabled by connecting pin REFADJ to pin VDD. The input resistance is typically 15kΩ.

During conversion, an external reference at pin REF must deliver up to 350µA DC load current and have 10Ω or less output impedance. If the reference has a higher output impedance or is noisy, bypass it with a 4.7µF capacitor placed as close to pin REF as possible.

Note: Using the REFADJ input makes buffering the external reference unnecessary.

9 Application Information

Initialization

When power is first applied to the AS1530/AS1531 internal power-on reset circuitry sets the devices for normal operation. At this point, the devices can perform data conversions with CSN held low.

Note: The device requires 10µs after the power supplies stabilize; no conversions should be initiated during this time.

The digital output at pin DOUT will be all 0s until an analog-to-digital conversion is initiated.

Serial Interface

The AS1530/AS1531 fully support SPI, QSPI, and Microwire interfaces. For SPI, select the correct clock polarity and sampling edge in the SPI control registers (set CPOL = 0 and CPHA = 0).

Note: Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time.

Using the circuit shown in Figure 33 on page 24, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the AS1530/AS1531, and two more 8-bit transfers to clock out the 12-bit conversion result).

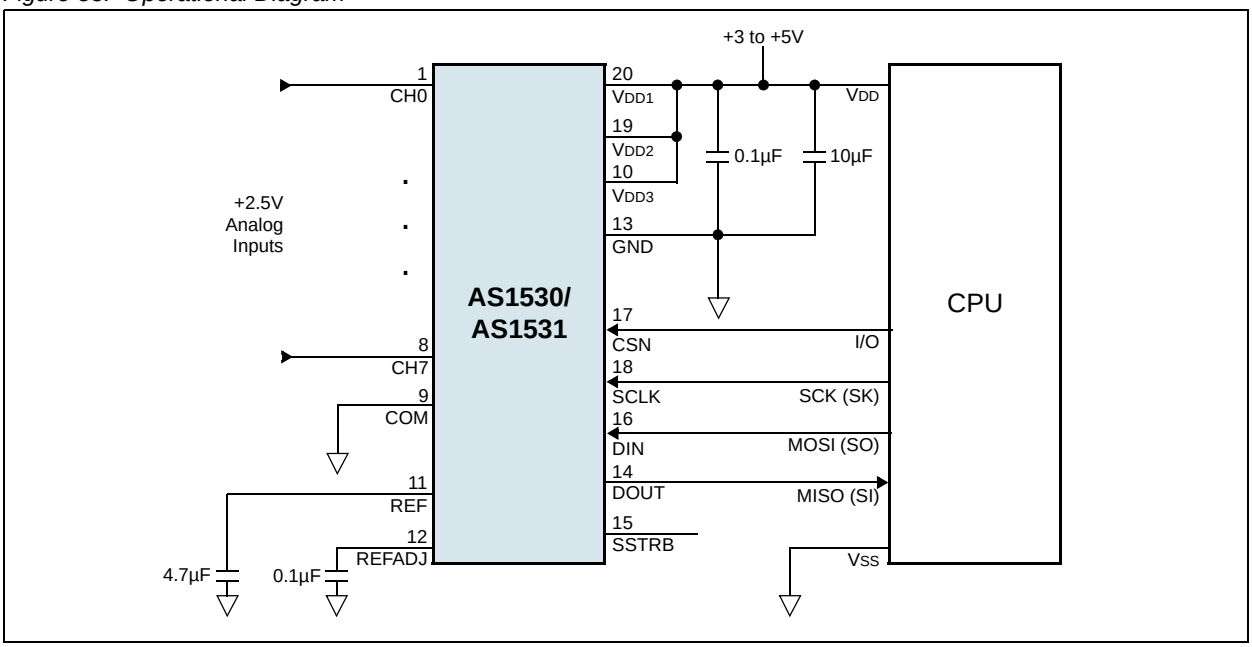
Serial Interface Configuration

The following steps describe how to configure the serial interface:

1. Confirm that the CPU serial interface is in master mode (so the CPU generates the serial clock).
2. Choose a clock frequency from 500kHz to 6.4MHz (AS1530) or 4.8MHz (AS1531).
3. Set up the control byte and call it TB1. TB1 should be in the format 1XXXXXXX binary, where the Xs indicate the selected channel, conversion mode, and power mode.
4. Use a general-purpose I/O line on the CPU to pull CSN low.
5. Transmit TB1 and simultaneously receive a byte (RB1). Ignore this byte.
6. Transmit a byte of all zeros ($00h) and simultaneously receive byte RB2.
7. Transmit a byte of all zeros ($00h) and simultaneously receive byte RB3.
8. Pull CSN high.

Bytes RB2 and RB3 (see Figure 21 on page 17) contain the results of the conversion, padded with three leading zeros and one trailing zero. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive track/hold droop, make sure the total conversion time does not exceed 120µs.

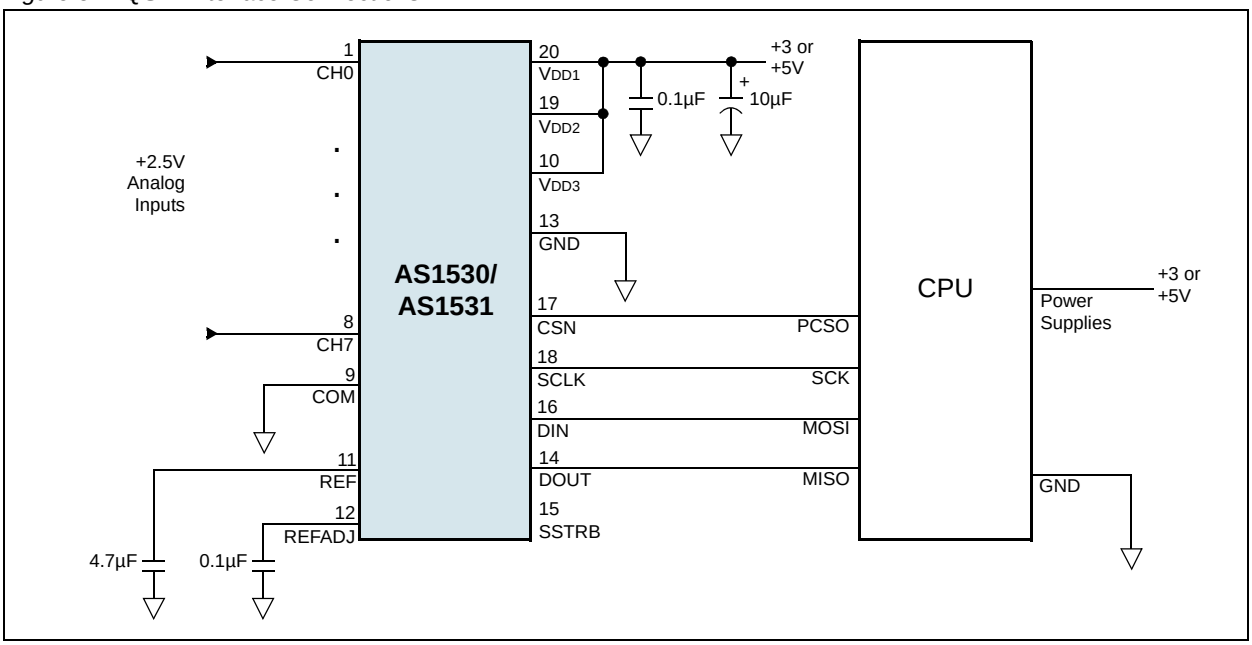
Figure 33. Operational Diagram



QSPI Interface

The AS1530/AS1531 can interface with QSPI using the circuit in Figure 34 (f_{SCLK} = 4.0MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without affecting CPU performance, since QSPI incorporates a micro-sequencer.

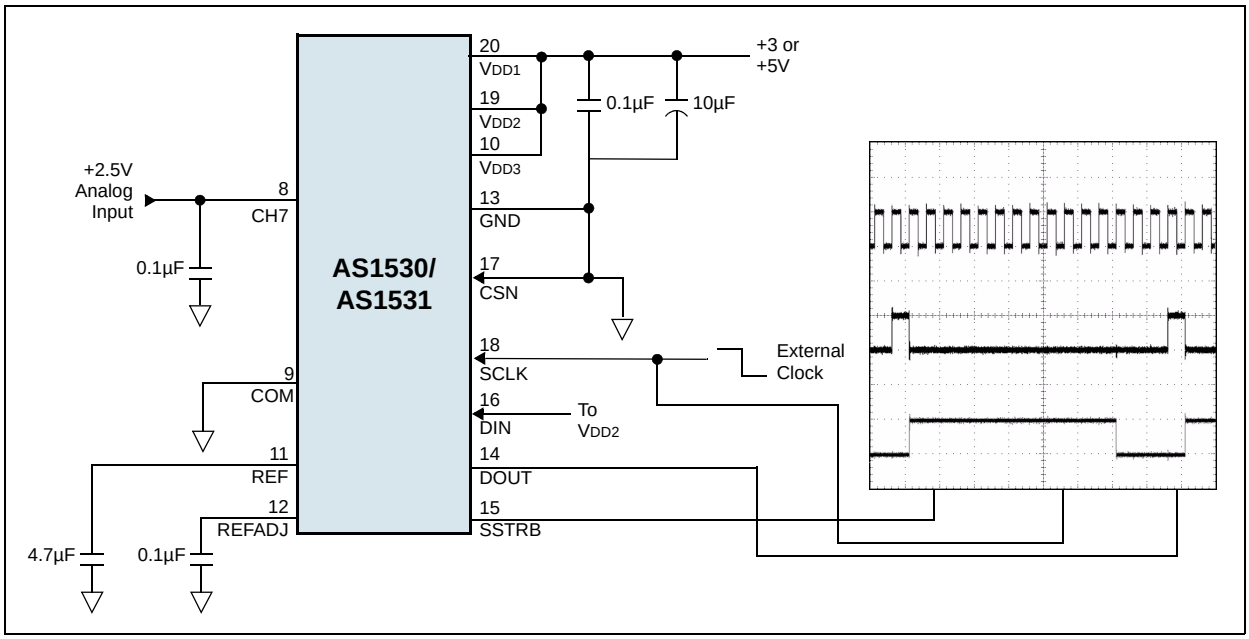
Figure 34. QSPI Interface Connections



Quick Evaluation Circuit

In order to quickly evaluate the analog performance of the AS1530/AS1531, use the circuit shown in Figure 35.

Figure 35. Evaluation Circuit Diagram



Connecting DIN to V_{DD2} shifts in control bytes of $FFh, which trigger single-ended conversions (bit RANGE (page 15) = 1) on CH7 without powering down between conversions. The SSTRB output pulses high for one clock period before the MSB of the 12-bit conversion result is shifted out of DOUT. Varying the analog input to CH7 will alter the sequence of bits from DOUT. A total of 16 clock cycles is required per conversion.

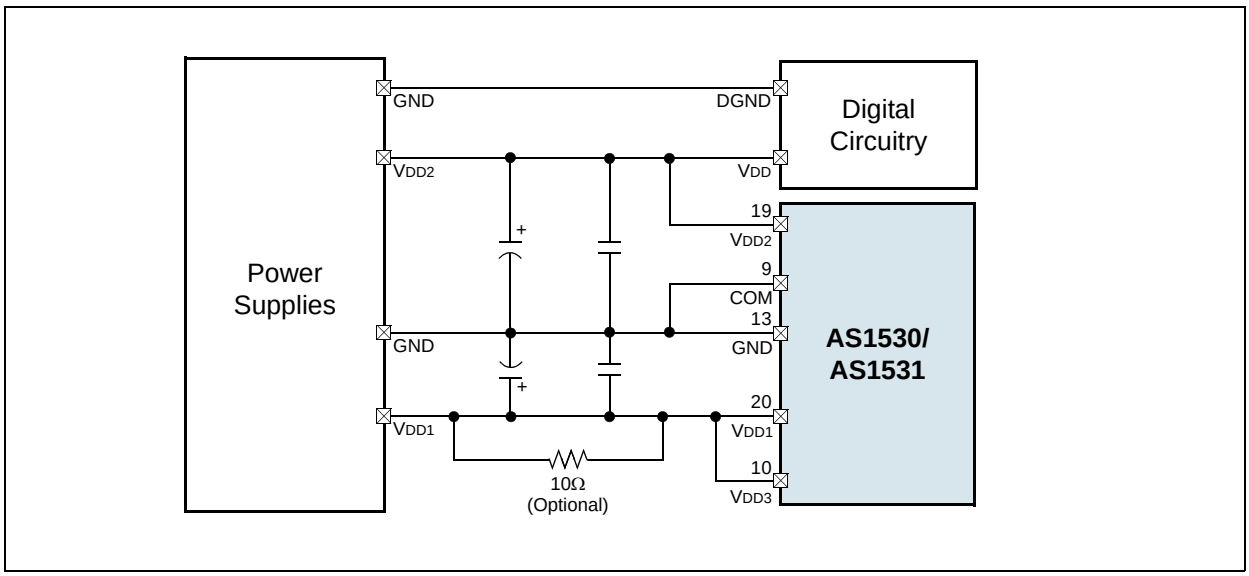
Note: All SSTRB and DOUT output transitions occur 25ns (typ) after the rising edge of SCLK.

Layout Considerations

The AS1530/AS1531 require proper layout and design procedures for optimum performance.

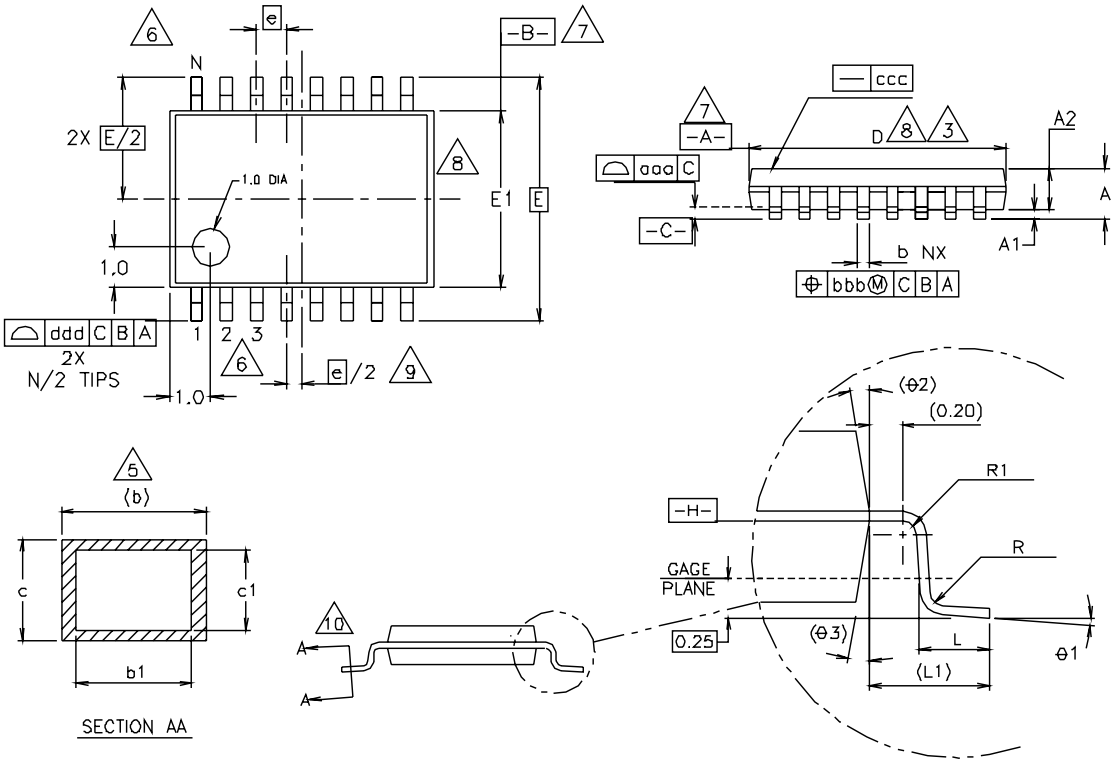
- Use printed circuit boards; wirewrap boards should not be used.
- Analog and digital traces should be separate and should not run parallel to each other (especially clock traces).
- Digital traces should not run beneath the AS1530/AS1531.
- Use a single-point analog ground at GND, separate from the digital ground (see Figure 36). Connect all other analog grounds and DGND to this star ground point for further noise reduction. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.
- High-frequency noise in the V_{DD} power supply may affect the AS1530/AS1531 high-speed comparator. Bypass this supply to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors. Bypass capacitors should be as close to the device as possible for optimum power supply noise-rejection. If the power supply is very noisy, a 10Ω resistor can be connected as a low-pass filter to attenuate supply noise (see Figure 36).

Figure 36. Recommended GND Design



10 Package Drawings and Markings

Figure 37. 20-pin TSSOP Package



Notes:

1. All dimensions are in millimeters; angles in degrees.
2. Dimensioning and tolerancing per *ASME Y14.5M – 1994*.
3. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15mm per side.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.
6. Terminal numbers are for reference only.
7. Datums A and B to be determined at datum plane H.
8. Dimensions D and E1 are to be determined at datum plane H.
9. This dimension applies only to variations with an even number of leads per side.
10. Cross section A-A to be determined at 0.10 to 0.25mm from the leadtip.

Symbol	Min	Typ	Max	Notes
A	-	-	1.10	1,2
A1	0.05	-	0.15	1,2
A2	0.85	0.90	0.95	1,2
L	0.50	0.60	0.75	1,2
R	0.09	-	-	1,2
R1	0.09	-	-	1,2
b	0.19	-	0.30	1,2,5
b1	0.19	0.22	0.25	1,2
c	0.09	-	0.20	1,2
c1	0.09	-	0.16	1,2
θ1	0º	-	8º	1,2
L1	1.0REF			1,2
aaa	0.10			1,2
bbb	0.10			1,2
ccc	0.05			1,2
ddd	0.20			1,2
e	0.65BSC			1,2
θ2	12ºREF			1,2
θ3	12ºREF			1,2
Variations				
D	6.40	6.50	6.60	1,2,3,8
E1	4.30	4.40	4.50	1,2,4,8
E	6.4BSC			1,2
e	0.65BSC			1,2
N	20			1,2,6

11 Ordering Information

The devices are available as the standard products shown in Table 13.

Table 13. Ordering Information

Model	Description	Delivery Form	Package
AS1530-T	12-bit ADC, 8-channel, 400ksps	Tape and Reel	20-pin TSSOP
AS1530	12-bit ADC, 8-channel, 400ksps	Tubes	20-pin TSSOP
AS1531-T	12-bit ADC, 8-channel, 300ksps	Tape and Reel	20-pin TSSOP
AS1531	12-bit ADC, 8-channel, 300ksps	Tubes	20-pin TSSOP

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