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ACT™ 1 Series FPGAs

Features

- 5V and 3.3V Families fully compatible with JEDEC specifications
- Up to 2000 Gate Array Gates (6000 PLD equivalent gates)
- Replaces up to 50 TTL Packages
- Replaces up to twenty 20-Pin PAL® Packages
- Design Library with over 250 Macro Functions
- Gate Array Architecture Allows Completely Automatic Place and Route
- Up to 547 Programmable Logic Modules
- Up to 273 Flip-Flops
- Data Rates to 75 MHz
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 25 MHz
- Built-In High Speed Clock Distribution Network
- I/O Drive to 10 mA (5 V), 6 mA (3.3 V)
- Nonvolatile, User Programmable
- Fabricated in 1.0 micron CMOS technology

Description

The ACT™ 1 Series of field programmable gate arrays (FPGAs) offers a variety of package, speed, and application combinations. Devices are implemented in silicon gate, 1-micron two-level metal CMOS, and they employ Actel's PLICE® antifuse technology. The unique architecture offers gate array flexibility, high performance, and instant turnaround through user programming. Device utilization is typically 95 to 100 percent of available logic modules.

ACT 1 devices also provide system designers with unique on-chip diagnostic probe capabilities, allowing convenient testing and debugging. Additional features include an on-chip clock driver with a hardwired distribution network. The network provides efficient clock distribution with minimum skew.

The user-definable I/Os are capable of driving at both TTL and CMOS drive levels. Available packages include plastic and ceramic J-led chip carriers, ceramic and plastic quad flatpacks, and ceramic pin grid array.

A security fuse may be programmed to disable all further programming and to protect the design from being copied or reverse engineered.

Product Family Profile

| Device | A1010B A10V10B | A1020B A10V20B |
|--------------------------------|--|--|
| Capacity | | |
| Gate Array Equivalent Gates | 1,200 | 2,000 |
| PLD Equivalent Gates | 3,000 | 6,000 |
| TTL Equivalent Packages | 30 | 50 |
| 20-Pin PAL Equivalent Packages | 12 | 20 |
| Logic Modules | 295 | 547 |
| Flip-Flops (maximum) | 147 | 273 |
| Routing Resources | | |
| Horizontal Tracks/Channel | 22 | 22 |
| Vertical Tracks/Column | 13 | 13 |
| PLICE Antifuse Elements | 112,000 | 186,000 |
| User I/Os (maximum) | 57 | 69 |
| Packages: | 44 PLCC 68 PLCC 100 PQFP 80 VQFP 84 CPGA | 44 PLCC 68 PLCC 84 PLCC 100 PQFP 80 VQFP 84 CPGA 84 CQFP |
| Performance | | |
| 5 V Data Rate (maximum) | 75 MHz | 75 MHz |
| 3.3 V Data Rate (maximum) | 55 MHz | 55 MHz |

Note: See Product Plan on page 1-286 for package availability.

The Designer and Designer Advantage™ Systems

The ACT 1 device family is supported by Actel's Designer and Designer Advantage Systems, allowing logic design implementation with minimum effort. The systems offer Microsoft® Windows™ and X Windows™ graphical user interfaces and integrate with the resident CAE system to provide a complete gate array design environment: schematic capture, simulation, fully automatic place and route, timing verification, and device programming. The systems also include the ACTmap™ VHDL optimization and synthesis tool and the ACTgen™ Macro Builder, a powerful macro function generator for counters, adders, and other structural blocks.

The systems are available for 386/486/Pentium™ PC and for HP™ and Sun™ workstations and for running Viewlogic®,

Mentor Graphics®, Cadence™, OrCAD™, and Synopsys design environments.

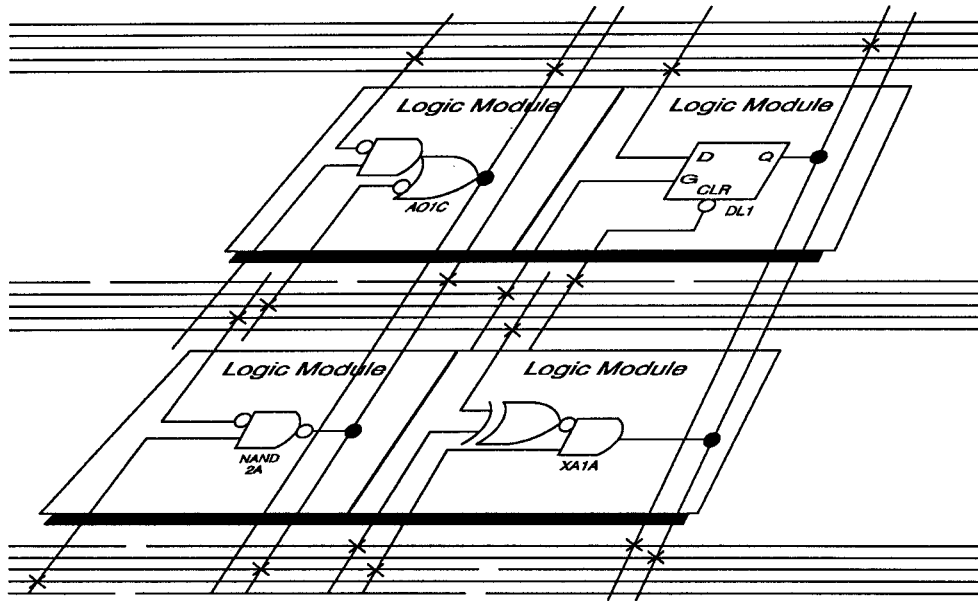


Figure 1 • Partial View of an ACT 1 Device

ACT 1 Device Structure

A partial view of an ACT 1 device (Figure 1) depicts four logic modules and distributed horizontal and vertical interconnect tracks. PLICE antifuses, located at intersections of the horizontal and vertical tracks, connect logic module inputs and outputs. During programming, these antifuses are addressed and programmed to make the connections required by the circuit application.

The ACT 1 Logic Module

The ACT 1 logic module is an 8-input, one-output logic circuit chosen for the wide range of functions it implements and for its efficient use of interconnect routing resources (Figure 2).

The logic module can implement the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function may have many versions, with different combinations of active-low inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs, and OR-ANDs. No dedicated hardwired latches or flip-flops are required in the array, since latches and flip-flops may be constructed from logic modules wherever needed in the application.

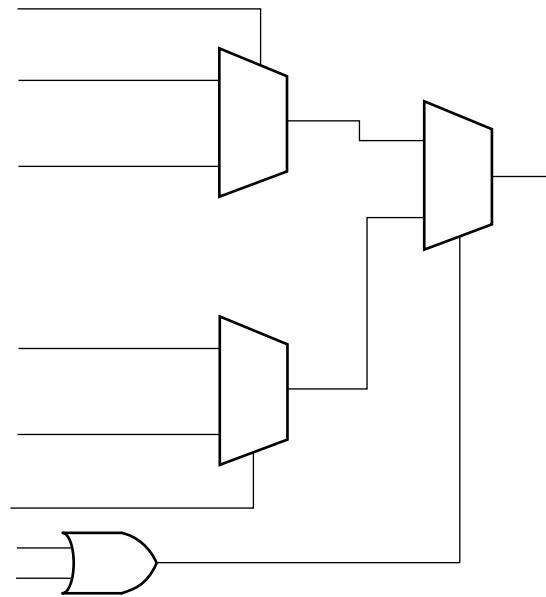


Figure 2 • ACT 1 Logic Module

I/O Buffers

Each I/O pin is available as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Outputs sink or

source 10 mA at TTL levels. See Electrical Specifications for additional I/O buffer specifications.

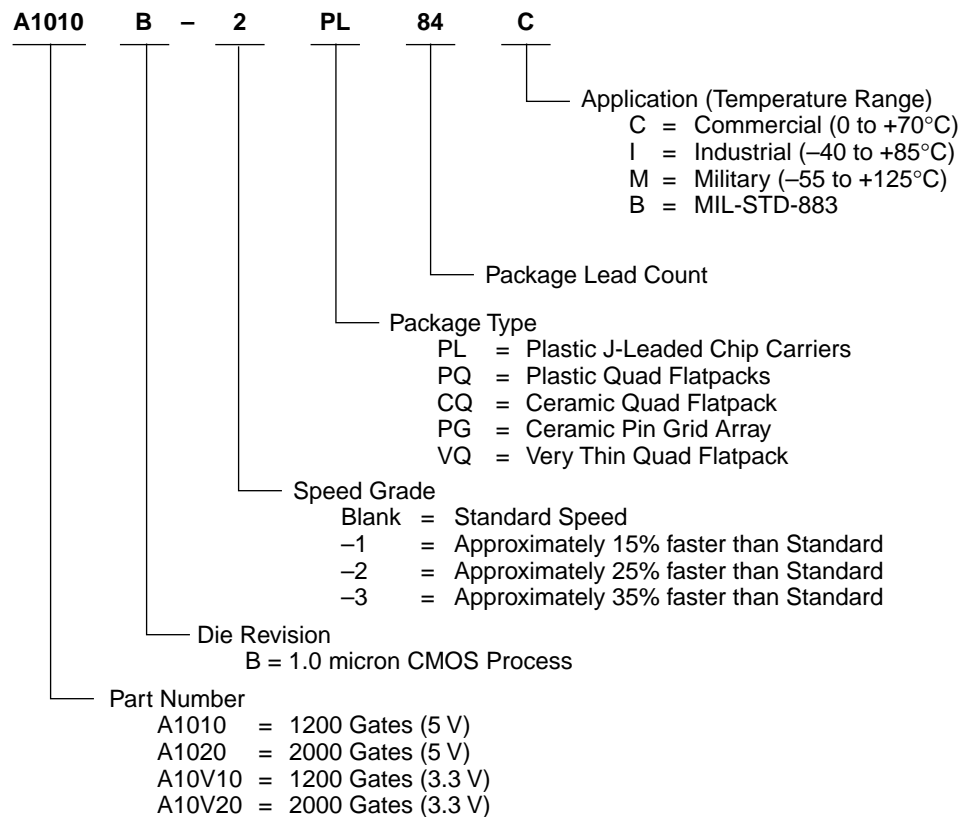
Device Organization

ACT 1 devices consist of a matrix of logic modules arranged in rows separated by wiring channels. This array is surrounded by a ring of peripheral circuits including I/O buffers, testability circuits, and diagnostic probe circuits providing real-time diagnostic capability. Between rows of logic modules are routing channels containing sets of segmented metal tracks with PLICE antifuses. Each channel has 22 signal tracks. Vertical routing is permitted via 13 vertical tracks per logic module column. The resulting network allows arbitrary and flexible interconnections between logic modules and I/O modules.

Probe Pin

ACT 1 devices have two independent diagnostic probe pins. These pins allow the user to observe any two internal signals by entering the appropriate net name in the diagnostic software. Signals may be viewed on a logic analyzer using Actel's Actionprobe® diagnostic tools. The probe pins can also be used as user-defined I/Os when debugging is finished.

Ordering Information



ACT 1 Array Performance

Temperature and Voltage Effects

Worst-case delays for ACT 1 arrays are calculated in the same manner as for masked array products. A typical delay parameter is multiplied by a derating factor to account for temperature, voltage, and processing effects. However, in an ACT 1 array, temperature and voltage effects are less dramatic than with masked devices. The electrical characteristics of module interconnections on ACT 1 devices remain constant over voltage and temperature fluctuations.

As a result, the total derating factor from typical to worst-case for a standard speed ACT 1 array is only 1.19 to 1, compared to 2 to 1 for a masked gate array.

Logic Module Size

Logic module size also affects performance. A mask programmed gate array cell with four transistors usually implements only one logic level. In the more complex logic module (similar to the complexity of a gate array macro) of an ACT 1 array, implementation of multiple logic levels within a single module is possible. This eliminates interlevel wiring and associated RC delays. The effect is termed "net compression."

Pin Description

CLK Clock (Input)

TTL Clock input for global clock distribution network. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground

Input LOW supply voltage.

I/O Input/Output (Input, Output)

I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

MODE Mode (Input)

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/O. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} Supply Voltage

Input HIGH supply voltage.

Absolute Maximum Ratings¹

Free air temperature range

| Symbol | Parameter | Limits | Units |
|------------------|--------------------------------------|------------------------------|-------|
| V _{CC} | DC Supply Voltage ² | -0.5 to +7.0 | Volts |
| V _I | Input Voltage | -0.5 to V _{CC} +0.5 | Volts |
| V _O | Output Voltage | -0.5 to V _{CC} +0.5 | Volts |
| I _{IO} | I/O Sink/Source Current ³ | ±20 | mA |
| T _{STG} | Storage Temperature | -65 to +150 | °C |

Notes:

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.
- V_{PP} = V_{CC}, except during device programming.
- Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND - 0.5 V, the internal protection diode will be forward biased and can draw excessive current.

Recommended Operating Conditions

| Parameter | Commercial | Industrial | Military | Units |
|--------------------------------|------------|------------|-------------|------------------|
| Temperature Range ¹ | 0 to +70 | -40 to +85 | -55 to +125 | °C |
| Power Supply Tolerance | ±5 | ±10 | ±10 | %V _{CC} |

Note:

- Ambient temperature (T_A) used for commercial and industrial; case temperature (T_C) used for military.

Electrical Specifications (5V)

| Symbol | Parameter | Commercial | | Industrial | | Military | | Units |
|--|-------------------------------|------------|----------------|------------|----------------|----------|----------------|---------------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| V_{OH}^1 | $(I_{OH} = -10 \text{ mA})^2$ | 2.4 | | | | | | V |
| | $(I_{OH} = -6 \text{ mA})$ | 3.84 | | | | | | V |
| | $(I_{OH} = -4 \text{ mA})$ | | | 3.7 | | 3.7 | | V |
| V_{OL}^1 | $(I_{OL} = 10 \text{ mA})^2$ | | 0.5 | | | | | V |
| | $(I_{OL} = 6 \text{ mA})$ | | 0.33 | | 0.40 | | 0.40 | V |
| V_{IL} | | -0.3 | 0.8 | -0.3 | 0.8 | -0.3 | 0.8 | V |
| V_{IH} | | 2.0 | $V_{CC} + 0.3$ | 2.0 | $V_{CC} + 0.3$ | 2.0 | $V_{CC} + 0.3$ | V |
| Input Transition Time t_R, t_F^2 | | | 500 | | 500 | | 500 | ns |
| C_{IO} I/O Capacitance ^{2, 3} | | | 10 | | 10 | | 10 | pF |
| Standby Current, I_{CC}^4 (typical = 1 mA) | | | 3 | | 10 | | 20 | mA |
| Leakage Current ⁵ | | -10 | 10 | -10 | 10 | -10 | 10 | μA |

Notes:

1. Only one output tested at a time. $V_{CC} = \text{min.}$
2. Not tested, for information only.
3. Includes worst-case 84-pin PLCC package capacitance. $V_{OUT} = 0 \text{ V}, f = 1 \text{ MHz.}$
4. Typical standby current = 1 mA. All outputs unloaded. All inputs = V_{CC} or GND.
5. $V_O, V_{IN} = V_{CC}$ or GND.

Electrical Specifications (3.3V)

| Parameter | Commercial | | Units |
|--|------------------------------|----------------|---------------|
| | Min. | Max. | |
| V_{OH}^1 | $(I_{OH} = -4 \text{ mA})$ | 2.15 | V |
| | $(I_{OH} = -3.2 \text{ mA})$ | 2.4 | V |
| V_{OL}^1 | $(I_{OL} = 6 \text{ mA})$ | 0.4 | V |
| V_{IL} | -0.3 | 0.8 | V |
| V_{IH} | 2.0 | $V_{CC} + 0.3$ | V |
| Input Transition Time t_R, t_F^2 | | 500 | ns |
| C_{IO} I/O Capacitance ^{2, 3} | | 10 | pF |
| Standby Current, I_{CC}^4 (typical = 0.3 mA) | | 0.75 | mA |
| Leakage Current ⁵ | | -10 | μA |

Notes:

1. Only one output tested at a time. $V_{CC} = \text{min.}$
2. Not tested, for information only.
3. Includes worst-case 84-pin PLCC package capacitance. $V_{OUT} = 0 \text{ V}, f = 1 \text{ MHz.}$
4. Typical standby current = 0.3 mA. All outputs unloaded. All inputs = V_{CC} or GND.
5. $V_O, V_{IN} = V_{CC}$ or GND.

Package Thermal Characteristics

The device junction to case thermal characteristics is θ_{jc} , and the junction to ambient air characteristics is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates. Maximum junction temperature is 150°C.

A sample calculation of the maximum power dissipation for an 84-pin plastic leaded chip carrier at commercial temperature is as follows:

$$\frac{\text{Max junction temp.}(\text{°C}) - \text{Max commercial temp.}(\text{°C})}{\theta_{ja}(\text{°C/W})} = \frac{150\text{°C} - 70\text{°C}}{37\text{°C/W}} = 2.2 \text{ W}$$

| Package Type | Pin Count | θ_{jc} | θ_{ja} Still Air | θ_{ja} 300 ft/min | Units |
|----------------------------------|-----------|---------------|----------------------------|-----------------------------|-------|
| Plastic J-Leaded Chip Carrier | 44 | 15 | 45 | 35 | °C/W |
| | 68 | 13 | 38 | 29 | °C/W |
| | 84 | 12 | 37 | 28 | °C/W |
| Plastic Quad Flatpack | 100 | 13 | 48 | 40 | °C/W |
| Very Thin (1.0 mm) Quad Flatpack | 80 | 12 | 43 | 35 | °C/W |
| Ceramic Pin Grid Array | 84 | 8 | 33 | 20 | °C/W |
| Ceramic Quad Flatpack | 84 | 5 | 40 | 30 | °C/W |

General Power Equation

$$P = [I_{CC\text{standby}} + I_{CC\text{active}}] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

Where:

$I_{CC\text{standby}}$ is the current flowing when no inputs or outputs are changing.

$I_{CC\text{active}}$ is the current flowing due to CMOS switching.

I_{OL} , I_{OH} are TTL sink/source currents.

V_{OL} , V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL} .

M equals the number of outputs driving TTL loads to V_{OH} .

An accurate determination of N and M is problematical because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst case conditions.

| I_{CC} | V_{CC} | Power |
|----------|----------|----------------|
| 3 mA | 5.25 V | 15.75 mW (max) |
| 1 mA | 5.25 V | 5.25 mW (typ) |
| 0.75 mA | 3.60 V | 2.70 mW (max) |
| 0.30 mA | 3.30 V | 0.99 mW (typ) |

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by the Equation 1.

$$\text{Power (uW)} = C_{EQ} * V_{CC2} * F \quad (1)$$

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{CC} active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC} . Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Actel FPGAs

| | A10V10B | A1010B |
|--|---------|--------|
| | A10V20B | A1020B |
| Modules (C_{EQM}) | 3.2 | 3.7 |
| Input Buffers (C_{EQI}) | 10.9 | 22.1 |
| Output Buffers (C_{EQO}) | 11.6 | 31.2 |
| Routed Array Clock Buffer Loads (C_{EQCR}) | 4.1 | 4.6 |

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CC}^2 * [(m * C_{EQM} * f_m)_{\text{modules}} + (n * C_{EQI} * f_n)_{\text{inputs}} + (p * (C_{EQO} + C_L) * f_p)_{\text{outputs}} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{\text{routed_Clk1}} + (r_1 * f_{q1})_{\text{routed_Clk1}}] \quad (2)$$

Where:

- m = Number of logic modules switching at f_m
- n = Number of input buffers switching at f_n
- p = Number of output buffers switching at f_p
- q_1 = Number of clock loads on the first routed array clock (All families)
- r_1 = Fixed capacitance due to first routed array clock (All families)

- C_{EQM} = Equivalent capacitance of logic modules in pF
- C_{EQI} = Equivalent capacitance of input buffers in pF
- C_{EQO} = Equivalent capacitance of output buffers in pF
- C_{EQCR} = Equivalent capacitance of routed array clock in pF
- C_L = Output lead capacitance in pF
- f_m = Average logic module switching rate in MHz
- f_n = Average input buffer switching rate in MHz
- f_p = Average output buffer switching rate in MHz
- f_{q1} = Average first routed array clock rate in MHz (All families)

Fixed Capacitance Values for Actel FPGAs (pF)

| Device Type | r_1 routed_Clk1 |
|-------------|----------------------|
| A1010B | 41.4 |
| A1020B | 68.6 |
| A10V10B | 40 |
| A10V20B | 65 |

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

| | |
|--|----------------|
| Logic Modules (m) | 90% of modules |
| Inputs switching (n) | #inputs/4 |
| Outputs switching (p) | #outputs/4 |
| First routed array clock loads (q_1) | 40% of modules |
| Load capacitance (C_L) | 35 pF |
| Average logic module switching rate (f_m) | F/10 |
| Average input switching rate (f_n) | F/5 |
| Average output switching rate (f_p) | F/10 |
| Average first routed array clock rate (f_{q1}) | F |

Functional Timing Tests

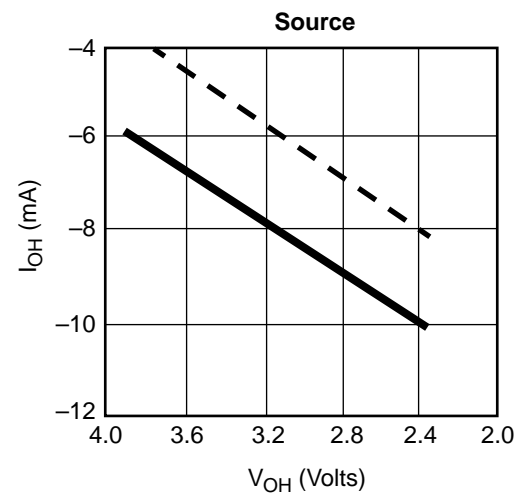
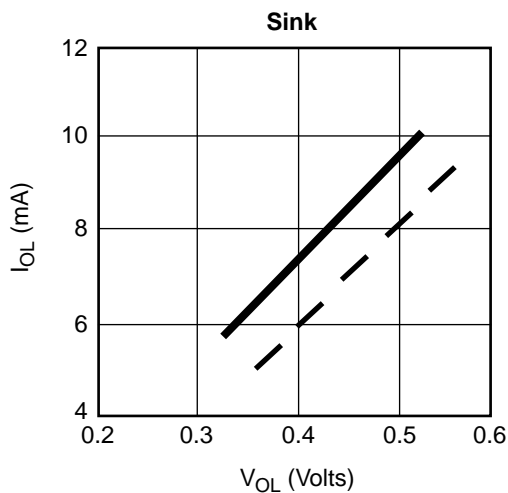
AC timing for logic module internal delays is determined after place and route. The DirectTime Analyzer utility displays actual timing parameters for circuit delays. ACT 1 devices are AC tested to a “binning” circuit specification.

The circuit consists of one input buffer + n logic modules + one output buffer (n = 16 for A1010B; n = 28 for A1020B). The

logic modules are distributed along two sides of the device, as inverting or non-inverting buffers. The modules are connected through programmed antifuses with typical capacitive loading.

Propagation delay [$t_{PD} = (t_{PLH} + t_{PHL})/2$] is tested to the following AC test specifications.

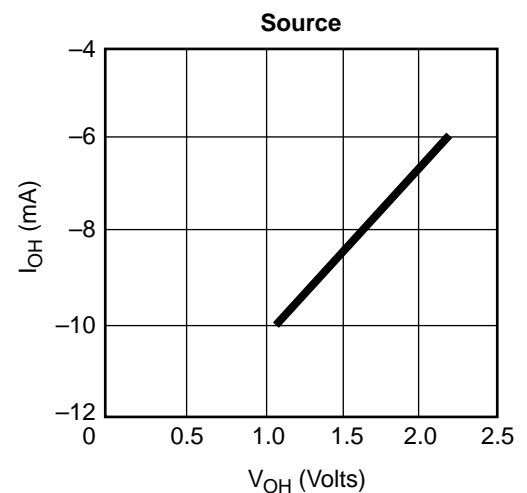
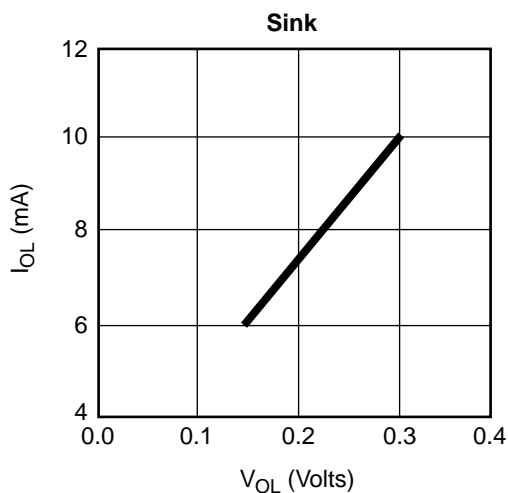
Output Buffer Performance Derating (5V)



--- Military, worst-case values at 125°C, 4.5 V.
 — Commercial, worst-case values at 70°C, 4.75 V.

Note: The above curves are based on characterizations of sample devices and are not completely tested on all devices.

Output Buffer Performance Derating (3.3V)



— Commercial, worst-case values at 70°C, 4.75 V.

Note: The above curves are based on characterizations of sample devices and are not completely tested on all devices.

ACT 1 Timing Module*



* Values shown for ACT 1 '-3 speed' devices at worst-case commercial conditions.

Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The ACT 1 family delivers a very tight fanout delay distribution. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The ACT 1 family's antifuses, fabricated in 1.0 micron lithography, offer nominal levels of 200 ohms resistance and 7.5 femtofarad (fF) capacitance per antifuse.

The ACT 1 fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The ACT 1 family's proprietary architecture limits the number of antifuses per path to a maximum of four, with 90% of interconnects using two antifuses.

Timing Characteristics

Timing characteristics for ACT 1 devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ACT 1 family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 5 ns to 10 ns delay. This additional delay is represented statistically in higher fanout ($FO=8$) routing delays in the data sheet specifications section.

Timing Derating

A best case timing derating factor of 0.45 is used to reflect best case processing. Note that this factor is relative to the

“standard speed” timing parameters, and must be multiplied by the appropriate voltage and temperature derating factors for a given application.

Timing Derating Factor (Temperature and Voltage)

| | Industrial | | Military | |
|--|------------|------|----------|------|
| | Min. | Max. | Min. | Max. |
| (Commercial Minimum/Maximum Specification) x | 0.69 | 1.11 | 0.67 | 1.23 |

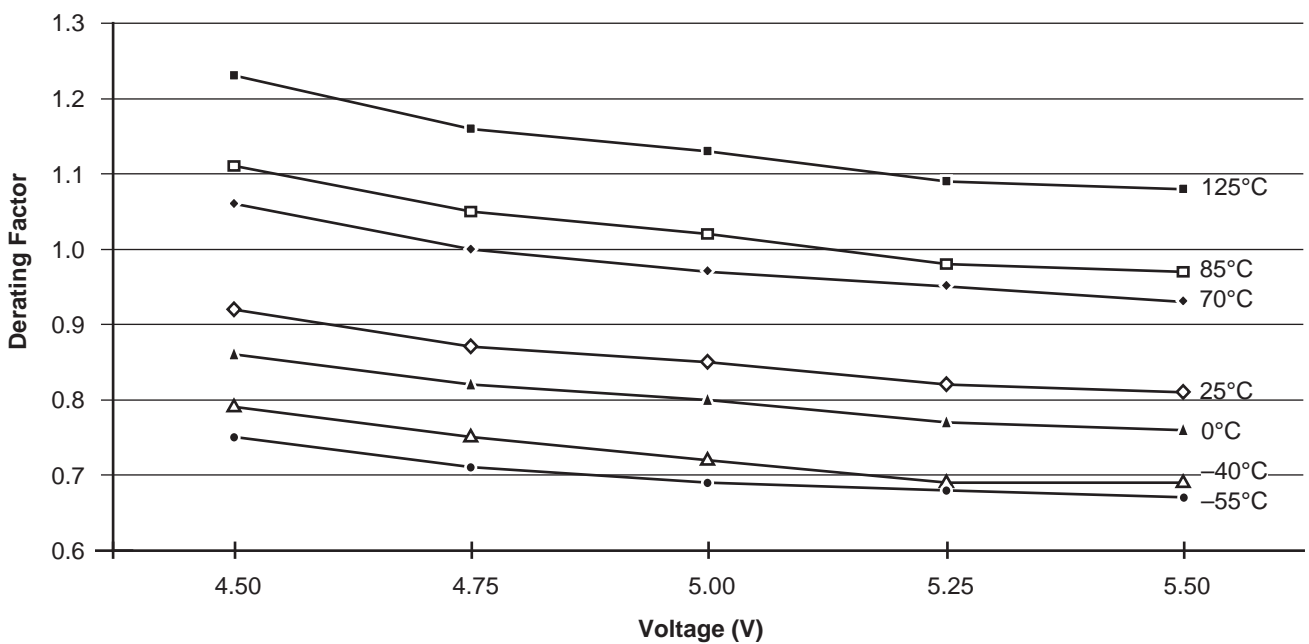
Timing Derating Factor for Designs at Typical Temperature ($T_J = 25^\circ\text{C}$) and Voltage (5.0 V)

| | |
|--------------------------------------|------|
| (Commercial Maximum Specification) x | 0.85 |
|--------------------------------------|------|

Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, $T_J = 4.75\text{ V}, 70^\circ\text{C}$)

| | -55 | -40 | 0 | 25 | 70 | 85 | 125 |
|------|------|------|------|------|------|------|------|
| 4.50 | 0.75 | 0.79 | 0.86 | 0.92 | 1.06 | 1.11 | 1.23 |
| 4.75 | 0.71 | 0.75 | 0.82 | 0.87 | 1.00 | 1.05 | 1.16 |
| 5.00 | 0.69 | 0.72 | 0.80 | 0.85 | 0.97 | 1.02 | 1.13 |
| 5.25 | 0.68 | 0.69 | 0.77 | 0.82 | 0.95 | 0.98 | 1.09 |
| 5.50 | 0.67 | 0.69 | 0.76 | 0.81 | 0.93 | 0.97 | 1.08 |

Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, $T_J = 4.75\text{ V}, 70^\circ\text{C}$)

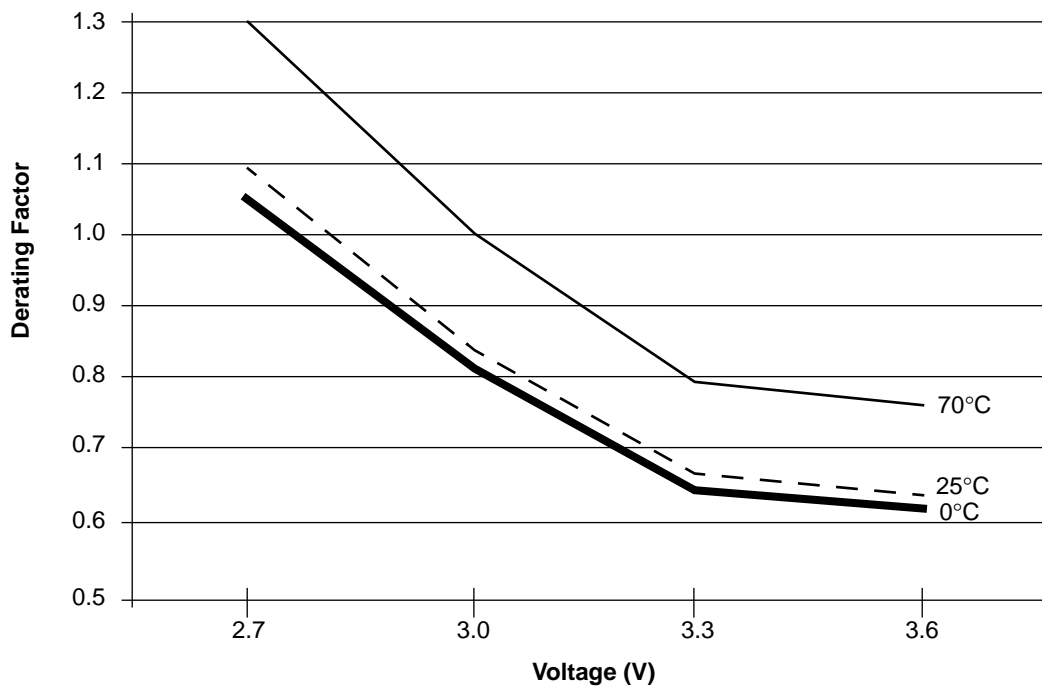


Note: This derating factor applies to all routing and propagation delays.

Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, $T_J = 3.0\text{ V}, 70^\circ\text{C}$)

| | 0 | 25 | 70 |
|-----|------|------|------|
| 2.7 | 1.05 | 1.09 | 1.30 |
| 3.0 | 0.81 | 0.84 | 1.00 |
| 3.3 | 0.64 | 0.67 | 0.79 |
| 3.6 | 0.62 | 0.64 | 0.76 |

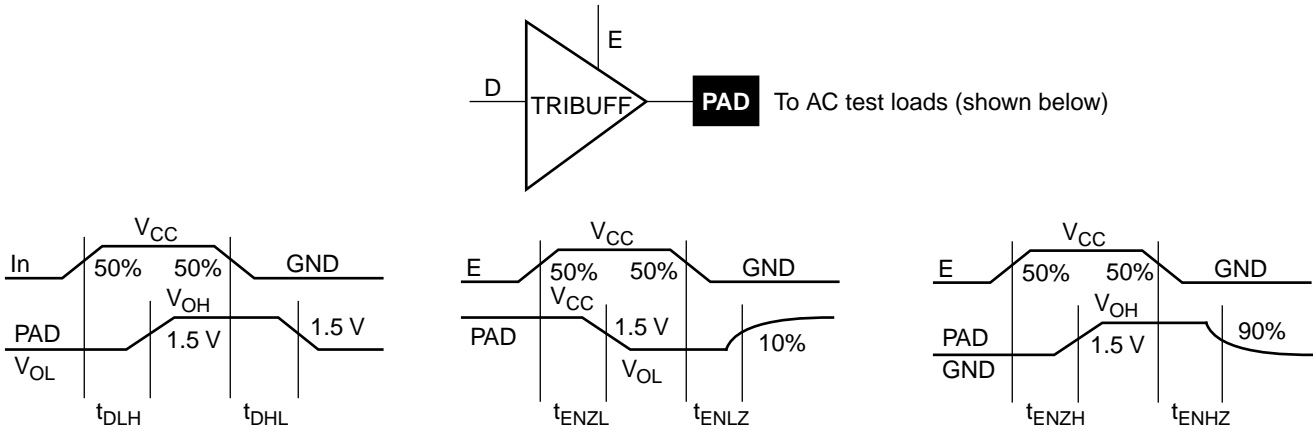
Junction Temperature and Voltage Derating Curves
(normalized to Worst-Case Commercial, $T_J = 3.0\text{ V}, 70^\circ\text{C}$)



Note: This derating factor applies to all routing and propagation delays.

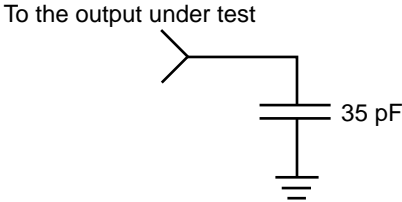
Parameter Measurement

Output Buffer Delays

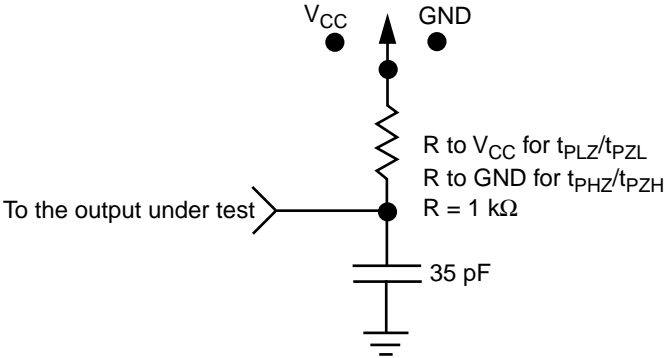


AC Test Loads

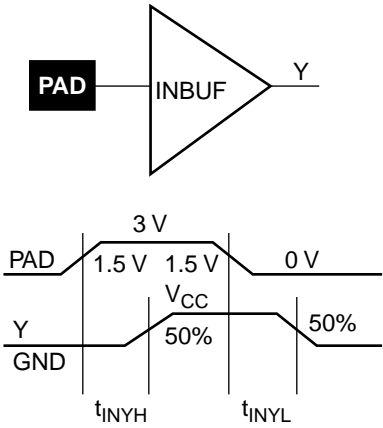
Load 1
(Used to measure propagation delay)



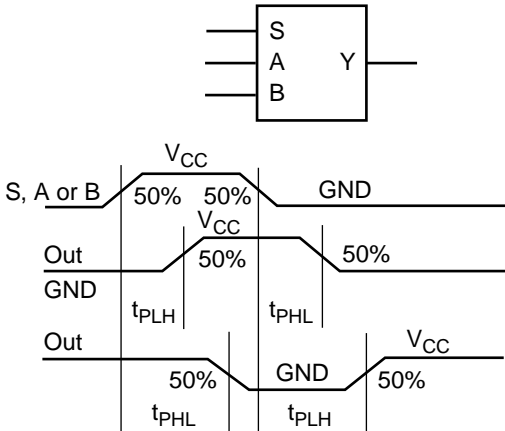
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

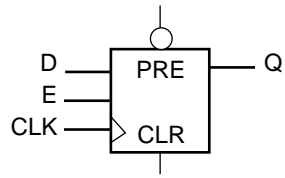


Module Delays

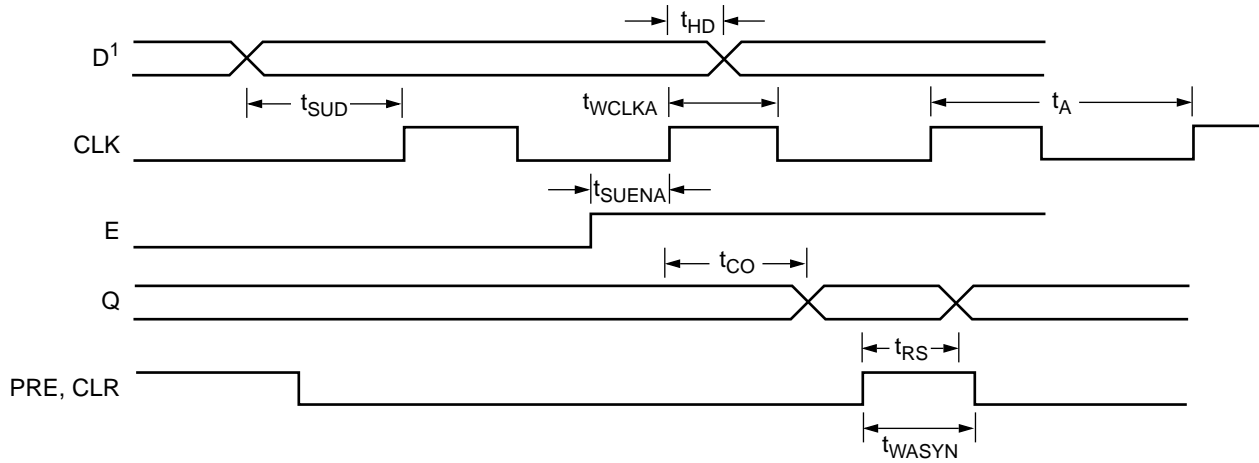


Sequential Timing Characteristics

Flip-Flops and Latches



(Positive edge triggered)



Note: D represents all data functions involving A , B , S for multiplexed flip-flops.

ACT 1 Timing Characteristics

(Worst-Case Commercial Conditions, $V_{CC} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)¹

| Logic Module Propagation Delays | | ‘-3’ Speed | | ‘-2’ Speed | | ‘-1’ Speed | | ‘Std’ Speed | | 3.3 V Speed | | |
|--|--|------------|------|------------|------|------------|------|-------------|------|-------------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| t _{PD1} | Single Module | | 2.9 | | 3.4 | | 3.8 | | 4.5 | | 6.5 | ns |
| t _{PD2} | Dual Module Macros | | 6.8 | | 7.8 | | 8.8 | | 10.4 | | 15.1 | ns |
| t _{CO} | Sequential Clk to Q | | 2.9 | | 3.4 | | 3.8 | | 4.5 | | 6.5 | ns |
| t _{GO} | Latch G to Q | | 2.9 | | 3.4 | | 3.8 | | 4.5 | | 6.5 | ns |
| t _{RS} | Flip-Flop (Latch) Reset to Q | | 2.9 | | 3.4 | | 3.8 | | 4.5 | | 6.5 | ns |
| Predicted Routing Delays² | | | | | | | | | | | | |
| t _{RD1} | FO=1 Routing Delay | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |
| t _{RD2} | FO=2 Routing Delay | | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.2 | ns |
| t _{RD3} | FO=3 Routing Delay | | 2.1 | | 2.5 | | 2.8 | | 3.3 | | 4.8 | ns |
| t _{RD4} | FO=4 Routing Delay | | 3.1 | | 3.6 | | 4.1 | | 4.8 | | 7.0 | ns |
| t _{RD8} | FO=8 Routing Delay | | 6.6 | | 7.7 | | 8.7 | | 10.2 | | 14.8 | ns |
| Sequential Timing Characteristics³ | | | | | | | | | | | | |
| t _{SUD} | Flip-Flop (Latch) Data Input Setup | 5.5 | | 6.4 | | 7.2 | | 8.5 | | 10.0 | | ns |
| t _{HD} ⁴ | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 5.5 | | 6.4 | | 7.2 | | 8.5 | | 10.0 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{WCLKA} | Flip-Flop (Latch) Clock Active Pulse Width | 6.8 | | 8.0 | | 9.0 | | 10.5 | | 9.8 | | ns |
| t _{WASYN} | Flip-Flop (Latch) Asynchronous Pulse Width | 6.8 | | 8.0 | | 9.0 | | 10.5 | | 9.8 | | ns |
| t _A | Flip-Flop Clock Input Period | 14.2 | | 16.7 | | 18.9 | | 22.3 | | 20.0 | | ns |
| f _{MAX} | Flip-Flop (Latch) Clock Frequency (FO = 128) | | 70 | | 60 | | 53 | | 45 | | 50 | MHz |

Notes:

1. $V_{CC} = 3.0\text{ V}$ for 3.3V specifications.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Setup times assume fanout of 3. Further testing information can be obtained from the DirectTime Analyzer utility.
4. The Hold Time for the DFME1A macro may be greater than 0 ns. Use the Designer 3.0 or later Timer to check the Hold Time for this macro.

ACT 1 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

| Input Module Propagation Delays | | | ‘-3’ Speed | | ‘-2’ Speed | | ‘-1’ Speed | | ‘Std’ Speed | | 3.3 V Speed | | |
|--|-----------------------------|----------|------------|------|------------|------|------------|------|-------------|------|-------------|------|-------|
| Parameter | Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| t _{INYH} | Pad to Y High | | | 3.1 | | 3.5 | | 4.0 | | 4.7 | | 6.8 | ns |
| t _{INYL} | Pad to Y Low | | | 3.1 | | 3.5 | | 4.0 | | 4.7 | | 6.8 | ns |
| Input Module Predicted Routing Delays¹ | | | | | | | | | | | | | |
| t _{IRD1} | FO=1 Routing Delay | | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |
| t _{IRD2} | FO=2 Routing Delay | | | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.2 | ns |
| t _{IRD3} | FO=3 Routing Delay | | | 2.1 | | 2.5 | | 2.8 | | 3.3 | | 4.8 | ns |
| t _{IRD4} | FO=4 Routing Delay | | | 3.1 | | 3.6 | | 4.1 | | 4.8 | | 7.0 | ns |
| t _{IRD8} | FO=8 Routing Delay | | | 6.6 | | 7.7 | | 8.7 | | 10.2 | | 14.8 | ns |
| Global Clock Network | | | | | | | | | | | | | |
| t _{CKH} | Input Low to High | FO = 16 | | 4.9 | | 5.6 | | 6.4 | | 7.5 | | 6.7 | ns |
| | | FO = 128 | | 5.6 | | 6.4 | | 7.3 | | 8.6 | | 7.9 | |
| t _{CKL} | Input High to Low | FO = 16 | | 6.4 | | 7.4 | | 8.4 | | 9.9 | | 8.8 | ns |
| | | FO = 128 | | 7.0 | | 8.1 | | 9.2 | | 10.8 | | 10.0 | |
| t _{PWH} | Minimum Pulse Width High | FO = 16 | | 6.5 | | 7.5 | | 8.5 | | 10.0 | | 8.9 | ns |
| | | FO = 128 | | 6.8 | | 8.0 | | 9.0 | | 10.5 | | 9.8 | |
| t _{PWL} | Minimum Pulse Width Low | FO = 16 | | 6.5 | | 7.5 | | 8.5 | | 10.0 | | 8.9 | ns |
| | | FO = 128 | | 6.8 | | 8.0 | | 9.0 | | 10.5 | | 9.8 | |
| t _{CKSW} | Maximum Skew | FO = 16 | | 1.2 | | 1.3 | | 1.5 | | 1.8 | | 1.5 | ns |
| | | FO = 128 | | 1.8 | | 2.1 | | 2.4 | | 2.8 | | 2.4 | |
| t _P | Minimum Period | FO = 16 | | 13.2 | | 15.4 | | 17.6 | | 20.9 | | 18.2 | ns |
| | | FO = 128 | | 14.2 | | 16.7 | | 18.9 | | 22.3 | | 20 | |
| f _{MAX} | Maximum Frequency | FO = 16 | | 75 | | 65 | | 57 | | 48 | | 55 | MHz |
| | | FO = 128 | | 70 | | 60 | | 53 | | 45 | | 50 | |

Note:

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

ACT 1 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

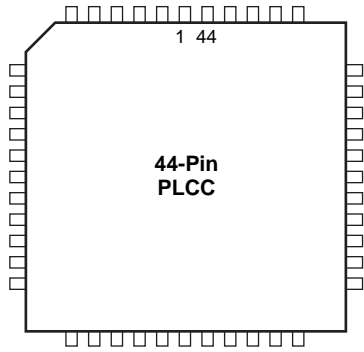
| Output Module Timing | | ‘-3’ Speed | | ‘-2’ Speed | | ‘-1’ Speed | | ‘Std’ Speed | | 3.3 V Speed | | |
|--|----------------------|------------|------|------------|------|------------|------|-------------|------|-------------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| TTL Output Module Timing¹ | | | | | | | | | | | | |
| t _{DLH} | Data to Pad High | 6.7 | 7.6 | 7.6 | 8.7 | 8.7 | 10.3 | 10.3 | 15.0 | 15.0 | | ns |
| t _{DHL} | Data to Pad Low | 7.5 | 8.6 | 8.6 | 9.8 | 9.8 | 11.5 | 11.5 | 16.7 | 16.7 | | ns |
| t _{ENZH} | Enable Pad Z to High | 6.6 | 7.5 | 7.5 | 8.6 | 8.6 | 10.2 | 10.2 | 14.8 | 14.8 | | ns |
| t _{ENZL} | Enable Pad Z to Low | 7.9 | 9.1 | 9.1 | 10.4 | 10.4 | 12.2 | 12.2 | 17.7 | 17.7 | | ns |
| t _{ENHZ} | Enable Pad High to Z | 10.0 | 11.6 | 11.6 | 13.1 | 13.1 | 15.4 | 15.4 | 22.4 | 22.4 | | ns |
| t _{ENLZ} | Enable Pad Low to Z | 9.0 | 10.4 | 10.4 | 11.8 | 11.8 | 13.9 | 13.9 | 20.2 | 20.2 | | ns |
| d _{TLH} | Delta Low to High | 0.06 | 0.07 | 0.07 | 0.08 | 0.08 | 0.09 | 0.09 | 0.13 | 0.13 | | ns/pF |
| d _{THL} | Delta High to Low | 0.08 | 0.09 | 0.09 | 0.10 | 0.10 | 0.12 | 0.12 | 0.17 | 0.17 | | ns/pF |
| CMOS Output Module Timing¹ | | | | | | | | | | | | |
| t _{DLH} | Data to Pad High | 7.9 | 9.2 | 9.2 | 10.4 | 10.4 | 12.2 | 12.2 | 17.7 | 17.7 | | ns |
| t _{DHL} | Data to Pad Low | 6.4 | 7.2 | 7.2 | 8.2 | 8.2 | 9.8 | 9.8 | 14.2 | 14.2 | | ns |
| t _{ENZH} | Enable Pad Z to High | 6.0 | 6.9 | 6.9 | 7.9 | 7.9 | 9.2 | 9.2 | 13.4 | 13.4 | | ns |
| t _{ENZL} | Enable Pad Z to Low | 8.3 | 9.4 | 9.4 | 10.7 | 10.7 | 12.7 | 12.7 | 18.5 | 18.5 | | ns |
| t _{ENHZ} | Enable Pad High to Z | 10.0 | 11.6 | 11.6 | 13.1 | 13.1 | 15.4 | 15.4 | 22.4 | 22.4 | | ns |
| t _{ENLZ} | Enable Pad Low to Z | 9.0 | 10.4 | 10.4 | 11.8 | 11.8 | 13.9 | 13.9 | 20.2 | 20.2 | | ns |
| d _{TLH} | Delta Low to High | 0.10 | 0.11 | 0.11 | 0.13 | 0.13 | 0.15 | 0.15 | 0.22 | 0.22 | | ns/pF |
| d _{THL} | Delta High to Low | 0.06 | 0.07 | 0.07 | 0.08 | 0.08 | 0.09 | 0.09 | 0.13 | 0.13 | | ns/pF |

Notes:

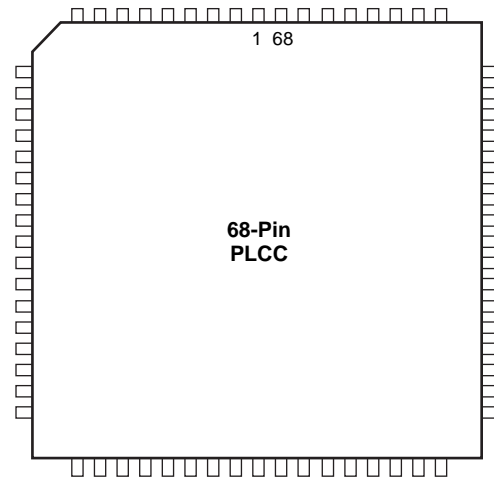
1. Delays based on 35 pF loading.
2. SSO information can be found in the “Simultaneous Switching Output Limits for Actel FPGAs” application note on page 4-125.

Package Pin Assignments

44-Pin PLCC



68-Pin PLCC



| Signal | A1010B Function | A1020B Function |
|--------|-----------------|-----------------|
| 3 | VCC | VCC |
| 10 | GND | GND |
| 14 | VCC | VCC |
| 16 | VCC | VCC |
| 21 | GND | GND |
| 25 | VCC | VCC |
| 32 | GND | GND |
| 33 | CLK, I/O | CLK, I/O |
| 34 | MODE | MODE |
| 35 | VCC | VCC |
| 36 | SDI, I/O | SDI, I/O |
| 37 | DCLK, I/O | DCLK, I/O |
| 38 | PRA, I/O | PRA, I/O |
| 39 | PRB, I/O | PRB, I/O |
| 43 | GND | GND |

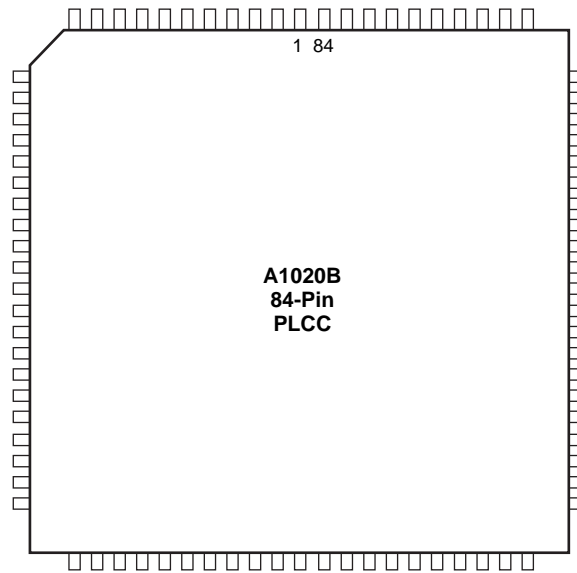
| Signal | A1010B, A10V10B Function | A1020B, A10V20B Functions |
|--------|--------------------------|---------------------------|
| 4 | VCC | VCC |
| 14 | GND | GND |
| 15 | GND | GND |
| 21 | VCC | VCC |
| 25 | VCC | VCC |
| 32 | GND | GND |
| 38 | VCC | VCC |
| 49 | GND | GND |
| 52 | CLK, I/O | CLK, I/O |
| 54 | MODE | MODE |
| 55 | VCC | VCC |
| 56 | SDI, I/O | SDI, I/O |
| 57 | DCLK, I/O | DCLK, I/O |
| 58 | PRA, I/O | PRA, I/O |
| 59 | PRB, I/O | PRB, I/O |
| 66 | GND | GND |

Notes:

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

84-Pin PLCC



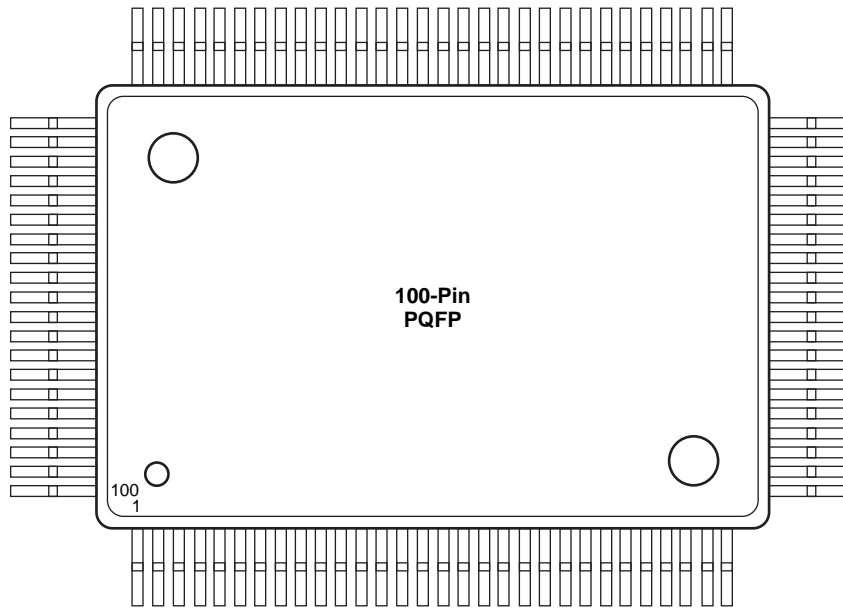
| Signal | A1020B, A10V20B Function |
|--------|--------------------------|
| 4 | VCC |
| 12 | NC |
| 18 | GND |
| 19 | GND |
| 25 | VCC |
| 26 | VCC |
| 33 | VCC |
| 40 | GND |
| 46 | VCC |
| 60 | GND |
| 61 | GND |
| 64 | CLK, I/O |
| 66 | MODE |
| 67 | VCC |
| 68 | VCC |
| 72 | SDI, I/O |
| 73 | DCLK, I/O |
| 74 | PRA, I/O |
| 75 | PRB, I/O |
| 82 | GND |

Notes:

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

100-Pin PQFP



| Pin | A1010B Function | A1020B Function |
|-----|-----------------|-----------------|
| 1 | NC | NC |
| 2 | NC | NC |
| 3 | NC | NC |
| 4 | NC | NC |
| 5 | NC | NC |
| 6 | PRB, I/O | PRB, I/O |
| 13 | GND | GND |
| 19 | VCC | VCC |
| 27 | NC | NC |
| 28 | NC | NC |
| 29 | NC | NC |
| 30 | NC | NC |
| 31 | NC | I/O |
| 32 | NC | I/O |
| 33 | NC | I/O |
| 36 | GND | GND |
| 37 | GND | GND |
| 43 | VCC | VCC |
| 44 | VCC | VCC |
| 48 | NC | I/O |
| 49 | NC | I/O |
| 50 | NC | I/O |
| 51 | NC | NC |
| 52 | NC | NC |

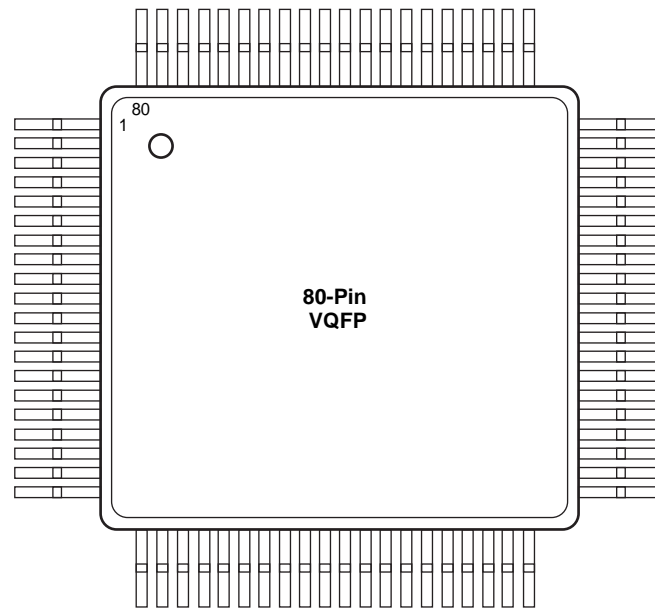
| Pin | A1010B Function | A1020B Function |
|-----|-----------------|-----------------|
| 53 | NC | NC |
| 54 | NC | NC |
| 55 | NC | NC |
| 56 | VCC | VCC |
| 63 | GND | GND |
| 69 | VCC | VCC |
| 77 | NC | NC |
| 78 | NC | NC |
| 79 | NC | NC |
| 80 | NC | I/O |
| 81 | NC | I/O |
| 82 | NC | I/O |
| 86 | GND | GND |
| 87 | GND | GND |
| 90 | CLK, I/O | CLK, I/O |
| 92 | MODE | MODE |
| 93 | VCC | VCC |
| 94 | VCC | VCC |
| 95 | NC | I/O |
| 96 | NC | I/O |
| 97 | NC | I/O |
| 98 | SDI, I/O | SDI, I/O |
| 99 | DCLK, I/O | DCLK, I/O |
| 100 | PRA, I/O | PRA, I/O |

Notes:

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

80-Pin VQFP



| Pin | A1010B, A10V10B Function | A1020B, A10V20B Function |
|-----|-----------------------------|-----------------------------|
| 2 | NC | I/O |
| 3 | NC | I/O |
| 4 | NC | I/O |
| 7 | GND | GND |
| 13 | VCC | VCC |
| 17 | NC | I/O |
| 18 | NC | I/O |
| 19 | NC | I/O |
| 20 | VCC | VCC |
| 27 | GND | GND |
| 33 | VCC | VCC |
| 41 | NC | I/O |
| 42 | NC | I/O |
| 43 | NC | I/O |

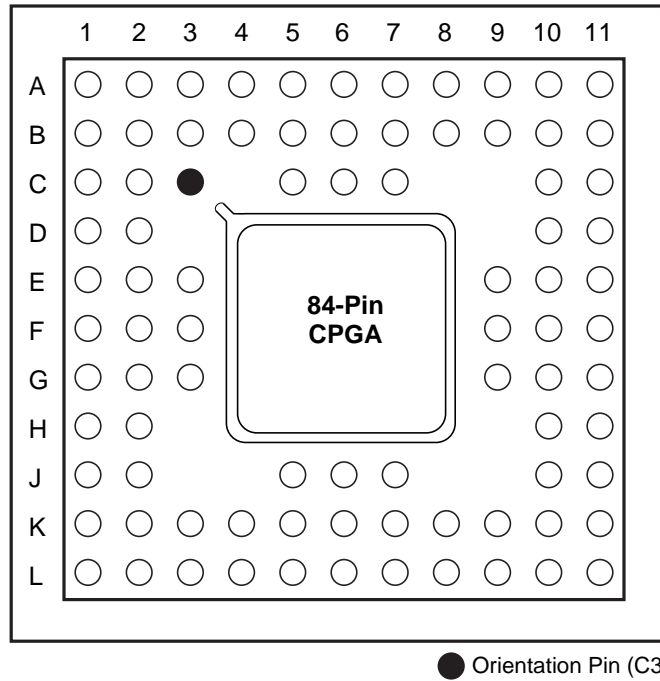
| Pin | A1010B, A10V10B Function | A1020B, A10V20B Function |
|-----|-----------------------------|-----------------------------|
| 47 | GND | GND |
| 50 | CLK, I/O | CLK, I/O |
| 52 | MODE | MODE |
| 53 | VCC | VCC |
| 54 | NC | I/O |
| 55 | NC | I/O |
| 56 | NC | I/O |
| 57 | SDI, I/O | SDI, I/O |
| 58 | DCLK, I/O | DCLK, I/O |
| 59 | PRA, I/O | PRA, I/O |
| 60 | NC | NC |
| 61 | PRB, I/O | PRB, I/O |
| 68 | GND | GND |
| 74 | VCC | VCC |

Notes:

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

84-Pin CPGA



| Pin | A1010B Function | A1020B Function |
|-----|-----------------|-----------------|
| A11 | PRA, I/O | PRA, I/O |
| B1 | NC | I/O |
| B2 | NC | NC |
| B5 | VCC | VCC |
| B7 | GND | GND |
| B10 | PRB, I/O | PRB, I/O |
| B11 | SDI, I/O | SDI, I/O |
| C1 | NC | I/O |
| C2 | NC | I/O |
| C10 | DCLK, I/O | DCLK, I/O |
| C11 | NC | I/O |
| D10 | NC | I/O |
| D11 | NC | I/O |
| E2 | GND | GND |
| E3 | GND | GND |
| E9 | VCC | VCC |

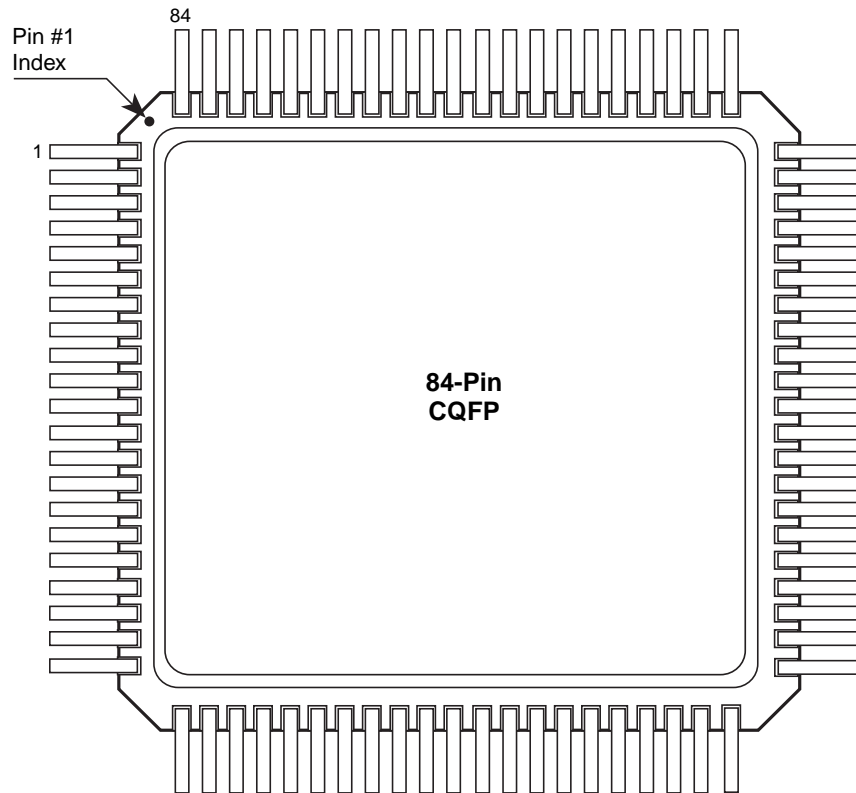
| Pin | A1010B Function | A1020B Function |
|-----|-----------------|-----------------|
| E10 | VCC | VCC |
| E11 | MODE | MODE |
| F1 | VCC | VCC |
| F9 | CLK, I/O | CLK, I/O |
| F10 | GND | GND |
| G2 | VCC | VCC |
| G10 | GND | GND |
| J2 | NC | I/O |
| J10 | NC | I/O |
| K1 | NC | I/O |
| K2 | VCC | VCC |
| K5 | GND | GND |
| K7 | VCC | VCC |
| K10 | NC | I/O |
| K11 | NC | I/O |
| L1 | NC | I/O |

Notes:

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

84-Pin CQFP



| Pin | A1020B Function |
|-----|-----------------|
| 1 | NC |
| 7 | GND |
| 8 | GND |
| 14 | VCC |
| 15 | VCC |
| 22 | VCC |
| 29 | GND |
| 35 | VCC |
| 49 | GND |
| 50 | GND |

| Pin | A1020B Function |
|-----|-----------------|
| 53 | CLK, I/O |
| 55 | MODE |
| 56 | VCC |
| 57 | VCC |
| 61 | SDI, I/O |
| 62 | DCLK, I/O |
| 63 | PRA, I/O |
| 64 | PRB, I/O |
| 71 | GND |
| 77 | VCC |

Notes:

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

